EG800P-CN QuecOpen Reference Design

LTE Standard Module Series

Version: 1.0

Date: 2024-06-03

Status: Released

At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
http://www.quectel.com/support/sales.htm.
For technical support, or to report documentation errors, please visit:
http://www.quectel.com/support/technical.htm.
Or email us at: support@quectel.com.

Legal Notices

We offer information as a service to you. The provided information is based on your requirements and we make every effort to ensure its quality. You agree that you are responsible for using independent analysis and evaluation in designing intended products, and we provide reference designs for illustrative purposes only. Before using any hardware, software or service guided by this document, please read this notice carefully. Even though we employ commercially reasonable efforts to provide the best possible experience, you hereby acknowledge and agree that this document and related services hereunder are provided to you on an “as available” basis. We may revise or restate this document from time to time at our sole discretion without any prior notice to you.

Use and Disclosure Restrictions

License Agreements

Documents and information provided by us shall be kept confidential, unless specific permission is granted. They shall not be accessed or used for any purpose except as expressly provided herein.

Copyright

Our and third-party products hereunder may contain copyrighted material. Such copyrighted material shall not be copied, reproduced, distributed, merged, published, translated, or modified without prior written consent. We and the third party have exclusive rights over copyrighted material. No license shall be granted or conveyed under any patents, copyrights, trademarks, or service mark rights. To avoid ambiguities, purchasing in any form cannot be deemed as granting a license other than the normal non-exclusive, royalty-free license to use the material. We reserve the right to take legal action for noncompliance with abovementioned requirements, unauthorized use, or other illegal or malicious use of the material.

Trademarks

Except as otherwise set forth herein, nothing in this document shall be construed as conferring any rights to use any trademark, trade name or name, abbreviation, or counterfeit product thereof owned by Quectel or any third party in advertising, publicity, or other aspects.

Third-Party Rights

This document may refer to hardware, software and/or documentation owned by one or more third parties ("third-party materials"). Use of such third-party materials shall be governed by all restrictions and obligations applicable thereto.

We make no warranty or representation, either express or implied, regarding the third-party materials, including but not limited to any implied or statutory, warranties of merchantability or fitness for a particular purpose, quiet enjoyment, system integration, information accuracy, and non-infringement of any third-party intellectual property rights with regard to the licensed technology or use thereof. Nothing herein constitutes a representation or warranty by us to either develop, enhance, modify, distribute, market, sell, offer for sale, or otherwise maintain production of any our products or any other hardware, software, device, tool, information, or product. We moreover disclaim any and all warranties arising from the course of dealing or usage of trade.

Privacy Policy

To implement module functionality, certain device data are uploaded to Quectel's or third-party's servers, including carriers, chipset suppliers or customer-designated servers. Quectel, strictly abiding by the relevant laws and regulations, shall retain, use, disclose or otherwise process relevant data for the purpose of performing the service only or as permitted by applicable laws. Before data interaction with third parties, please be informed of their privacy and data security policy.

Disclaimer

a) We acknowledge no liability for any injury or damage arising from the reliance upon the information.
b) We shall bear no liability resulting from any inaccuracies or omissions, or from the use of the information contained herein.
c) While we have made every effort to ensure that the functions and features under development are free from errors, it is possible that they could contain errors, inaccuracies, and omissions. Unless otherwise provided by valid agreement, we make no warranties of any kind, either implied or express, and exclude all liability for any loss or damage suffered in connection with the use of features and functions under development, to the maximum extent permitted by law, regardless of whether such loss or damage may have been foreseeable.
d) We are not responsible for the accessibility, safety, accuracy, availability, legality, or completeness of information, advertising, commercial offers, products, services, and materials on third-party websites and third-party resources.

About the Document

Revision History

Version	Date	Author	Description
-	2023-11-06	Mark YANG/ Janko LI	Creation of the document
1.0	2024-06-03	Mark YANG/ Janko LI	First official release

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EG800P-CN module in QuecOpen® solution, including block diagram, power system block diagram, module interfaces, power supply design, USIM interface, UART, LCM interface, camera interface and other designs.

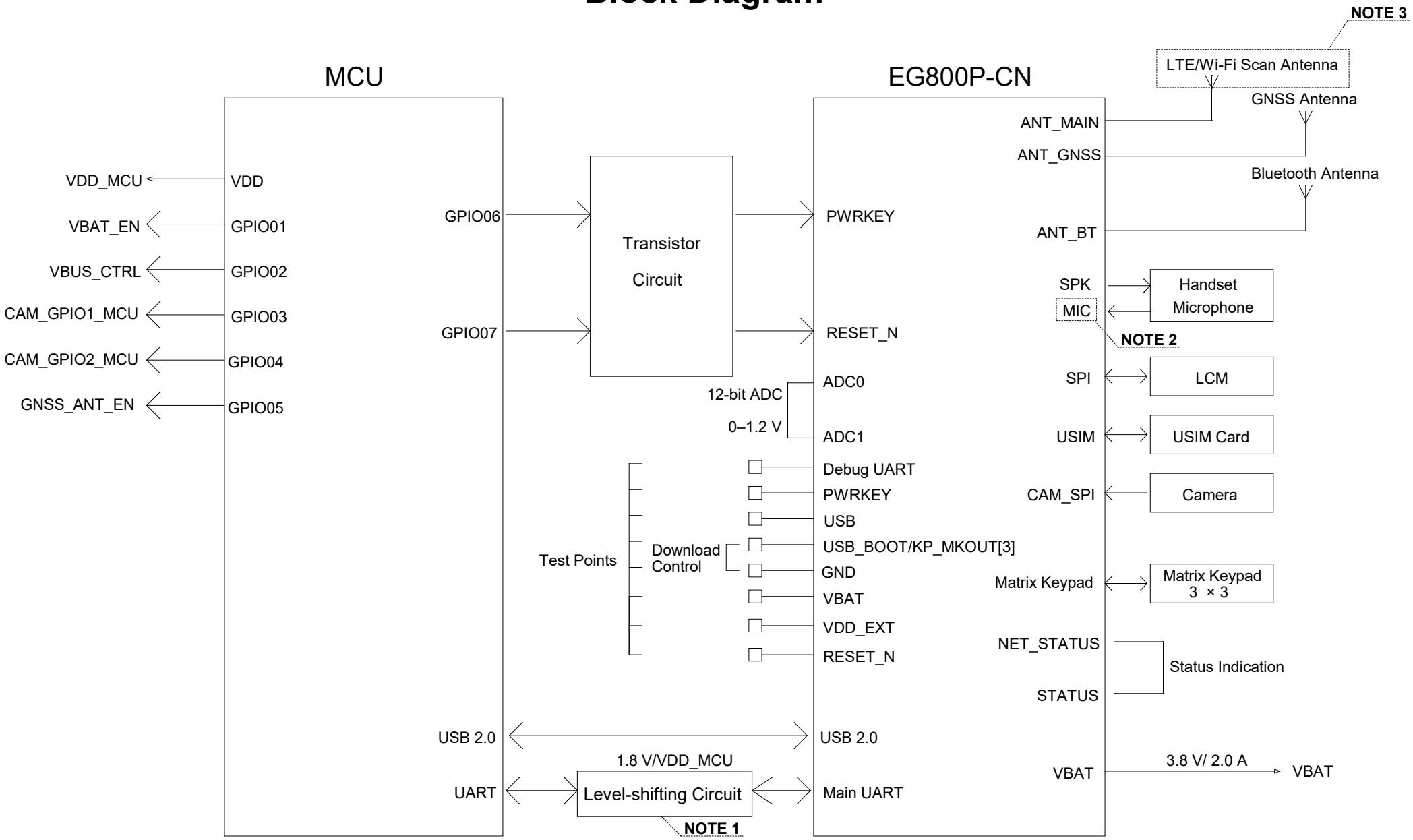
1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

NOTE

It is required to confirm the applicability and price from the supplier about the IC involved in the reference design.

Block Diagram

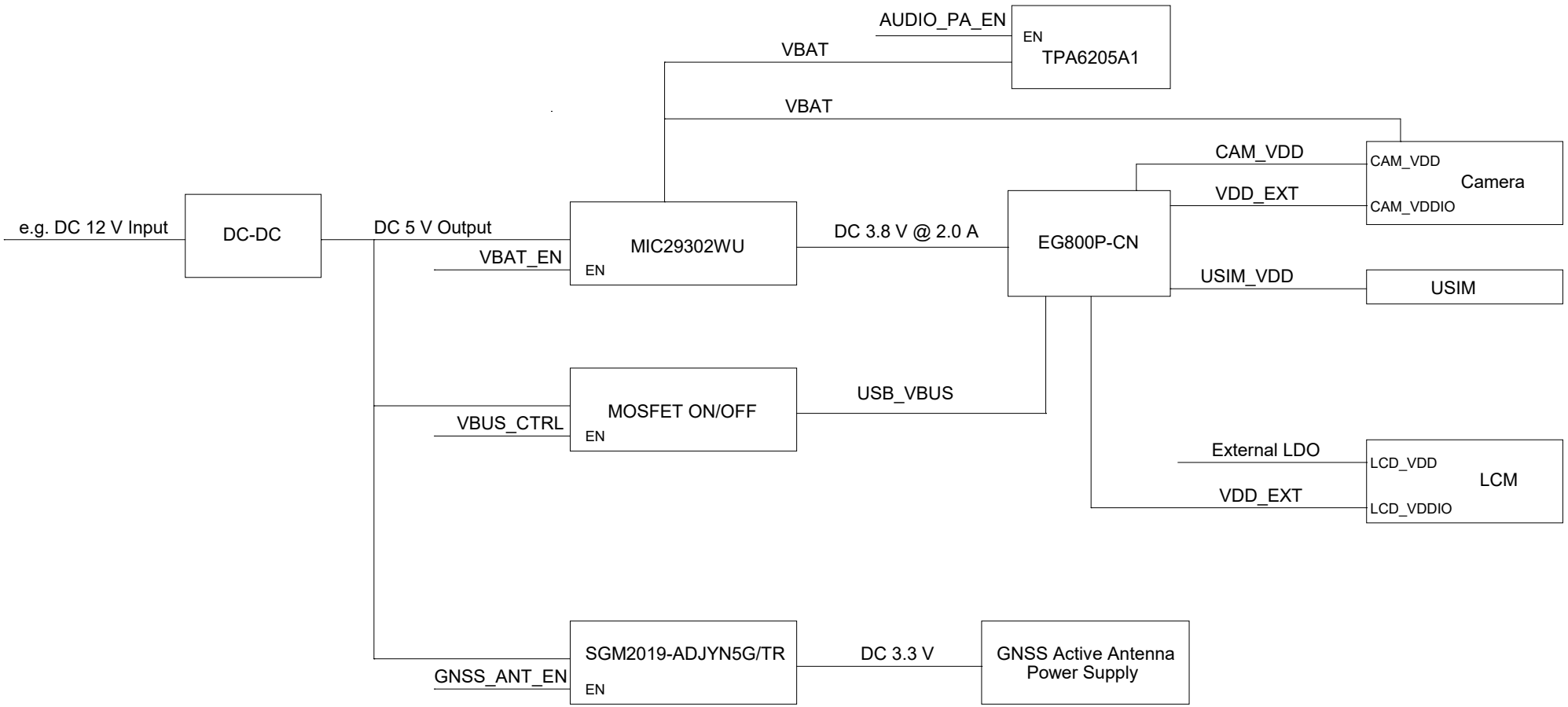


NOTE:

1. A transistor solution or an IC solution TXS0108EPWR provided by Texas Instruments is recommended.
2. The analog audio input channel requires an external microphone bias circuit. And MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO.
3. The module supports Wi-Fi Scan function. Wi-Fi Scan that only supports receiving shares the same antenna interface with main antenna, thus the two functions cannot be used at the same time.

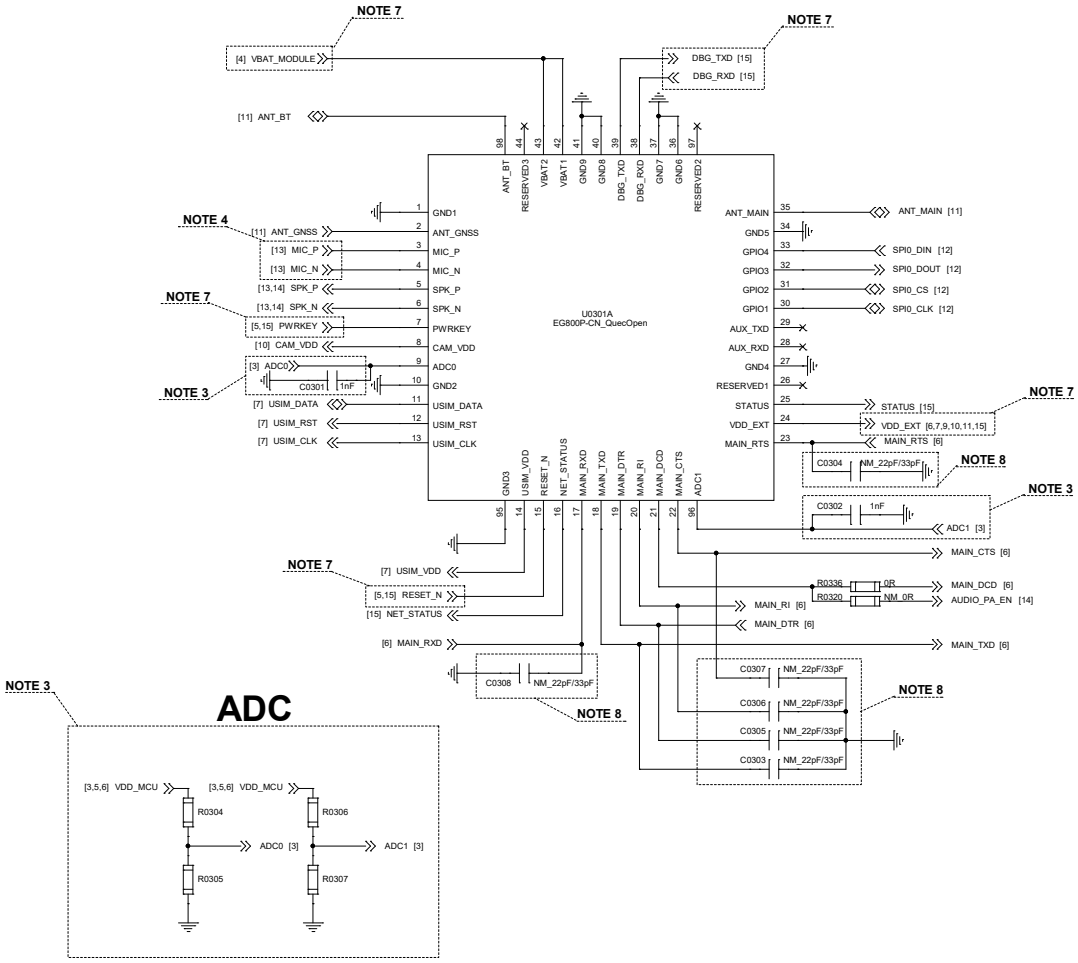
Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 1 OF 15	

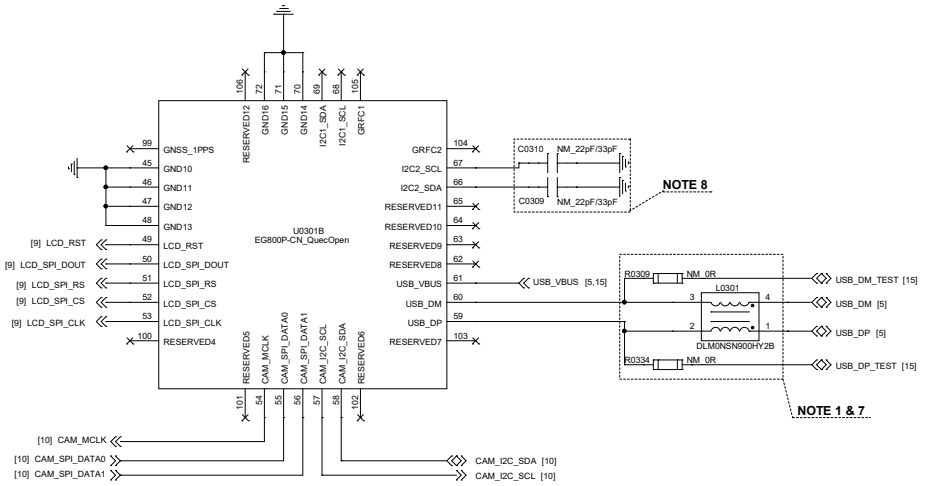
Power System Block Diagram

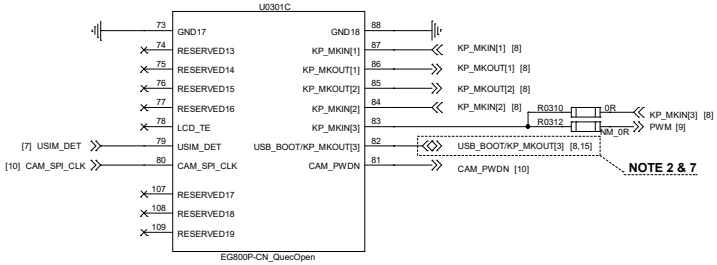


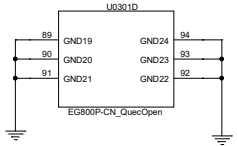
Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 2 OF 15	

Module Interfaces









NOTE:

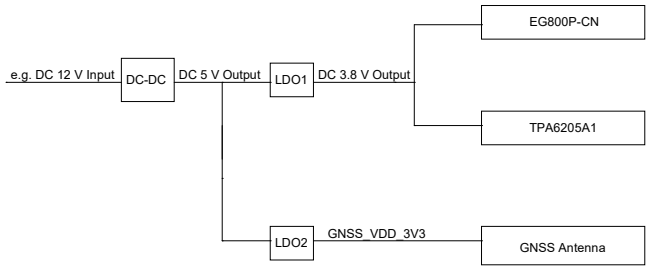
1. It is recommended to add a common mode choke L0301 in series between the module and your MCU to suppress EMI.
   Additionally, test points must be reserved over USB_DP and USB_DM for firmware upgrades, and it is recommended to minimize extra trace stubs.
   Place L0301 and two resistors, R0309 and R0334, close to the module to ensure USB signal integrity.
2. USB_BOOT/KP_MKOUT[3] cannot be pulled down to low level before the module starts up successfully.
3. The input voltage range of ADC0 and ADC1 is 0–1.2 V. A voltage divider circuit with two resistors must be used for ADC0 and ADC1 voltage inputs respectively, and the required resistance of the two resistors that connected to VDD_MCU (R0304 and R0306) is between 100 kΩ and 1 MΩ. The accuracy of the resistors directly affects ADC sampling error.
   It is recommended to use resistors with 1 % accuracy. For higher ADC accuracy, resistors with 0.5 % accuracy are recommended.
4. The analog audio input channel requires an external microphone bias circuit. And MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO.
5. Connect all GND pins to ground, and keep unused and RESERVED pins open.
6. Ensure an uninterrupted reference ground plane below the module, with minimal distance between the ground plane and the module layer.
   Avoid routing other traces on the first layer adjacent to the module layer. At least four-layer board design is recommended.
7. Test points must be reserved for DBG_TXD/RXD, USB_DP/DM and USB_VBUS. It is recommended to reserve test points for VDD_EXT, USB_BOOT/KP_MKOUT[3], PWRKEY and VBAT.
   If RESET_N is unused, it is recommended to reserve a test point.
8. If pins 17–20, 22, 23, 66 and 67 of module are required, the 22 pF or 33 pF filter capacitors should be reserved and placed near the pins, and the return path for current of capacitors to the main ground should be as short as possible. The capacitance should be selected according to the actual debugging situation.

Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 3 OF 15	

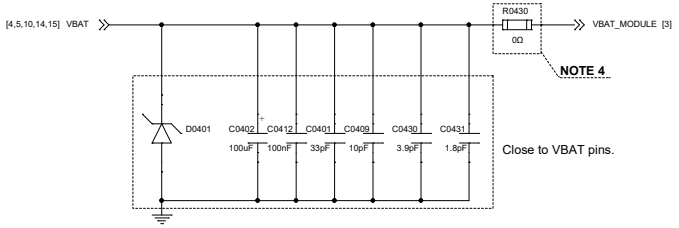
Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to 5.0 V, and then use LDOs to convert it to 3.8 V, 3.3 V to supply the module, audio PA and GNSS antenna.



VBAT Design

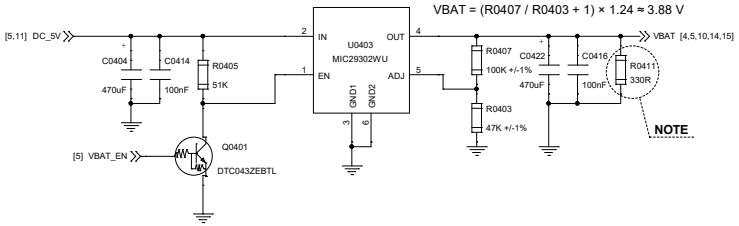


NOTE:

1. The power supply for the module should be capable of supplying a minimum current of 2.0 A.
2. The width of VBAT trace should be at least 2 mm.
3. The recommended operating voltage range for VBAT is 3.4 V to 4.3 V, with a typical value of 3.8 V.
4. It is recommended to reserve a 0 Ω resistor (minimum package size: R-0603) near the VBAT pins for future debugging purposes.

LDO Application

When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



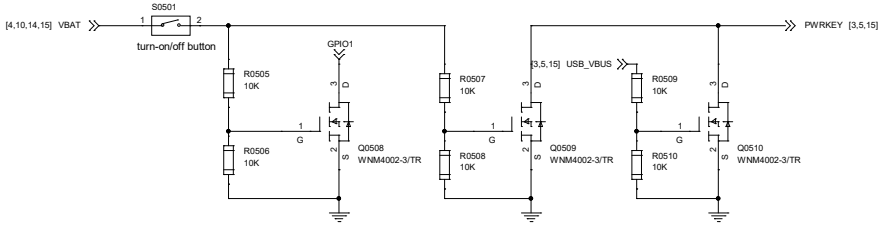
NOTE:

The recommended load current should exceed 10 mA.

Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 4 OF 15	

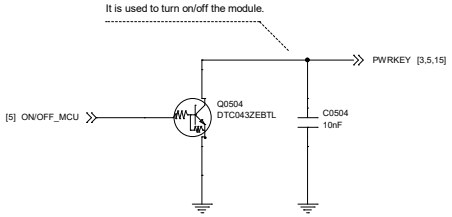
MCU Interfaces

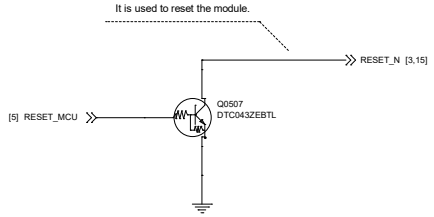
USB Insertion Enables Automatic Boot

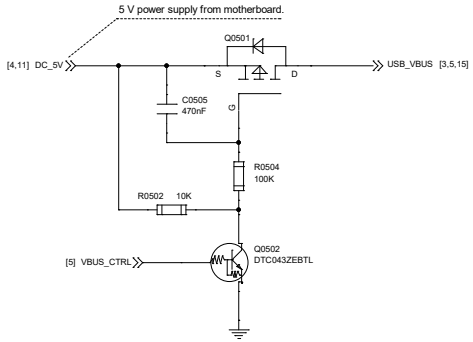


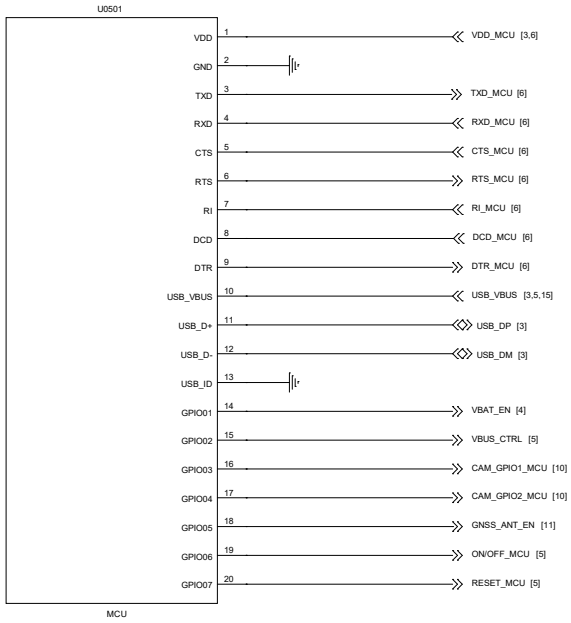
NOTE:

1. When USB is inserted, the module cannot be shut down normally, and will boot automatically after the shut down.
2. When USB is inserted, the level states of GPIO1 and PWRKEY pins are used to determine whether the module is turned on by the turn-on/off button or USB insertion.
   GPIO1 utilizes the GPIO resource with a default pull-up (PU) state.









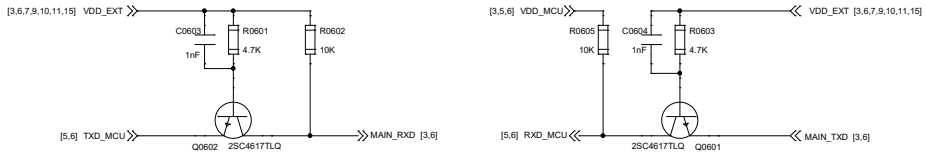
NOTE:

1. If the power domain of your MCU (U0401) is also 1.8 V, the level-shifting circuit is not necessary as it matches the 1.8 V power domain of the module's GPIO interfaces.
2. The USB interface of the module can only serve as a slave device and supports full-speed and high-speed modes of USB 2.0. To communicate with the USB interface, MCU needs to support USB host mode or OTG function.
   For USB detection, the USB_VBUS pin of the module should be powered by an external power system. Use VBUS_CTRL to control the on/off state of the USB_VBUS power supply.
3. It is recommended to choose MCU GPIO pins with a default low level to control the module's PWRKEY and RESET_N pins. Ensure that the load capacitance on these pins does not exceed 10 nF.

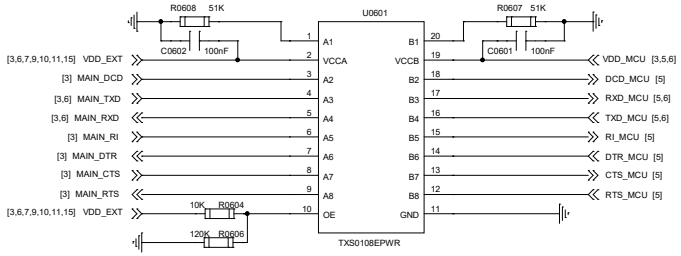
Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 5 OF 15	

UART Interface Design

UART Level-shifting Circuit - Transistor Solution



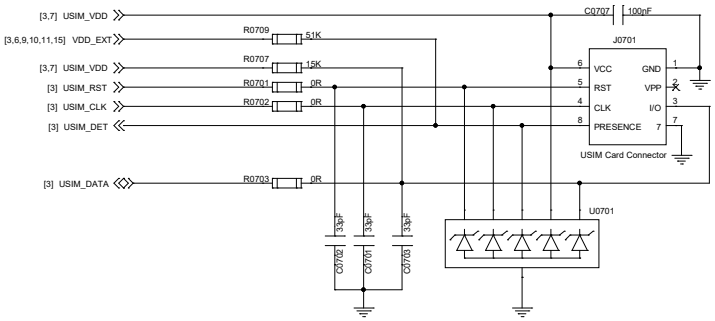
UART Level-shifting Circuit - IC Solution



NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter one.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, refer to the datasheet of TXS0108EPWR.
3. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C0603 and C0604 of 1 nF can improve the signal quality.
4. MAIN_RTS and MAIN_DTR level-shifting circuits are similar to that of the MAIN_RXD interface.
   MAIN_CTS, MAIN_RI and MAIN_DCD level-shifting circuits are similar to that of the MAIN_TXD interface.
5. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

USIM Interface Design

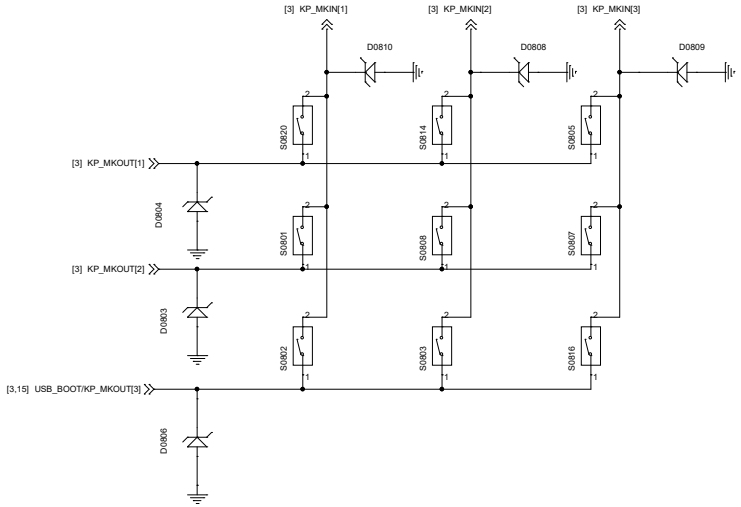


NOTE:

1. It is recommended to use U0701 for effective ESD protection with a parasitic capacitance below 15 pF.
2. For USIM_DATA, it is recommended to add a 15 kΩ pull-up resistor R0707 near the USIM card connector to improve the anti-jamming capability of the USIM card.
3. R0701–R0703 are used for debugging, and C0701–C0703 are used for filtering out RF interference.
4. The capacitance of C0707 should be less than 1 μF and it should be placed close to the USIM card connector.

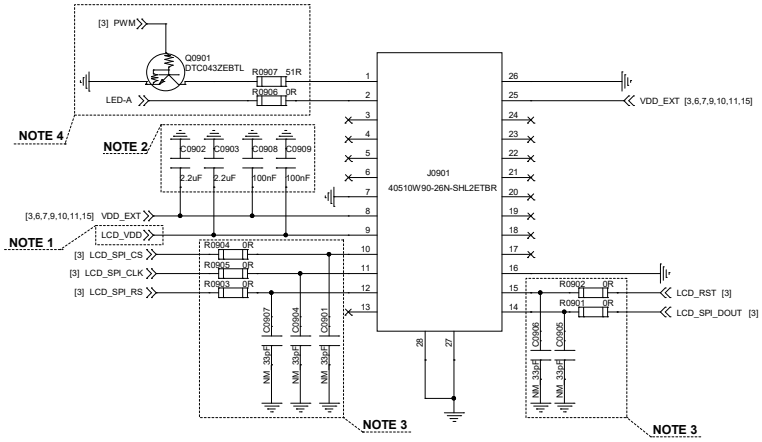
Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 7 OF 15	

Matrix Keypad Design



Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 8 OF 15	

LCM Interface Design



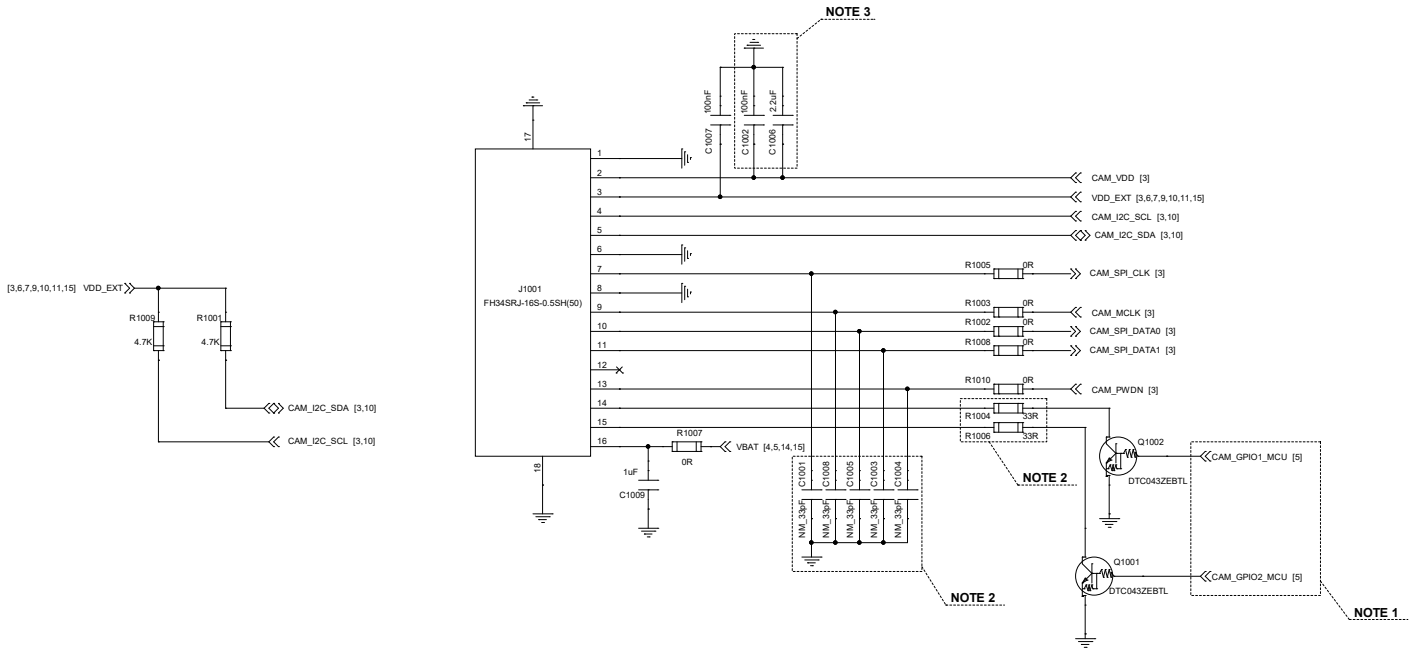
NOTE:

1. It is recommended to design LCM power supply by yourself.
2. To avoid abnormal LCD display caused by power fluctuation, it is recommended to mount filter capacitors.
3. Reserve 33 pF capacitors for the signal pins for debugging.
4. The LED-A backlight power supply should be designed by yourself.

   Select an appropriate resistor (R0907) based on the rated current of the digital transistor and the LED-A voltage value.

Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 9 OF 15	

Camera Interface Design



NOTE:

1. To control the cathode of the camera's positioning light, use CAM_GPIO1_MCU with a triode switching circuit.

   Similarly, CAM_GPIO2_MCU controls the cathode of the camera's supplement light.

   It is recommended to choose GPIO pins that are in a pull-down state by default as these two control pins.

2. Reserve 33 pF capacitors for the signal pins and use them for debugging.

   The values of current limiting resistors (R1004 and R1006) for the positioning light and supplement light should be adjusted based on the desired brightness level.

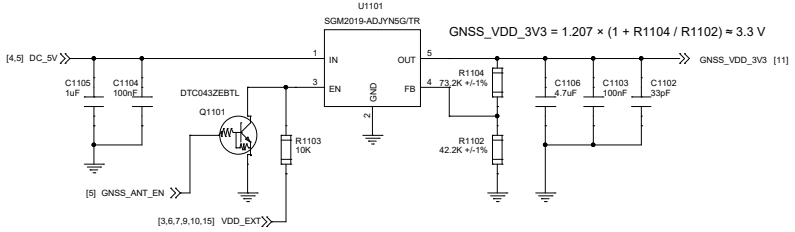
3. Connect the capacitors (C1002 and C1006) of the CAM_VDD power supply directly to the GND layer.

   Failure to do so may result in power supply noise causing abnormalities such as white dots on the preview screen.

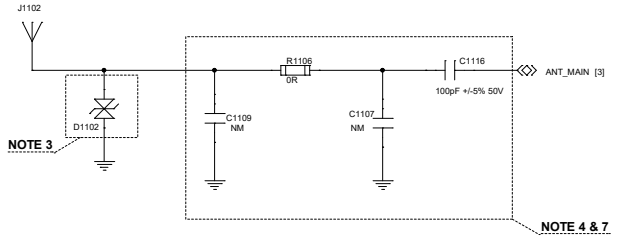
Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 10OF 15	

Antenna Interface Design

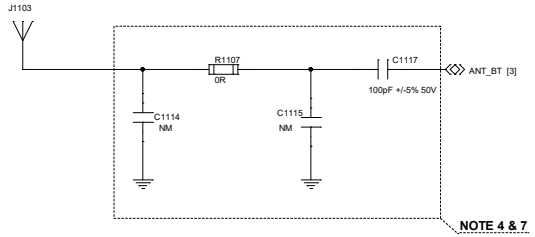
GNSS Active Antenna Power Supply



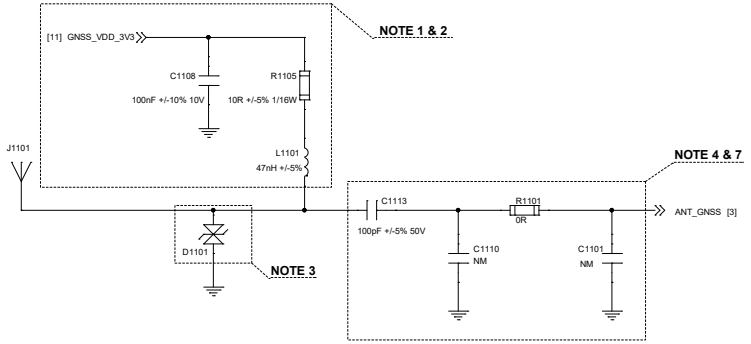
LTE/Wi-Fi Scan Antenna



Bluetooth Antenna



GNSS Antenna



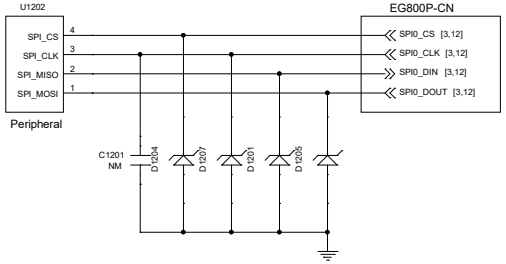
NOTE:

1. For active antennas, select an external LDO according to the active antenna types. In case of passive antennas, the VDD circuit is not necessary.
2. L1101, R1105, C1108 are recommended to be placed close to the RF traces during layout.
3. It is recommended to reserve an ESD protection component for the antenna interface and the junction capacitance should not exceed 0.05 pF.
4. Reserve a dual L-type matching circuit at antenna interfaces.
5. The single-ended impedance of the RF antenna is 50 Ω, and the trace length should be minimized.
6. The external active antenna power supply voltage range is 2.8 V to 4.3 V, with a typical value of 3.3 V.
   The power supply voltage can be designed according to the power supply requirements of the selected active antenna.
7. If there is DC power at the antenna ports, C1113, C1116 and C1117 must be used for DC-blocking to prevent short circuit to ground.
   The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements.
   If there is no DC power in the peripheral design, DC-blocking capacitors are not needed.

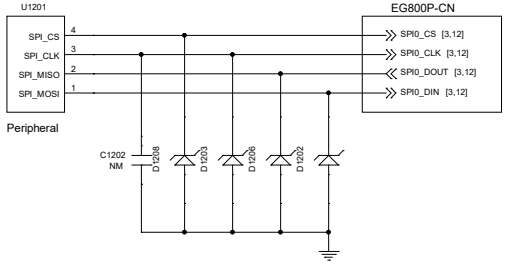
Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 11OF 15	

SPI Design

Module As Master



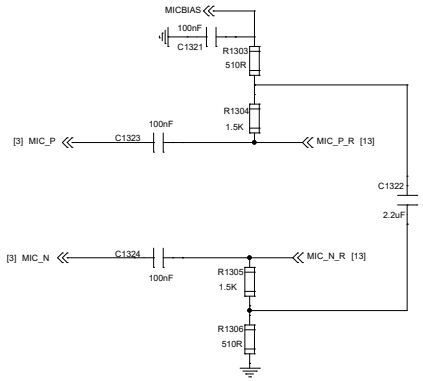
Module As Slave



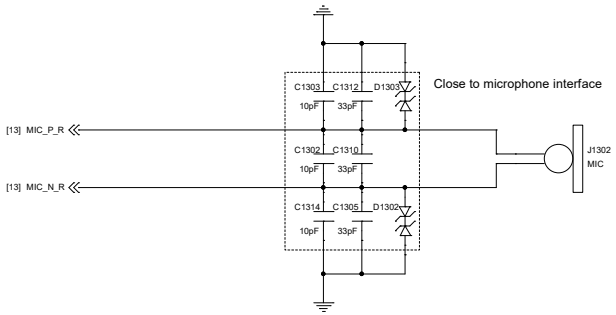
Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 12OF 15	

Analog Audio Design

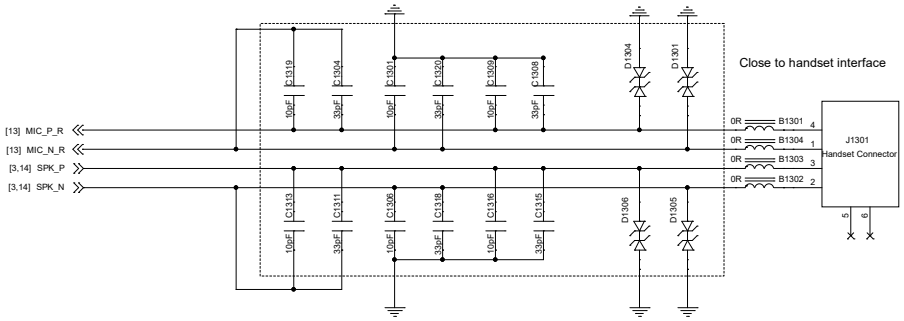
Microphone Bias Circuit



Microphone Application



Handset Application

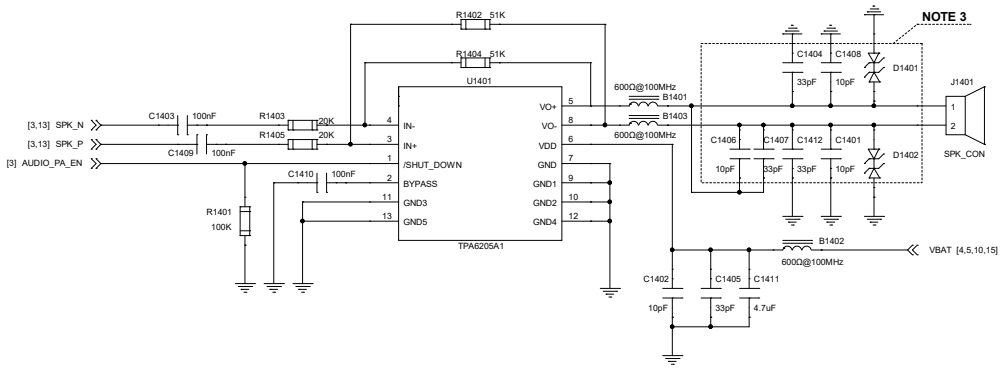


NOTE:

1. The analog audio input interface requires an external microphone bias circuit. MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO.
2. Both the MIC and SPK signal traces need to be routed as differential pairs.
3. Surround all MIC and SPK signal traces with ground on the same layer and with ground planes above and below to minimize noise interference.
4. In the audio design, you can choose either the analog audio or the codec.
5. It is recommended to use 10 pF and 33 pF capacitors to filter RF interference.

Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 13OF 15	

Analog Audio Design (Audio Power Amplifier)

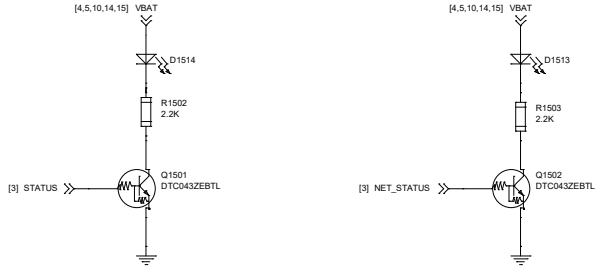


NOTE:

1. SPK_P and SPK_N channels are differential output channels intended for connecting to an external audio power amplifier.
   To eliminate Pop noise, it is recommended to utilize MAIN_DCD of the module as the control signal for the audio power amplifier's enable pin.
   For more information about AUDIO_PA_EN, contact Quectel Technical Support.
2. The power amplifier in this design is for reference only. Select the appropriate audio power amplifier according to actual needs.
3. When designing the layout, ensure that filter capacitors and ESD protection components are placed close to the loudspeaker to filter out interference and provide adequate protection.
4. The selection of ESD protection components should consider the output voltage range of the audio power amplifier. Ensure that the output voltage of the amplifier remains within the maximum reverse working voltage range of the selected ESD protection components under normal operating conditions.
   This precaution helps prevent damage to the ESD protection components.

Other Designs

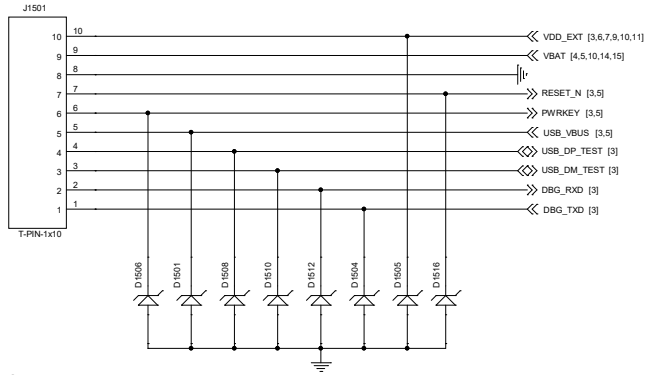
Indicators



NOTE:

1. For more details about STATUS and NET_STATUS, see the hardware design document of the module.
2. To minimize the module's power consumption during the sleep mode of your device, replace the power supply (VBAT) of the STATUS and NET_STATUS indicators with externally controllable sources and turn off the indicators when the module is in sleep mode.

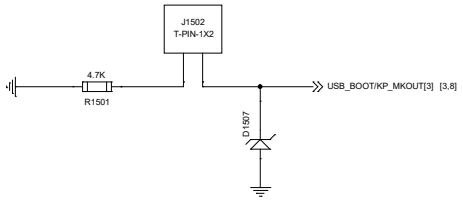
Reserved Test Points



NOTE:

1. Test points for both USB and debug UART interfaces are reserved for capturing logs.
2. Test points for USB interface can also be reserved for firmware upgrade.
3. The junction capacitance of the ESD protection components on USB data traces should be less than 2 pF.
4. The debug UART interface supports a 1.8 V power domain. If your application operates at 3.3 V, use a voltage-level translator.

USB_BOOT Interface



NOTE:

1. Make sure to reserve the USB_BOOT interface design and it is recommended to reserve a test point for USB_BOOT/KP_MKOUT[3].
2. Before turning on the module, pull USB_BOOT/KP_MKOUT[3] down to GND to activate the forced download mode. This mode enables firmware upgrades via the USB interface.
3. The 6.0 and above version of QFlash tool must be used for firmware upgrading.

Quectel Wireless Solutions		
PROJECT: EG800P-CN QuecOpen		VER: 1.0
DRAWN BY: Mark YANG/Janko LI	CHECKED BY: Tik HUANG/Shawn HU	SIZE: A2
DATE: Monday, June 03, 2024	SHEET: 15OF 15	