EG915U Series QuecOpen Reference Design

LTE Standard Module Series

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Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2022-06-30	Len CHEN	Creation of the document
1.0	2023-09-26	Phoebe FU/ Woping WANG	First official release

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EG915U series module in QuecOpen® solution, including block diagrams of module design, power supply, antenna, (U)SIM, analog audio, UART, camera, LCM, external flash and SD card interfaces.

1.2. Special Mark

Table 1: Special Mark

Mark	Definition
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO_DATA pins, SDIO_DATA0, SDIO_DATA1, SDIO_DATA2 and SDIO_DATA3.

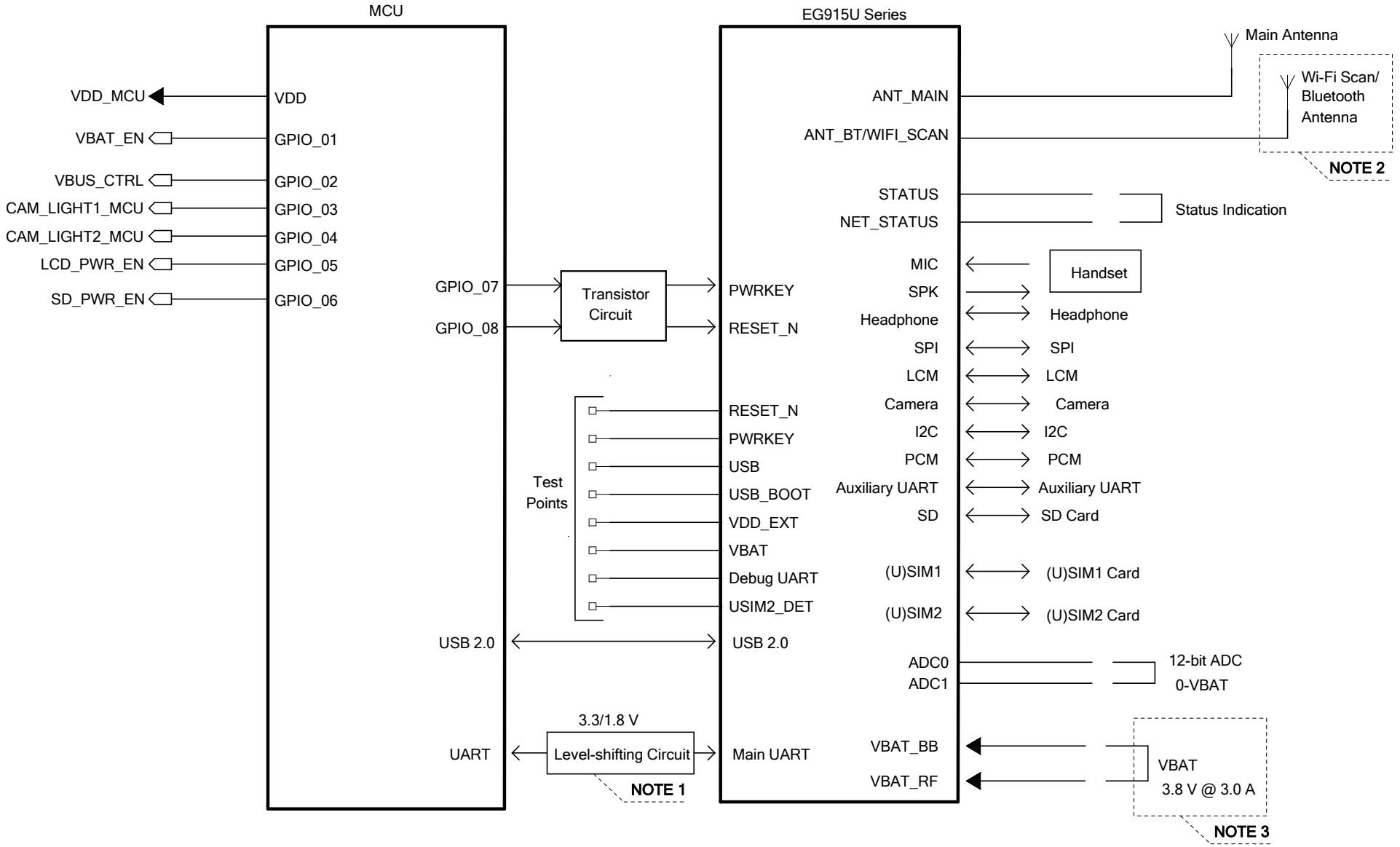
1.3. Schematics

The schematics illustrated in the following pages are provided for your reference only.

NOTE

It is required to confirm the applicability and price from the supplier about the IC involved in the reference design.

Block Diagram



NOTE:

1. A transistor circuit or a voltage-level translator TXS0104EPWR provided by Texas Instruments is recommended.
2. The module supports both Wi-Fi Scan and Bluetooth functions. However, as the antenna interface is shared, the two functions cannot be used simultaneously. For details about specific models, contact Quectel Technical Support.
3. The power supply should be able to provide sufficient current of at least 3.0 A for the module.

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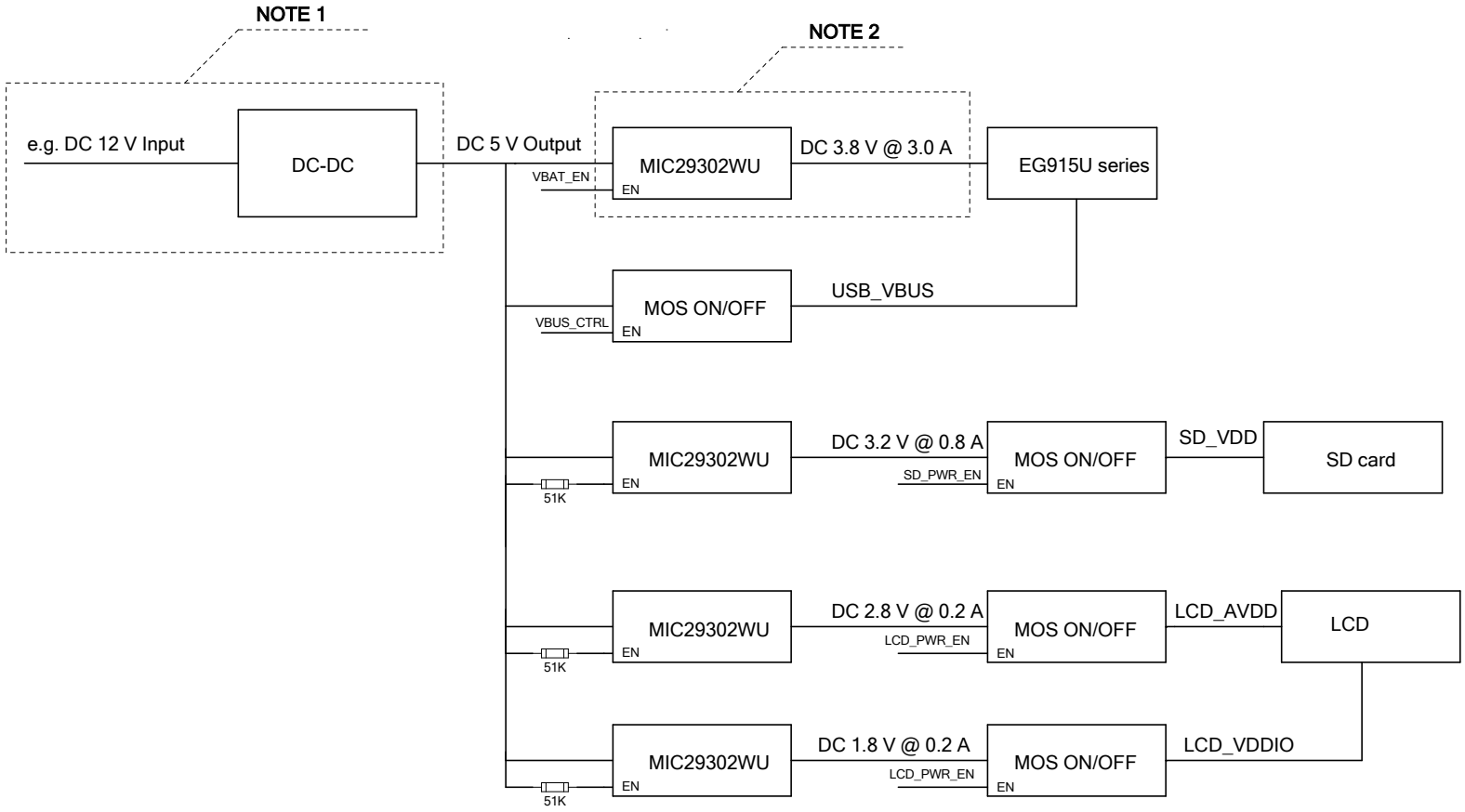
Power System Block Diagram



NOTE:

1. When the input voltage is above 7.0 V, use a DC-DC converter to convert a high input voltage into 5.0 V.
2. The LDO is used to convert the input voltage into 3.8 V typical voltage and the power supply should provide at least 3 A current for the module.

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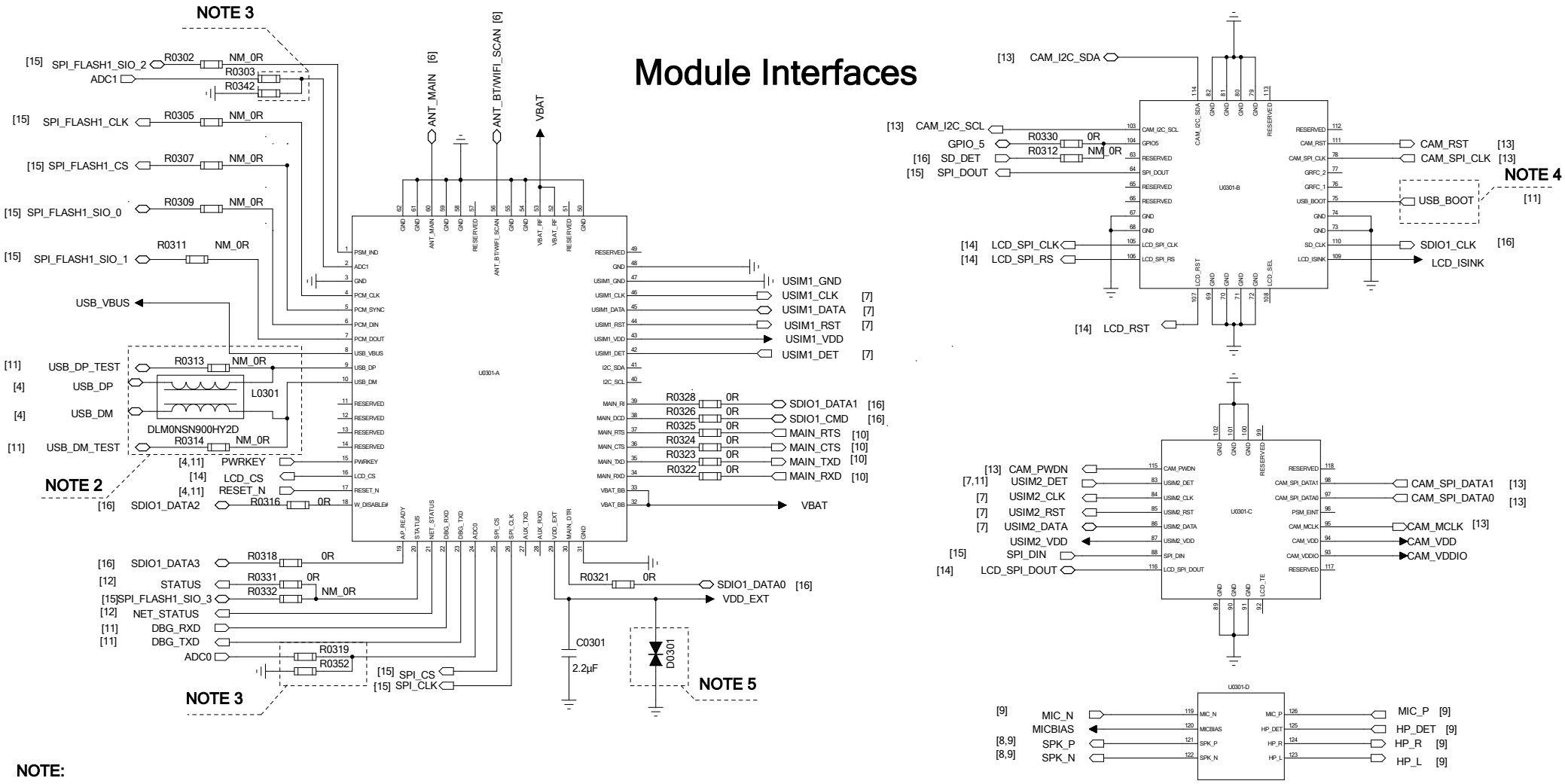
Module Interfaces



NOTE:

1. Keep unused and RESERVED pins open, and all GND pins are connected to the ground.
2. A common mode choke L0301 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission.
   Meanwhile, reserve test points for upgrading the firmware and debugging software over USB interface and minimize the extra stubs of the trace.
   L0301 and the two resistors R0313 and R0314 should be placed close to the module to ensure the integrity of USB signal.
3. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins,
   it is strongly recommended to reserve the voltage divider circuit for better compatibility with other Quectel modules.
   The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced.
   When the divider circuit is not used, the ADC pins require 1 kΩ resistor in series.
4. When emergency download function is not required, USB_BOOT cannot be pulled up before the module starts up.
5. The maximum reverse working voltage of the ESD protection components on VDD_EXT traces should not exceed 5 V.
6. Test points must be reserved for DBG_TXD, DBG_RXD, USB_DP, USB_DM, USB_VBUS and USIM2_DET.
   It is recommended to reserve test points for USB_BOOT, VDD_EXT, VBAT and PWRKEY.
   It is recommended to reserve a test point for RESET_N if it is unused.

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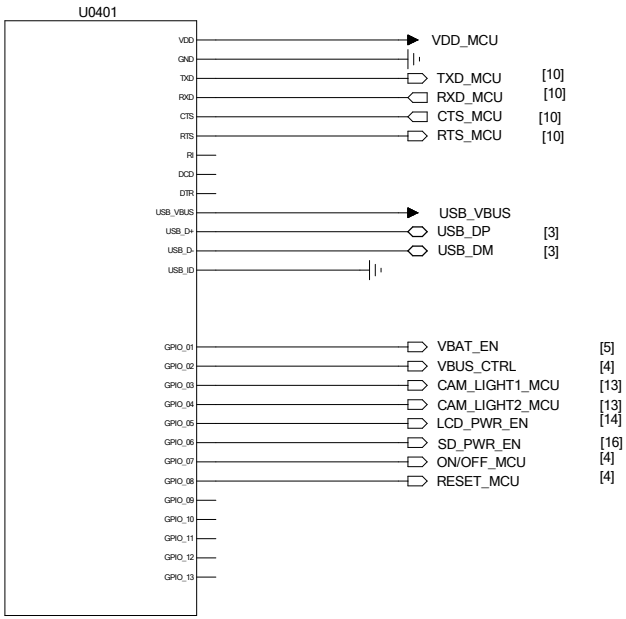
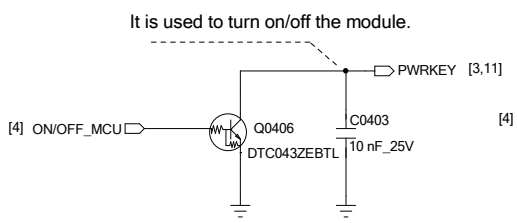
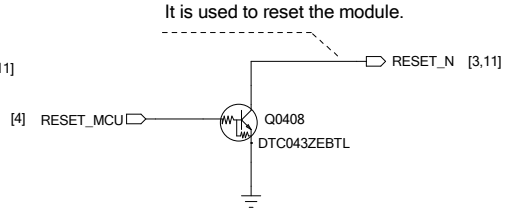
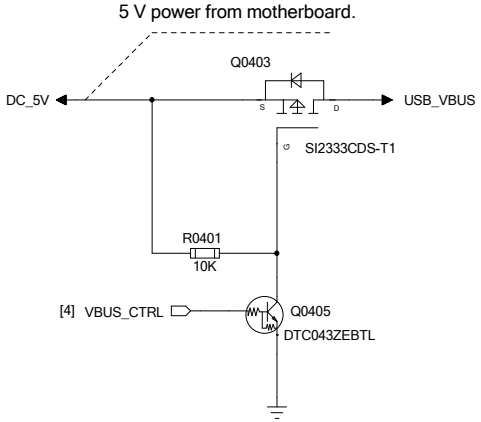
MCU Interfaces









NOTE:

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V;
   if the GPIO interfaces of U0401 share the same power domain, then the related level-shifting circuit is not required.
2. The USB 2.0 interface of the module only serves as a slave device and supports high-speed and full-speed modes.
   To communicate with the USB interface, MCU needs to support USB host mode or OTG function. The USB_VBUS of the module and MCU should be powered by an external power system, and USB_VBUS is for USB detection. VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the default low-level GPIO pins of MCU as the control pins for PWRKEY and RESET_N of the module.
   Ensure that the maximum load capacitance of PWRKEY and RESET_N does not exceed 10 nF.

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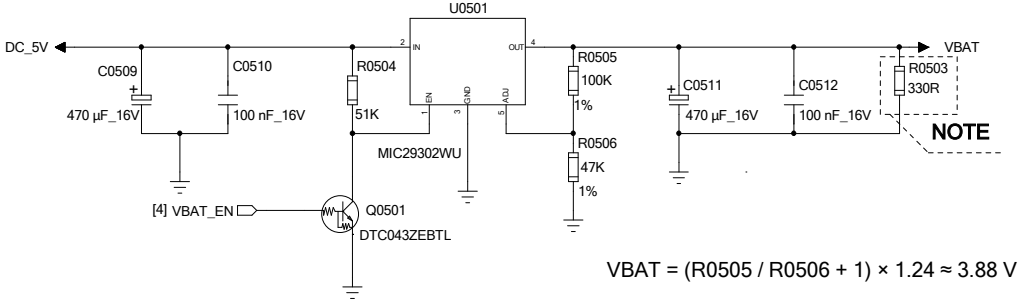
Power Supply Design

LDO Application

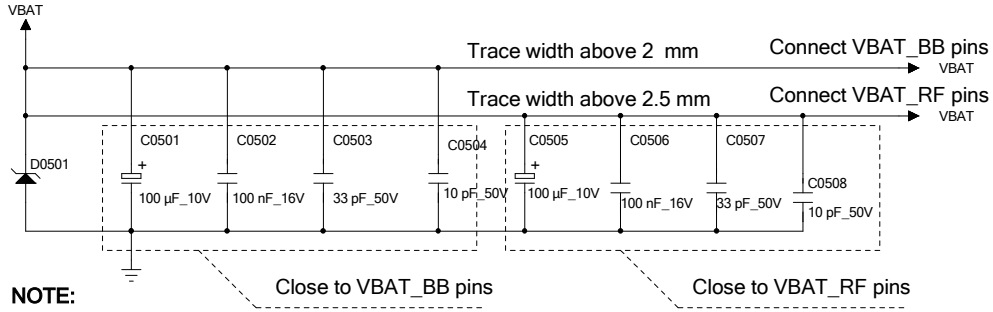
When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



VBAT = (R0505 / R0506 + 1) × 1.24 ≈ 3.88 V

NOTE: The recommended load current is greater than 10 mA.

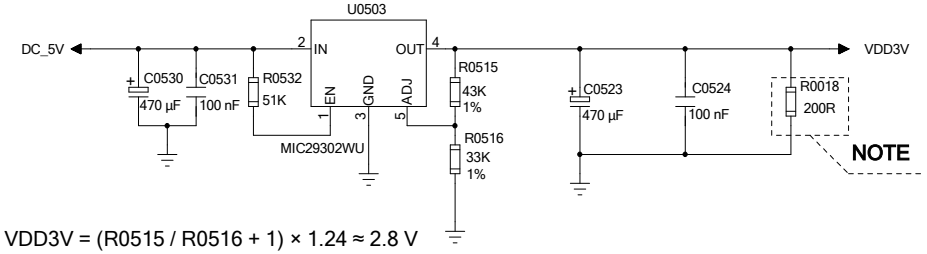
VBAT Design



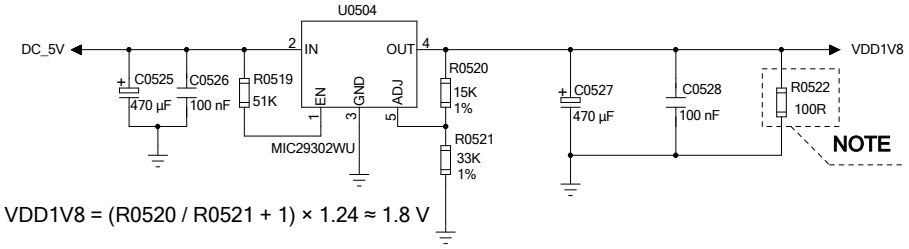
NOTE:

1. For more information about power supply of module, see the hardware design document of the module.
2. The VBAT traces must be connected to pins VBAT_BB and VBAT_RF in a star configuration.
3. The recommended operating voltage of VBAT is 3.3 V-4.3 V, and the typical value is 3.8 V.

LCD Power Supply



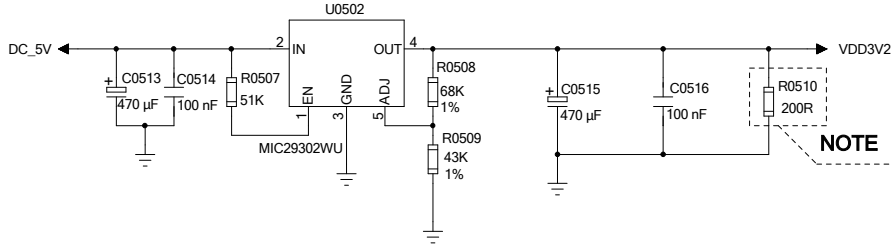
VDD3V = (R0515 / R0516 + 1) × 1.24 ≈ 2.8 V



VDD1V8 = (R0520 / R0521 + 1) × 1.24 ≈ 1.8 V

NOTE: The recommended load current is greater than 10 mA.

SD Card Power Supply



VDD3V2 = (R0508 / R0509 + 1) × 1.24 ≈ 3.2 V

NOTE: The recommended load current is greater than 10 mA.

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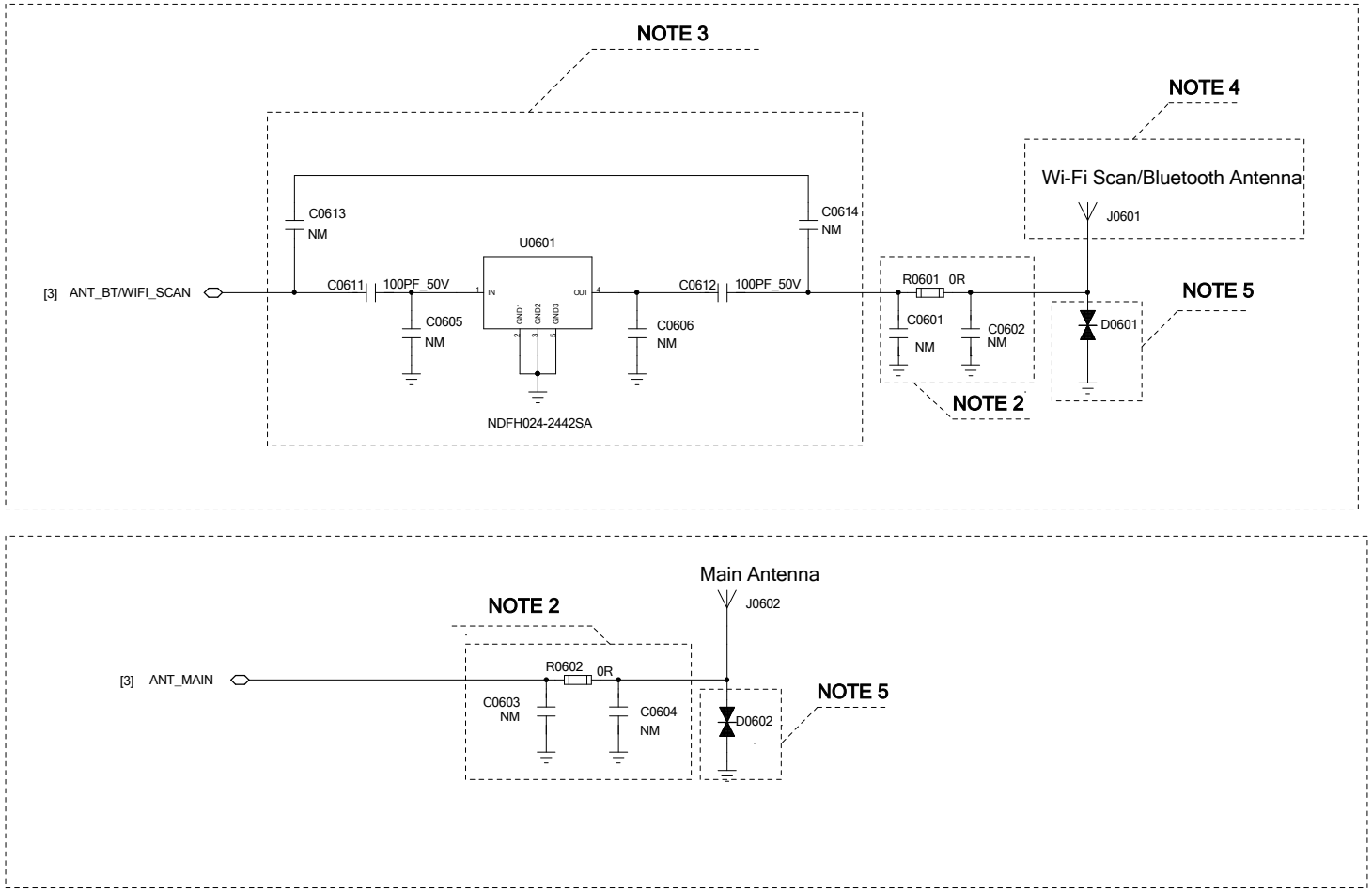
Antenna Interface Design



NOTE:

1. The single-ended impedance of the RF antenna is 50 Ω.
2. It is highly recommended to reserve a Π-type matching circuit for future debugging.
3. For EG915U-CN, you can select C0613 and C0614 in the compatible design, and C0605, C0606, C0611, C0612, U0601 are not mounted by default.
   For EG915U-EU/-LA/-EC, you can select C0605, C0606, C0611, C0612 and U0601 in the compatible design, and C0613 and C0614 are not mounted by default.
4. The module supports both Wi-Fi Scan and Bluetooth functions. However, as the antenna interface is shared, the two functions cannot be used simultaneously.
   Additionally, Bluetooth and Wi-Fi Scan functions are optional. For details, contact Quectel Technical Support.
5. It is recommended that the junction capacitance and peak reverse working voltage of the ESD protection components should not exceed 0.05 pF and 5 V respectively.

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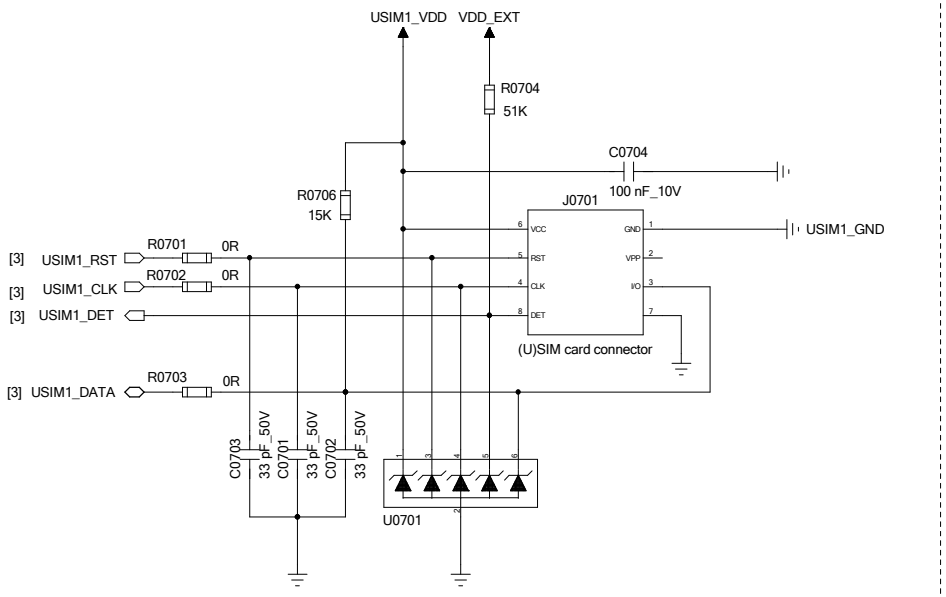
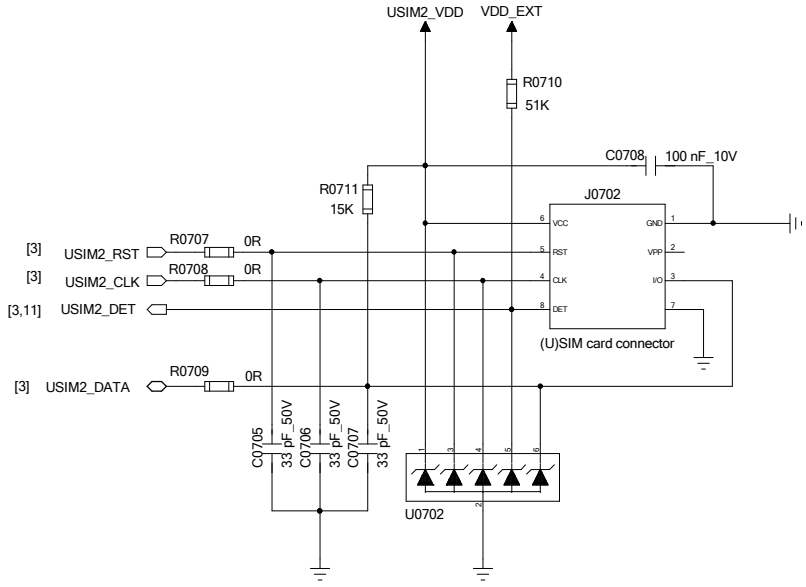
(U)SIM Interface Design

(U)SIM 1



(U)SIM 2



NOTE:

1. U0701 and U0702 are recommended to be used to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.
2. The pull-up resistor R0706 & R0711 can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.
3. R0701-R0703 and R0707-R0709 are used for debugging, and C0701-C0703 and C0705-C0707 are used for filtering out RF interference.
4. C0704 and C0708's capacitance should not exceed 1 μF and they should be placed close to the (U)SIM card connector.
5. The GND of the (U)SIM card connector is recommended to be connected to the GND layer directly.
6. The module supports (U)SIM card hot-plug via the USIM_DET pin and both high-level and low-level detections are supported. The function is disabled by default.
7. For more information about the layout of (U)SIM interface, see the hardware design document of the module.

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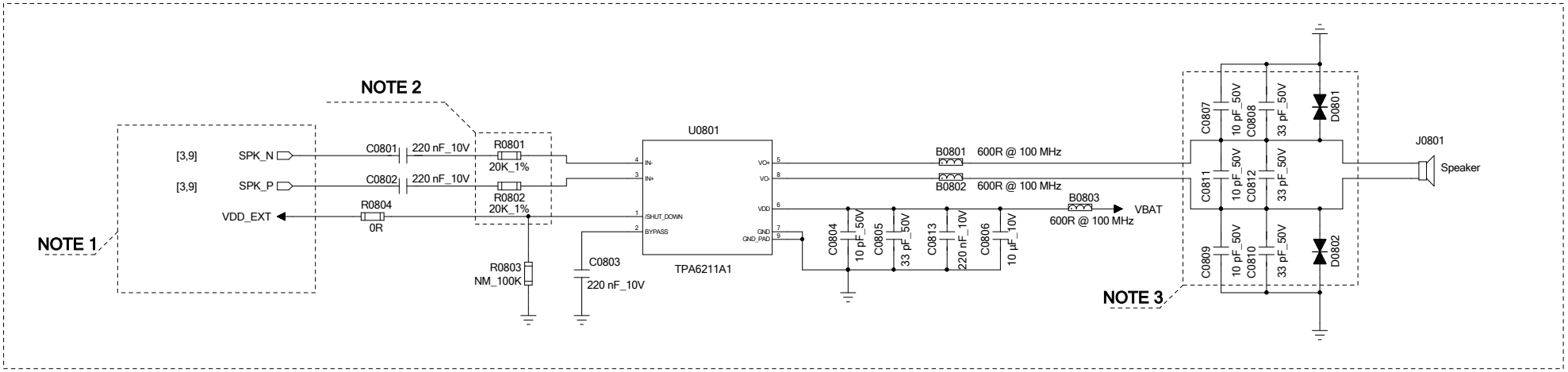
Analog Audio Design (External Audio Amplifier)



NOTE:

1. SPK_N and SPK_P are differential output channels that can connect an audio PA. When the channels are turned on or off, it is possible for the module to emit a pop sound, which can be eliminated by controlling the enable pin of the audio PA. For details, please contact Quectel Technical Support.
2. Choose the audio power amplifier with appropriate power according to the actual needs. Audio PA Gain = 40 kΩ / R0801 or R0802.
3. Place filter capacitors and ESD protection components close to the loudspeaker and the selection of ESD protection components is related to the selection of audio power amplifiers. Ensure that the output voltage of the audio power amplifier is within the maximum reverse working voltage range of the ESD protection components.

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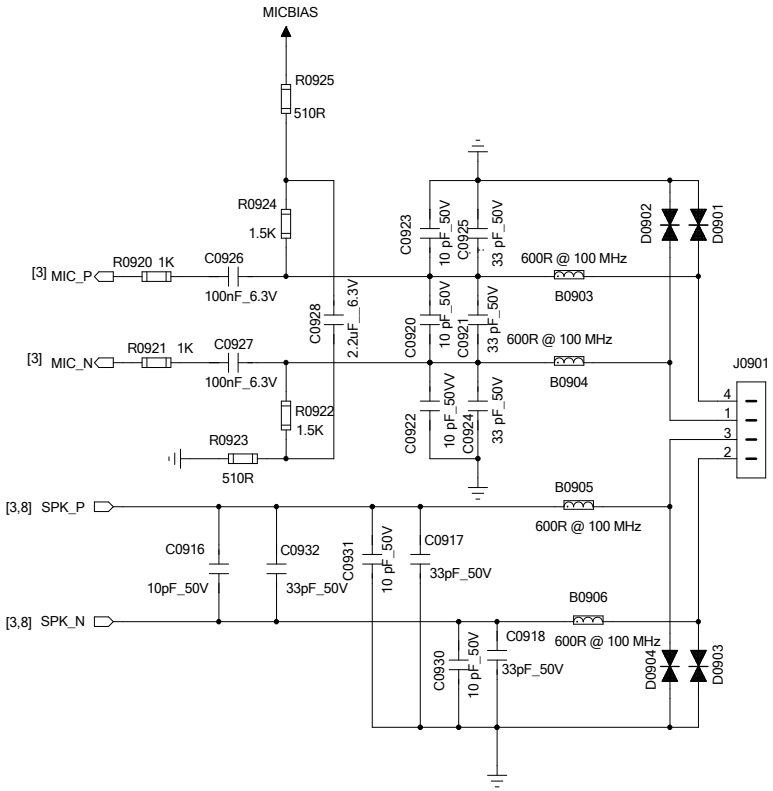
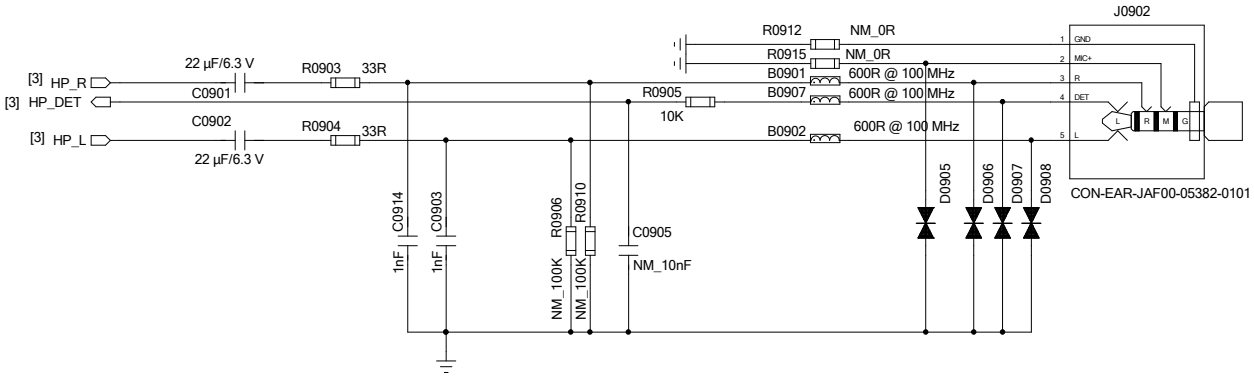
Analog Audio Interface Design

Handset (Microphone and Earpiece)



Headphone



Compatible Design

	CTIA	OMTP
R0912	NM	M
R0915	M	NM

Headphone Insertion Detection Mechanism

	Pins 4 and 5
Plug in	Connected
Plug out	Disconnected

Headphone type	Line sequence
OMTP	L, R, MIC+, GND
CTIA	L, R, GND, MIC+

NOTE:

1. Both the MIC and SPK signal traces need to be routed as differential pairs.
2. All MIC and SPK signal traces should be surrounded with ground on the layer and with ground planes above and below, and far away from noise sources.
3. ESD protection components should be placed as close to the audio interfaces as possible and ensure that the audio voltage is within the maximum reverse working voltage range of the ESD protection components.

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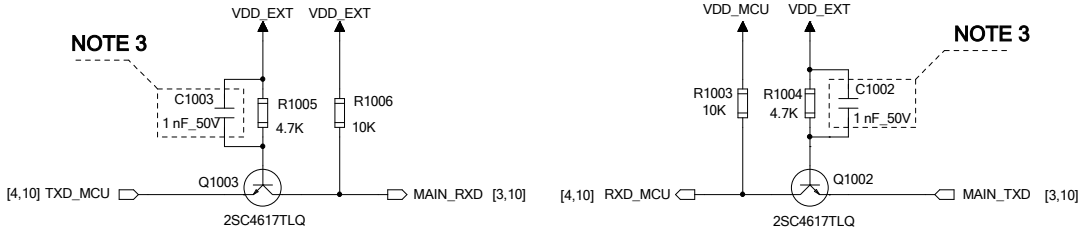
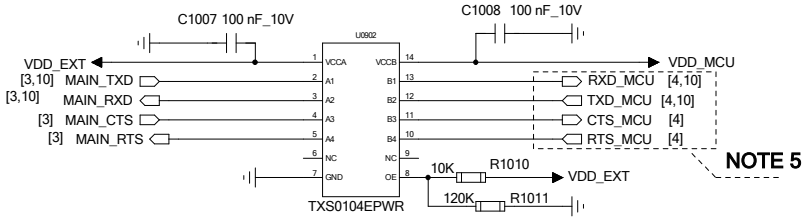
UART Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter.
2. The power supply of TXS0104EPWR's VCCA should not exceed that of VCCB. For more information, see the datasheet of TXS0104EPWR.
3. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C1002 and C1003 of 1 nF can improve the signal quality.
4. The MAIN_RTS level-shifting circuit is similar to that of the MAIN_RXD.
   The MAIN_CTS level-shifting circuit is similar to that of the MAIN_TXD.
5. The module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS. In addition, pay attention to the direction of connection.
   The TXD and RXD of the module are respectively connected to the RXD and TXD of the MCU.

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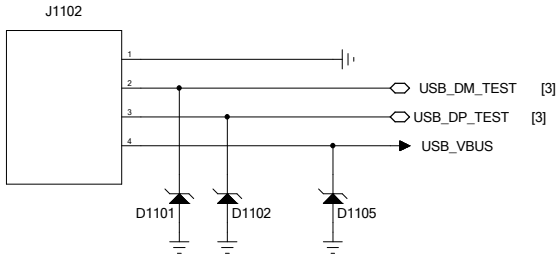
Test Points

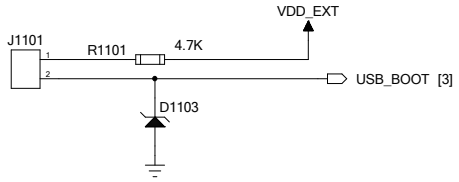
USB Interface Test Points



NOTE:

1. Test points must be reserved for USB interface to debug software.
2. The module can upgrade the firmware over USB interface.
3. The parasitic capacitance of the ESD protection components on USB data traces should not exceed 2 pF. Ensure that the signal voltage is within the maximum reverse working voltage range of the ESD protection components.

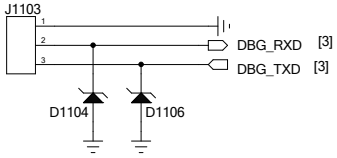
USB_BOOT Interface Test Points



NOTE:

1. It is recommended to reserve a test point for USB_BOOT interface.
2. Pull up the USB_BOOT to VDD_EXT before the module starts up, and the module will enter emergency download mode after powering up. In this mode, the module supports firmware upgrade over USB interface.

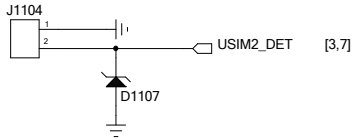
Debug UART Test Points



NOTE:

1. Test points must be reserved for DBG_TXD and DBG_RXD for debugging.
2. The debug UART interface supports 1.8 V power domain, and a level-shifting circuit should be used if the power domain of your application is 3.3 V. For details, refer to "UART Interface Design" sheet.
3. The debug UART only supports the baud rate of 921600 bps.

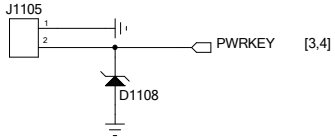
USIM2_DET Test Point



NOTE:

1. A test point must be reserved to capture CP logs.
2. The USIM2_DET test point supports 1.8 V power domain.
3. When capturing the CP log, set the baud rate to 8000000 bps.

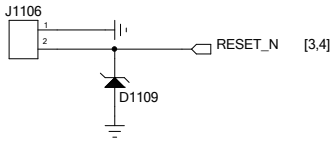
PWRKEY Test Point



NOTE:

It is recommended to reserve a test point for PWRKEY.

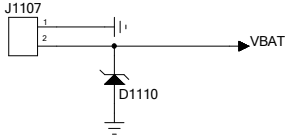
RESET_N Test Point



NOTE:

It is recommended to reserve a test point for RESET_N if it is unused.

VBAT Test Point



NOTE:

It is recommended to reserve a test point for VBAT.

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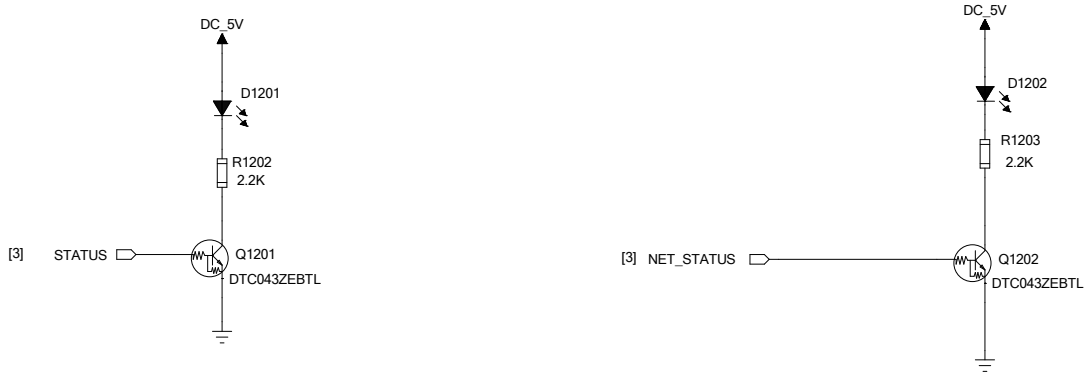
Indicator Designs



NOTE:

1. For more details about STATUS and NET_STATUS, see the hardware design document of the module.
2. If the low power consumption is required when your device is in sleep status, replace the power supply DC_5V of the STATUS and NET_STATUS indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

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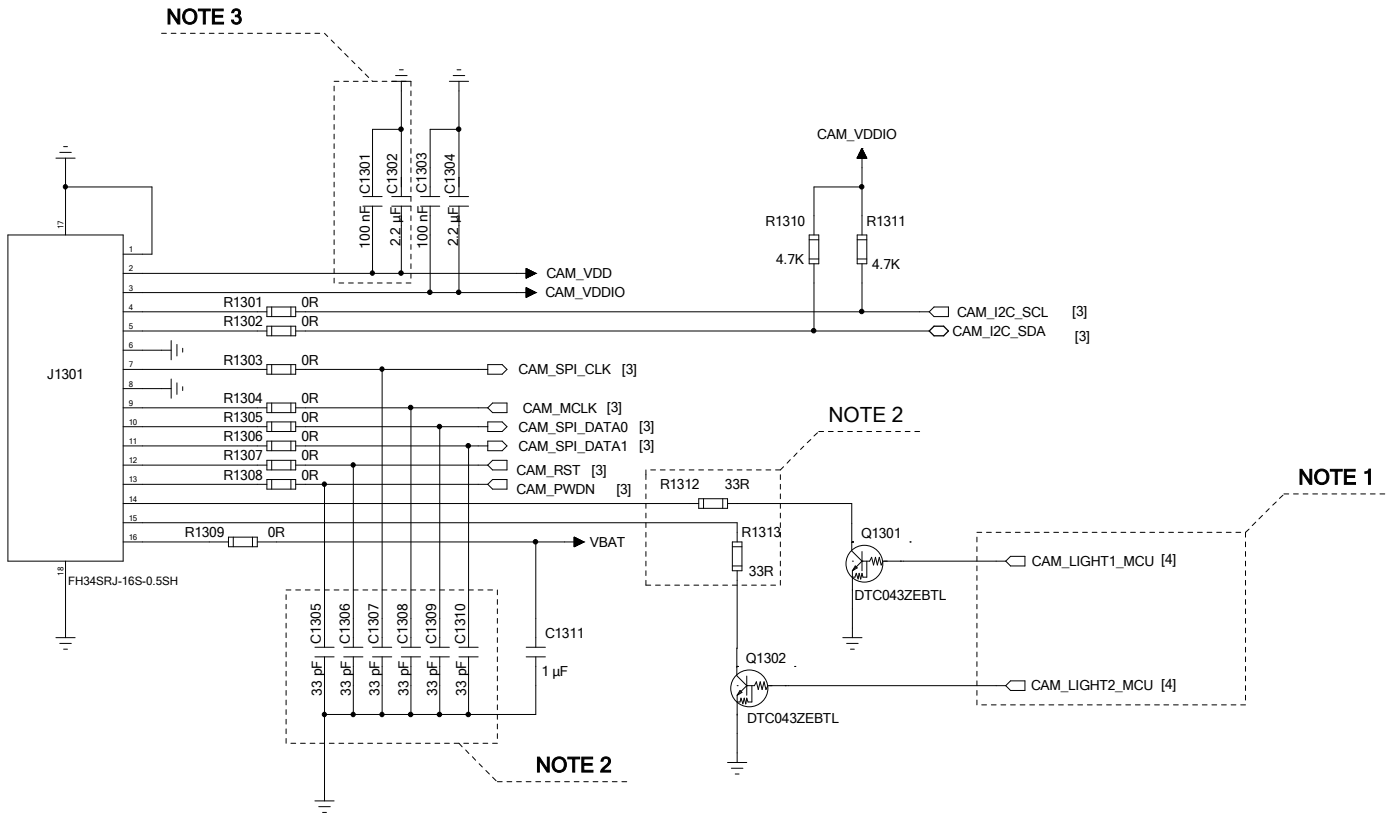
Camera Interface Design



NOTE:

1. CAM_LIGHT1_MCU controls the cathode of the position light of the camera by controlling the triode switching circuit;
   CAM_LIGHT2_MCU controls the cathode of the supplement light of the camera by controlling the triode switching circuit;
   Choose GPIO pins with default pull-down status as CAM_LIGHT1_MCU and CAM_LIGHT2_MCU.
2. The 33 pF capacitors of the signal pins are reserved, and they can be used according to the actual debugging situation.
   The values of current limiting resistors of position light and supplement light (R1312 and R1313) should be varied according to desired brightness level.
3. The capacitors of the CAM_VDD power supply should be connected to the GND layer directly, otherwise there may be power noise leading to abnormalities such as white dots on the preview screen.

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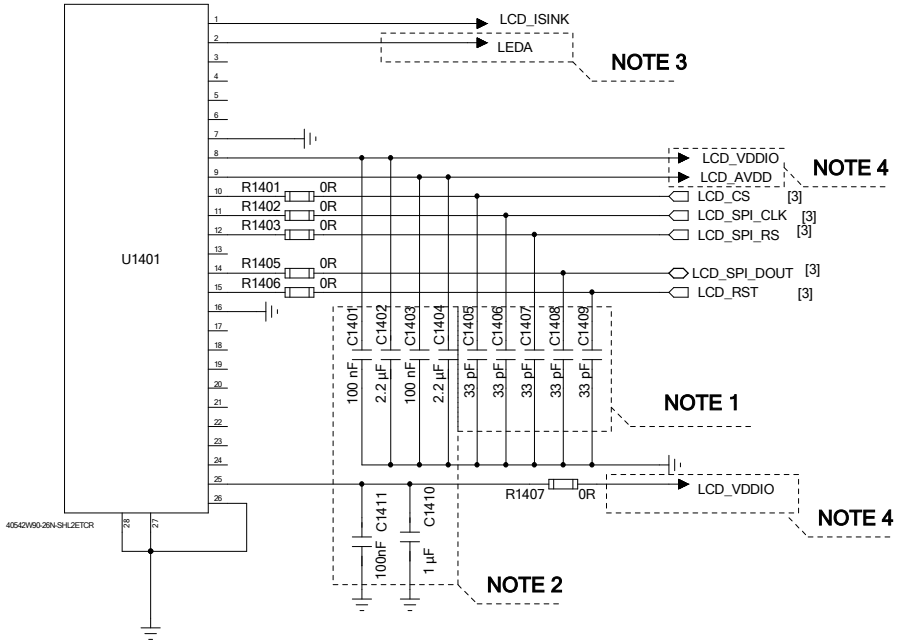
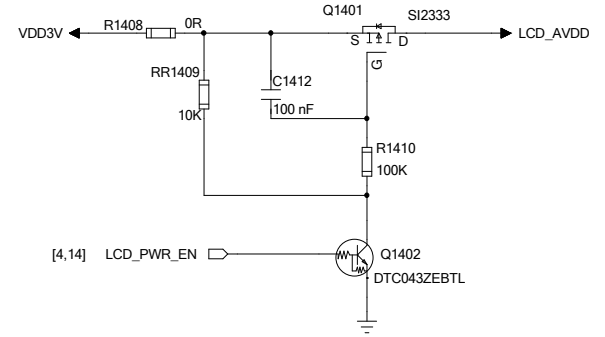
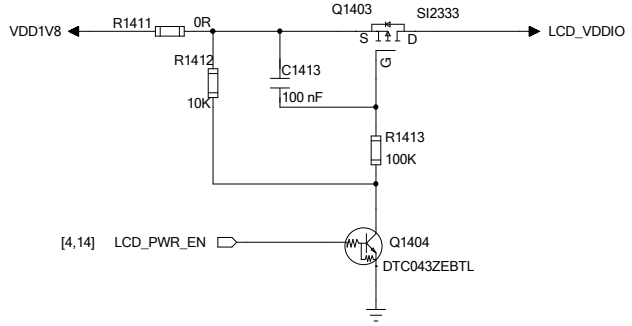
LCM Interface Design







NOTE:

1. The 33 pF capacitors of the signal pins are reserved, and can be used as per the actual debugging situation.
2. To avoid abnormal LCD display caused by power fluctuation, the filter capacitors of LCD_AVDD and LCD_VDDIO must be mounted.
3. The power supply pin LEDA of the backlight is provided by an external power supply circuit, and you can design the circuit by yourself.
4. The LCD analog power supply LCD_AVDD and digital power supply LCD_VDDIO are externally provided.
   The nominal voltage of LCD_VDDIO is 1.8 V and the nominal voltage of LCD_AVDD is 2.8 V.

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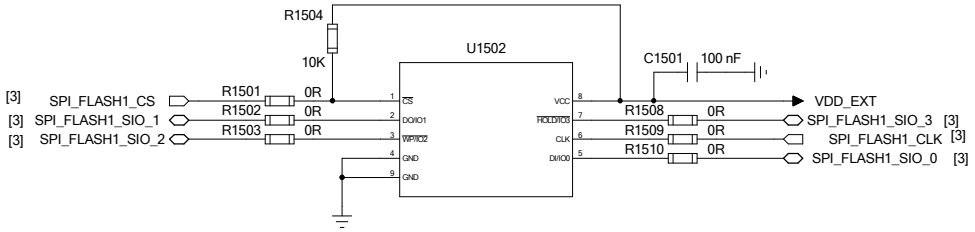
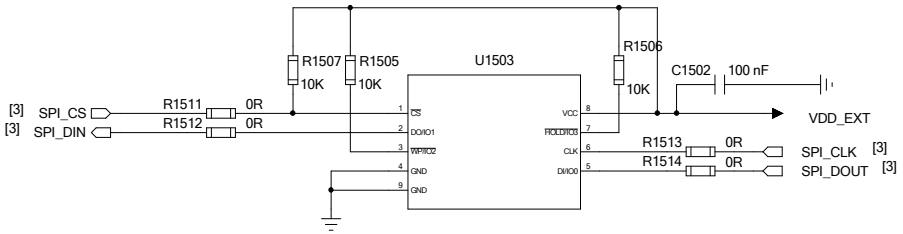
External Flash Interface Design

Six-wire NOR Flash Circuit Design



Four-wire NOR Flash Circuit Design



NOTE:

1. The filter capacitors C1501 and C1502 need to be placed close to the power pins of the flash chip to achieve the expected filtering effect.
2. For the four-wire NOR flash circuit, it is recommended that the WP and HOLD pins be connected with pull-up resistors, so as to avoid abnormal levels to damage the flash chip, resulting in abnormal transmission or data loss.
3. The SPI of the module only supports master mode, that is, the module can only be a host when communicating with the peripherals through the SPI.
4. There are two design schemes for the flash circuit of the module to be selected according to the design requirements.

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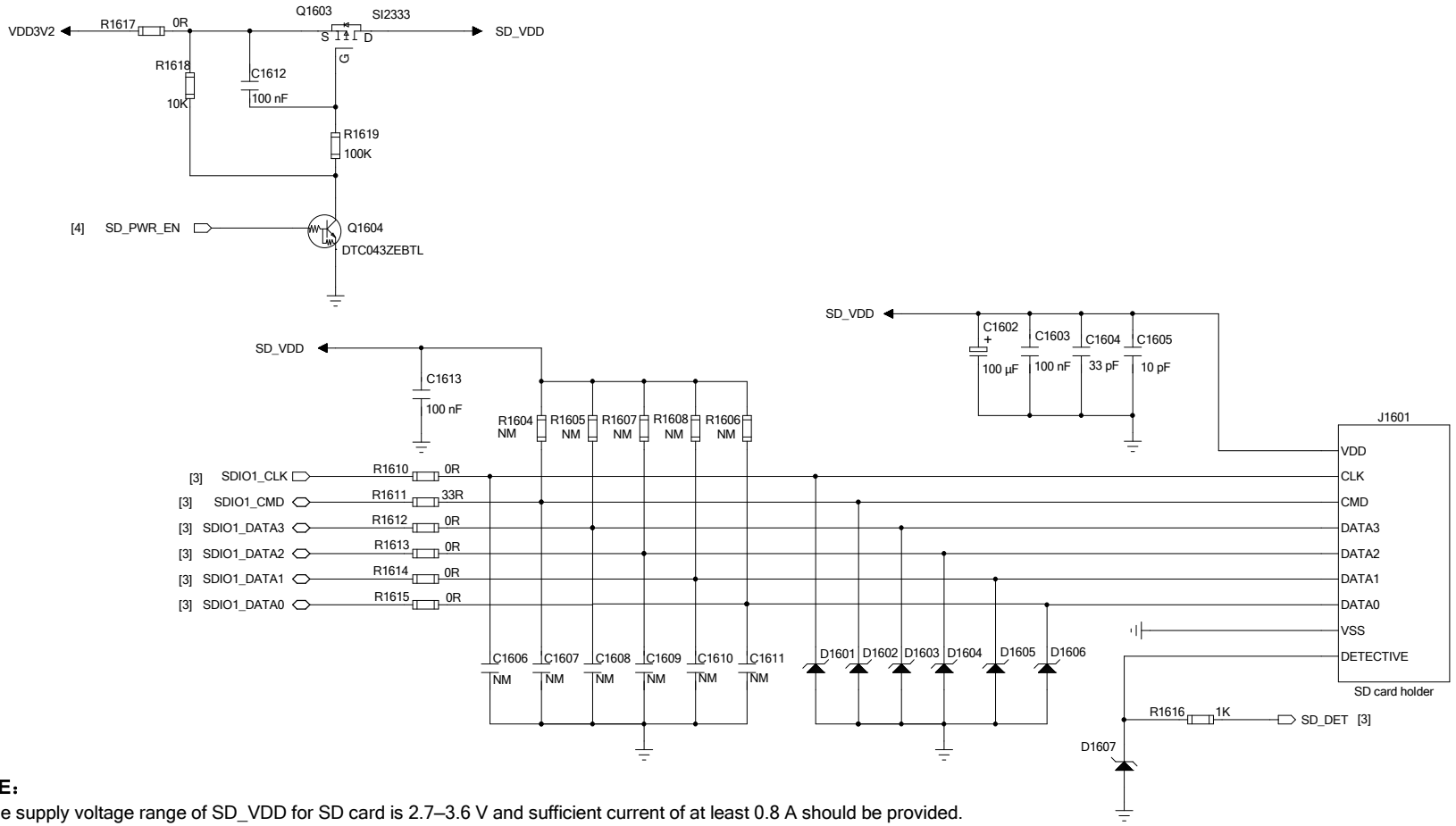
SD Card Interface Design



NOTE:

1. The supply voltage range of SD_VDD for SD card is 2.7–3.6 V and sufficient current of at least 0.8 A should be provided.
2. To avoid the jitter of bus, pull-up resistors R1604–R1608 are recommended to be added to SDIO bus. SDIO bus needs to be connected to a pull-up power supply.
   The values of these resistors are among 10–100 kΩ. The recommended value is 4.7 kΩ and the resistors are not mounted by default. The recommended pull-up power supply is 3.2 V.
3. In order to improve the signal quality, it is recommended to add 0 Ω resistors R1610–R1615 in series between the module and the SD card connector.
   The bypass capacitors C1606–C1611 are reserved and not mounted by default.
4. In order to ensure good ESD performance, it is recommended to add a TVS array and place it as close as possible to the SD card connector,
   and ensure that the junction capacitance of the TVS array is less than 15 pF.
5. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock and DC-DC signals.
6. It is important to route the SDIO signal traces with ground surrounded, and the impedance is controlled at 50 Ω ±10 %.
   The traces of SDIO1_CLK, SDIO1_DATA[0:3] and SDIO1_CMD should be equal in length (the difference is less than 1 mm),
   and the total length should be less than 50 mm.
7. The spacing between SDIO signals and other signals needs to be greater than twice the trace width, and ensure that the bus capacitance is less than 15 pF.

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