EG800G Series QuecOpen Reference Design

LTE Standard Module Series

Version: 1.0

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Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2023-08-18	Phoebe FU/ Eric MO	Creation of the document
1.0	2023-11-16	Phoebe FU/ Eric MO	First official release

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EG800G series module in QuecOpen® solution, including block diagrams of module interfaces, power supply, antenna, USIM, UART, audio codec, LCM, camera, SD card interfaces.

1.2. Special Mark

Table 1: Special Mark

Mark	Definition
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA [0:3] refers to all four SDIO_DATA pins, SDIO_DATA0, SDIO_DATA1, SDIO_DATA2 and SDIO_DATA3.

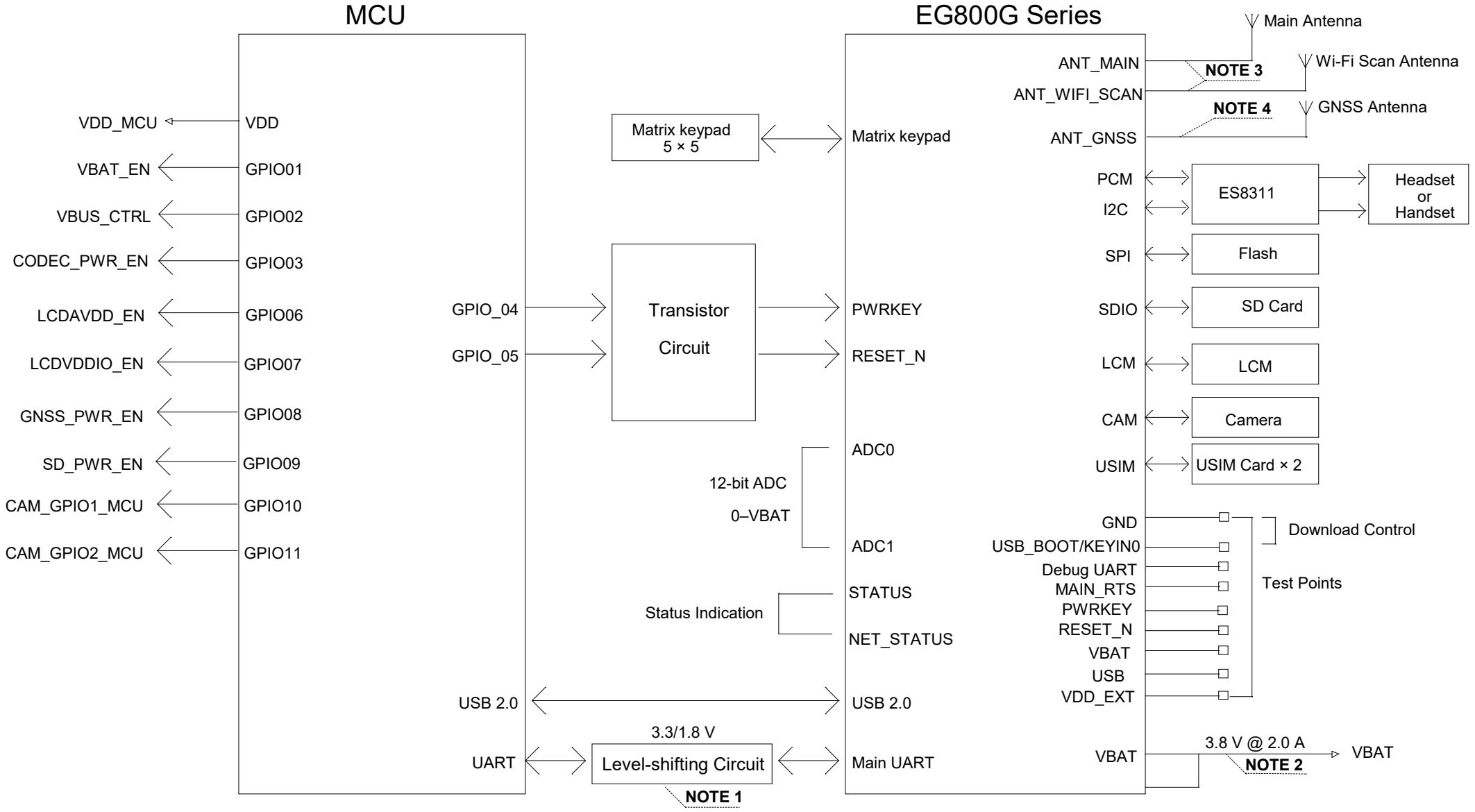
1.3. Schematics

The schematics illustrated in the following pages are provided for your reference only.

NOTE

It is required to confirm the applicability and price from the supplier about the IC involved in the reference design.

Block Diagram



NOTE:

1. A transistor circuit or a voltage-level translator TXS0104EPWR provided by Texas Instruments is recommended.
2. The power supply should be able to provide sufficient current of at least 2.0 A for the module.
3. EG800G-CN supports Wi-Fi scan function, which shares the same antenna interface with main antenna. The two functions cannot be used simultaneously.
   EG800G-EU/-LA provides a dedicated Wi-Fi scan antenna interface (ANT_WIFI_SCAN). Wi-Fi scan supports receiving only.
4. EG800G-CN supports GNSS function and the function is optional. EG800G-EU/-LA does not support GNSS function.

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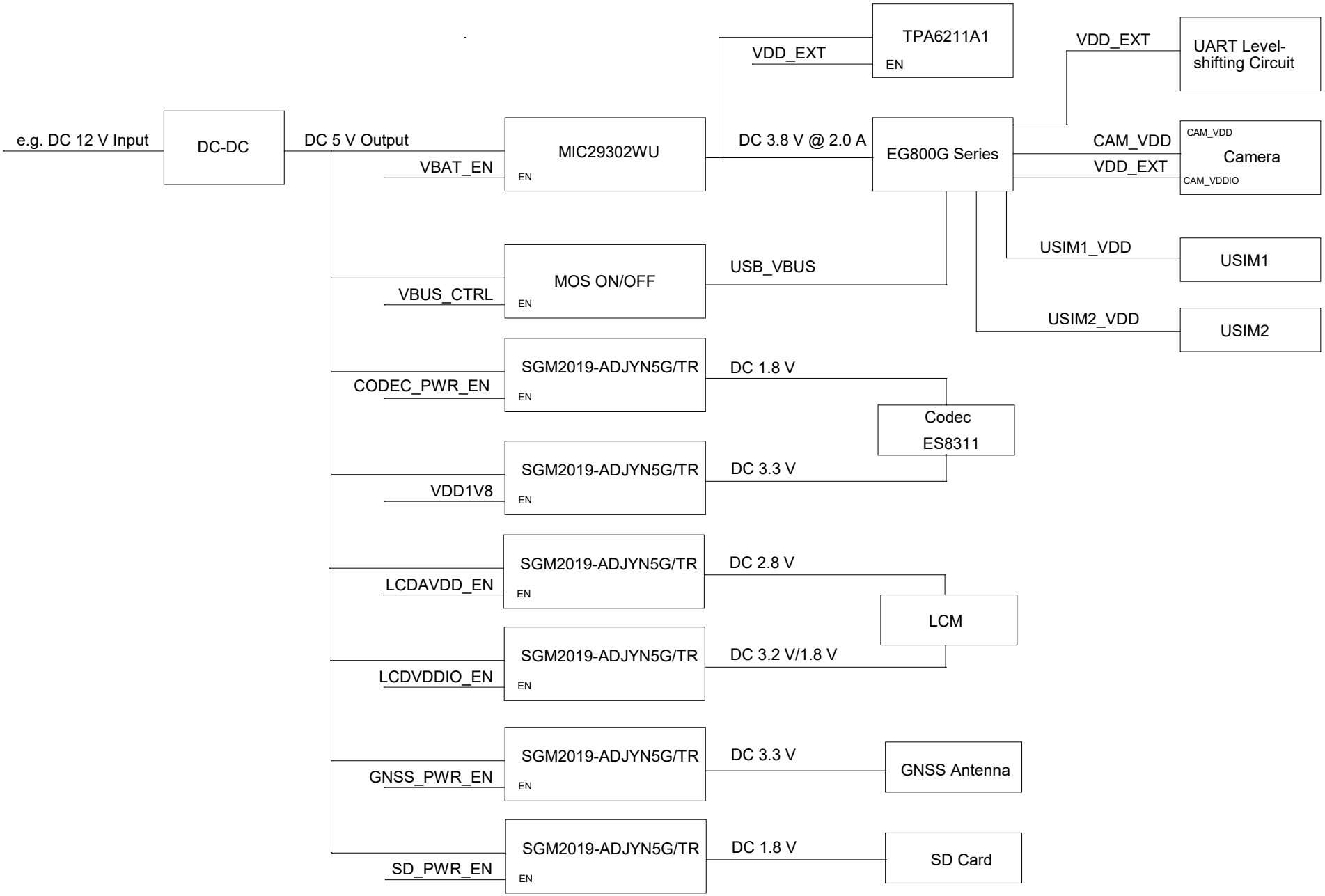
Power System Block Diagram



NOTE:

1. The power supply for the module should be at least 2 A.
2. EG800G-CN supports GNSS function and the function is optional. EG800G-EU/-LA does not support GNSS function.

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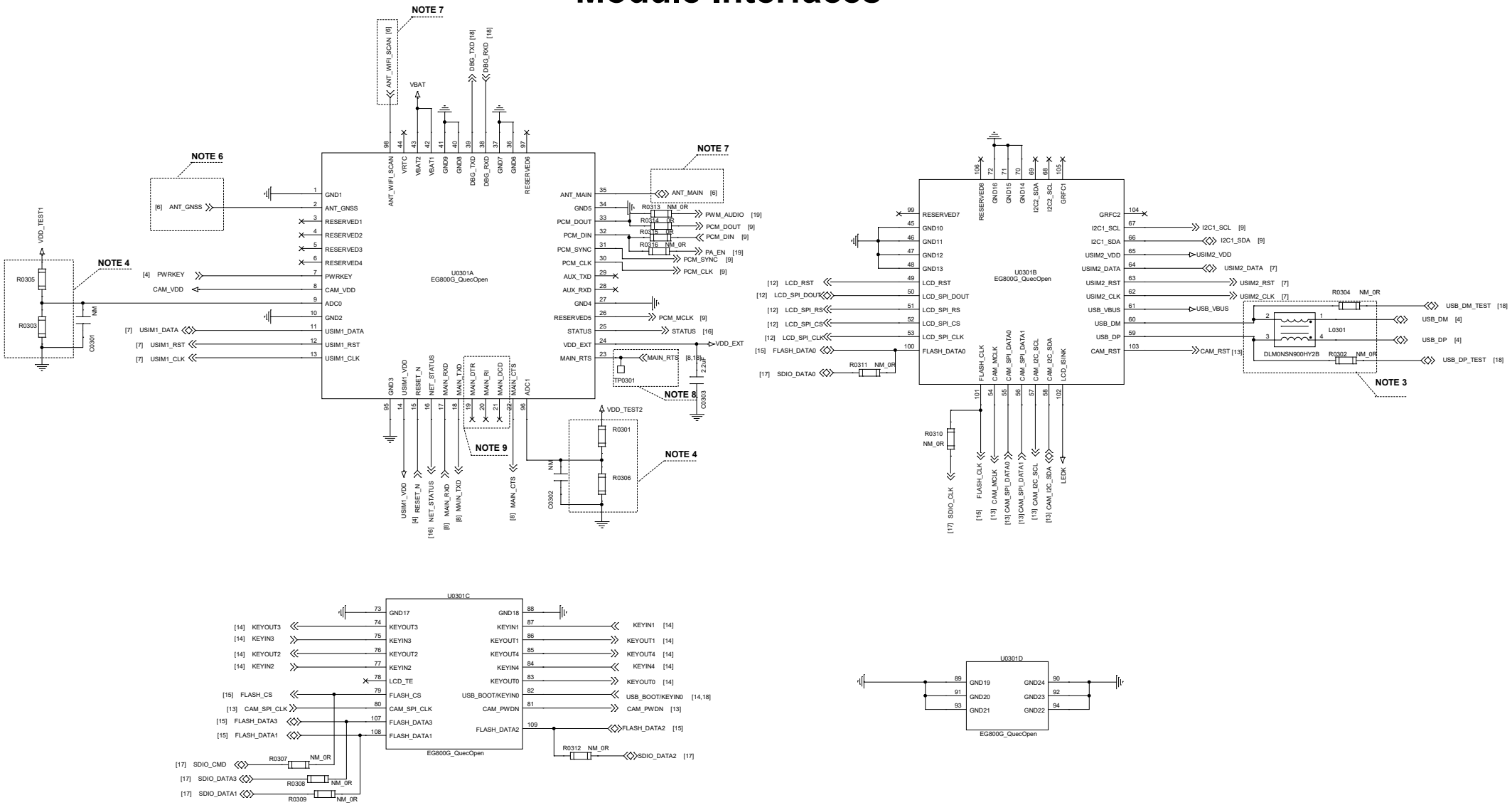
Module Interfaces



NOTE:

1. Keep unused and RESERVED pins open, and all GND pins should be connected to the ground.
2. Ensure there is a complete reference ground plane below the module, and the ground plane is as close to the module layer as possible. It is recommended to design at least 4-layers.
3. A common mode choke L0301 is recommended to be added in series between the module and your MCU to suppress EMI.

   Meanwhile, reserve the test points for upgrading the firmware over USB interface and minimize the extra stubs of the trace. L0301 and the two resistors R0302 and R0304 should be placed close to the module to ensure the integrity of USB signal.
4. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins, it is strongly recommended to reserve the voltage divider circuit for better compatibility with other Quectel modules.

   The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced. When the divider circuit is not used, the ADC pins require 1 kΩ resistors in series.
5. If the forced download function is not used, USB_BOOT/KEYIN0 cannot be pulled down to low level or pulled up to high level before the module is successfully turned on. KEYIN1, KEYIN2 cannot be pulled down to low level before the module is successfully turned on.
6. EG800G-CN supports GNSS function and the function is optional. EG800G-EU/-LA does not support GNSS function.
7. EG800G-CN supports Wi-Fi scan function, which shares the same antenna interface with main antenna. The two functions cannot be used simultaneously.

   EG800G-EU/-LA provides a dedicated Wi-Fi scan antenna interface (ANT_WIFI_SCAN). Wi-Fi scan supports receiving only.
8. Test points must be reserved for MAIN_RTS, DBG_TXD/_RXD, USB_DP/_DM and USB_VBUS. It is recommended to reserve test points for USB_BOOT/KEYIN0, VDD_EXT, VBAT and PWRKEY.

   If RESET_N is unused, it is recommended to reserve a test point.
9. MAIN_DTR, MAIN_RI and MAIN_DCD do not have the functions described by the pin names and their default functions are GPIOs.

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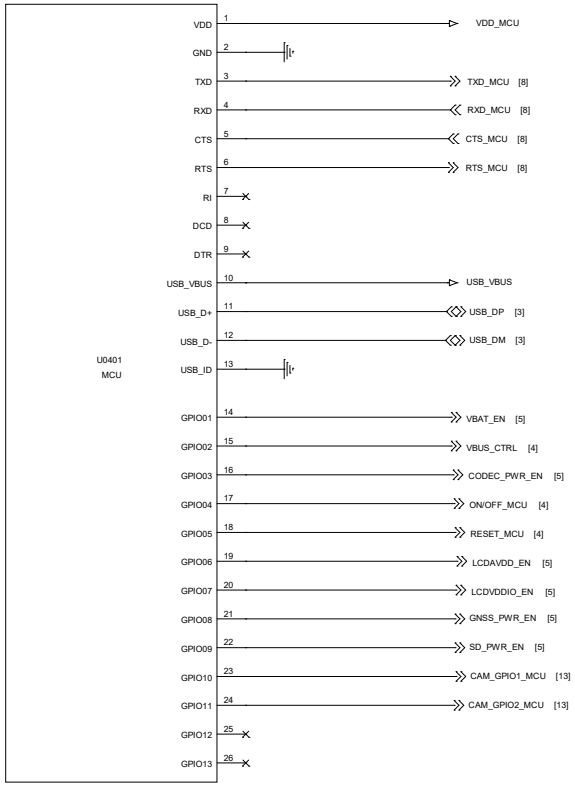
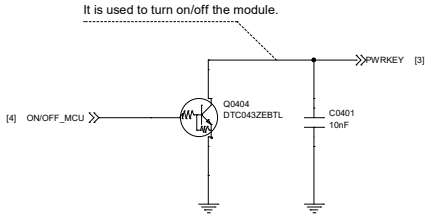
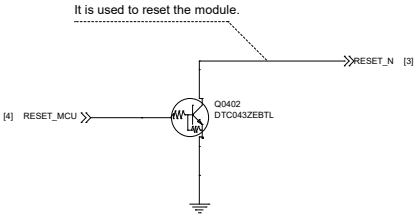
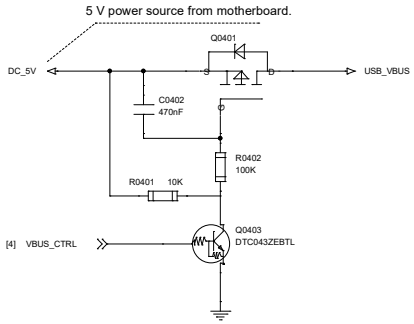
MCU Interfaces









NOTE:

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V. If the GPIO interfaces of U0401 share the same power domain, the related level-shifting circuit is not needed.
2. The USB 2.0 interface of the module only serves as a slave device and supports full-speed and high-speed modes. To communicate with the USB interface, MCU needs to support USB host mode or OTG function.

   The USB_VBUS pin of the module should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the default low-level GPIO pins of MCU as the control pins for PWRKEY and RESET_N of the module. Ensure that the maximum load capacitance of pins PWRKEY and RESET_N does not exceed 10 nF.

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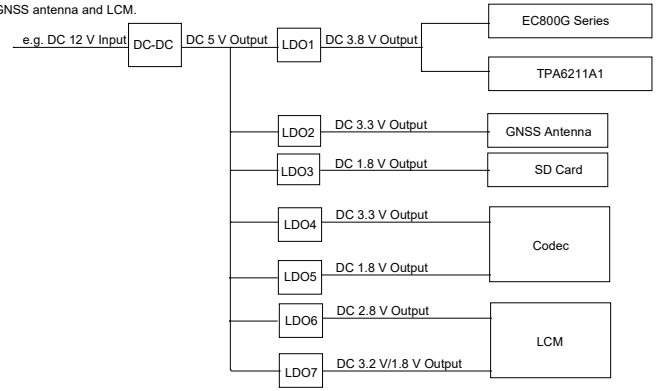
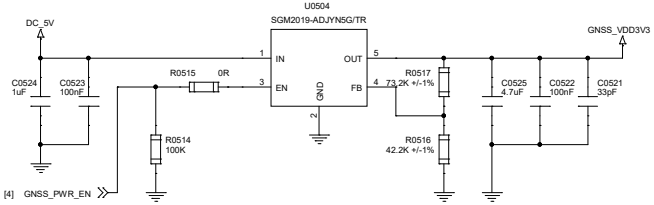
Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage into a 5.0 V, and then use LDOs to convert it to 3.8 V, 3.3 V, 3.2 V, 2.8 V,and 1.8 V to power the module, audio PA, SD card, codec, GNSS antenna and LCM.



GNSS Antenna Power Supply

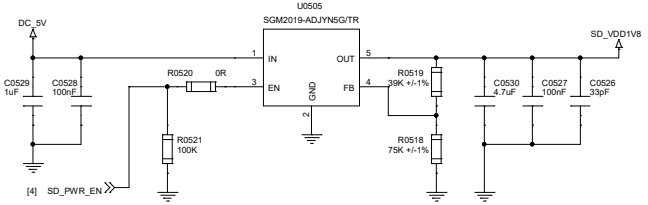


GNSS_VDD3V3 = 1.207 × (1 + R0517 / R0516) ≈ 3.3 V

NOTE:

EG800G-CN supports GNSS function and the function is optional. EG800G-EU/-LA does not support GNSS function.

SD Card Power Supply

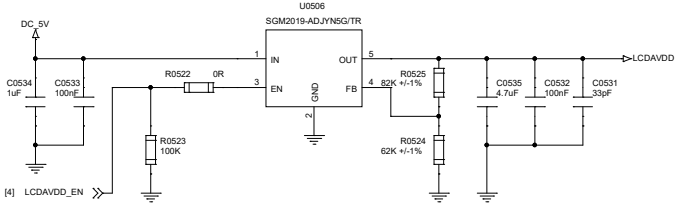


SD_VDD1V8 = 1.207 × (1 + R0519 / R0518) ≈ 1.8 V

NOTE:

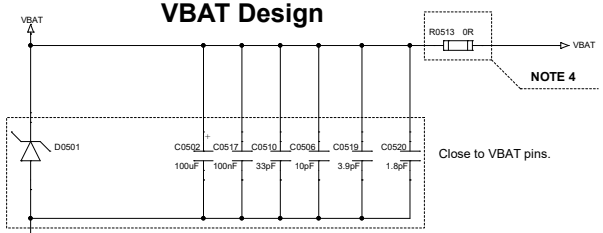
Only 1.8 V SD card is supported.

LCM Analog Power Supply



LCDAVDD = 1.207 × (1 + R0525 / R0524) ≈ 2.8 V

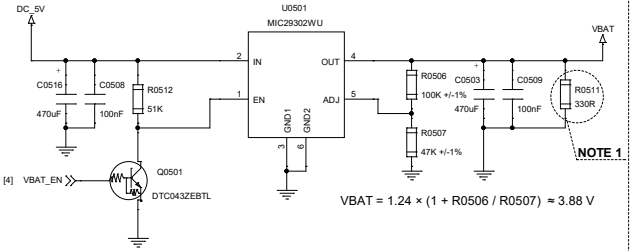
VBAT Design



NOTE:

1. The power supply should be able to provide sufficient current of at least 2.0 A for the module.
2. The width of VBAT trace should be at least 2 mm.
3. The recommended operating voltage of VBAT ranges from 3.3 V to 4.3 V.
   The typical operating voltage of VBAT is 3.8 V.
4. It is recommended to reserve a 0 Ω resistor (minimum package size: 0603) for future debugging.
   The resistor should be placed close to VBAT pins.

LDO Application

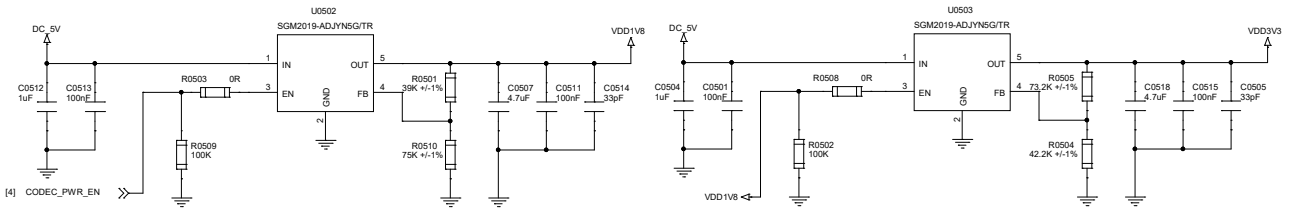


VBAT = 1.24 × (1 + R0506 / R0507) ≈ 3.88 V

NOTE:

1. The recommended load current is greater than 10 mA.
2. When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.

Codec Power Supply



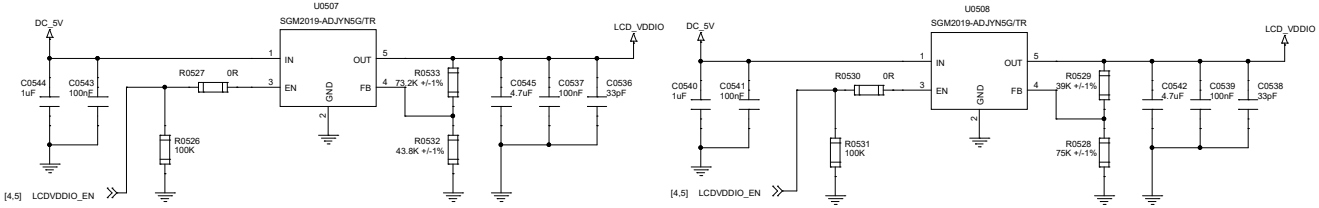
VDD1V8 = 1.207 × (1 + R0501 / R0510) ≈ 1.8 V

VDD3V3 = 1.207 × (1 + R0505 / R0504) ≈ 3.3 V

NOTE:

1. VDD1V8 and CODEC_PWR_EN are used to turn on/off of VDD3V3 and VDD1V8 respectively.
2. To ensure proper functioning of the audio codec, adhere to the following power-up/down sequences:
   Power-up sequence: power on VDD1V8 first, followed by VDD3V3.
   Power-down sequence: power off VDD3V3 first, followed by VDD1V8.

LCM Digital Power Supply



LCD_VDDIO = 1.207 × (1 + R0533 / R0532) ≈ 3.2 V

LCD_VDDIO = 1.207 × (1 + R0529 / R0528) ≈ 1.8 V

NOTE:

1. When the LCM is used in the 3.2 V voltage domain, see the design of the U0507.
2. When the LCM is used in the 1.8 V voltage domain, see the design of the U0508.

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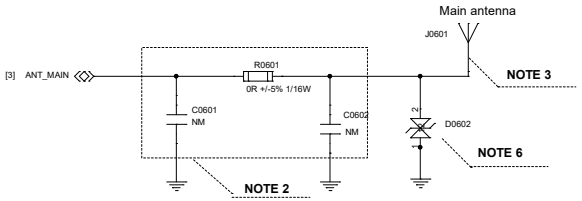
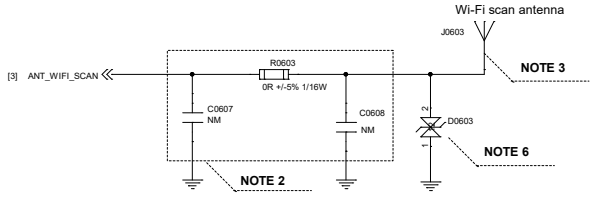
Antenna Interface Design

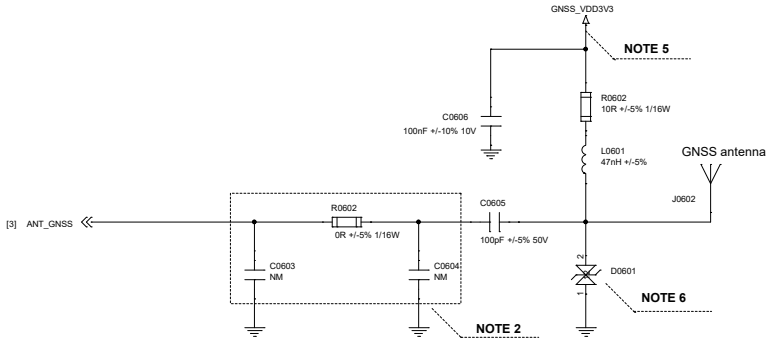
Main Antenna Interface



Wi-Fi Scan Antenna Interface



GNSS Antenna Interface

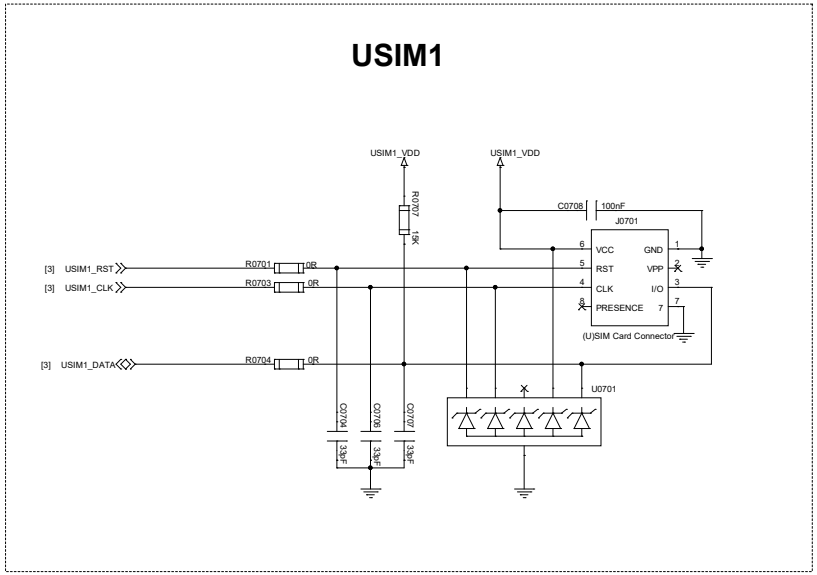


NOTE:

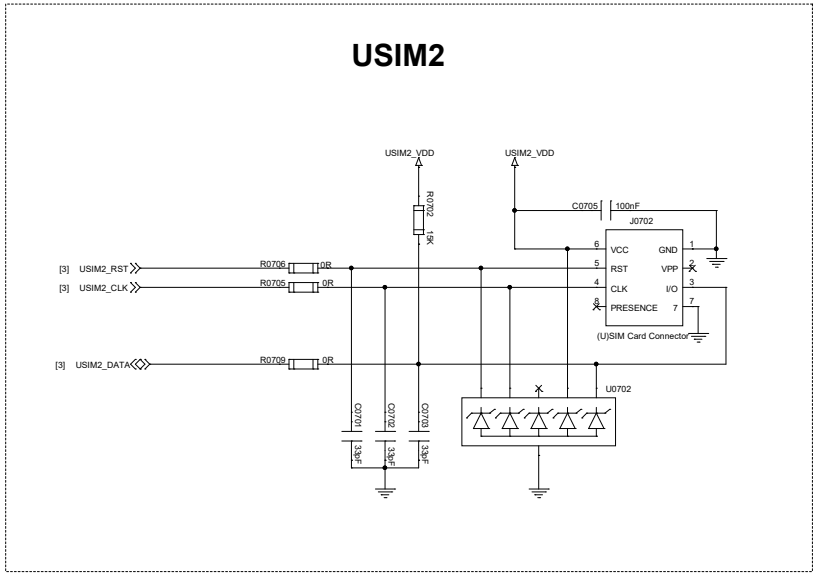
1. The single-ended impedance of the RF antenna is 50 Ω.
2. It is recommended to reserve a Π-type matching circuit at these antenna interfaces.
3. EG800G-CN supports Wi-Fi scan function, which shares the same antenna interface with main antenna. The two functions cannot be used simultaneously.
   EG800G-EU/-LA provides a dedicated Wi-Fi scan antenna interface (ANT_WIFI_SCAN). Wi-Fi scan supports receiving only.
4. EG800G-CN supports GNSS function and the function is optional. EG800G-EU/-LA does not support GNSS function.
5. The active antenna uses an LDO for power supply, and GNSS_VDD3V3 circuit is not needed when using a passive antenna.
6. The junction capacitance of the ESD protection component on the antenna interfaces is recommended to be less than 0.05 pF.

USIM Interface Design

USIM1



USIM2

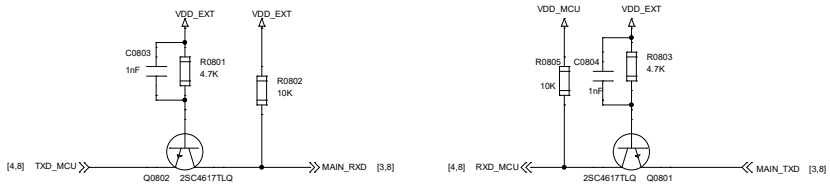


NOTE:

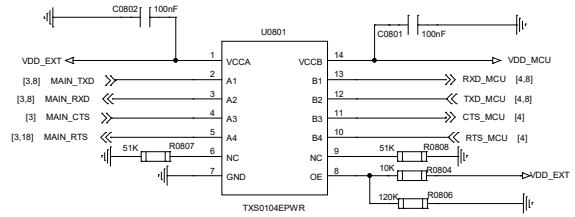
1. U0701 and U0702 are recommended to be used to offer good ESD protection, and the parasitic capacitance should not exceed 15 pF.
2. The pull-up resistors R0707 and R0702 can improve anti-jamming capability, and should be placed close to the USIM card connector.
3. R0701, R0703–R0706 and R0709 are used for debugging, and C0701–C0704, C0706 and C0707 are used for filtering out RF interference.
4. C0708 and C0705's capacitance should be less than 1 μF and they should be placed close to the USIM card connector.
5. The GND of the USIM card connector is recommended to be connected to the GND layer directly.
6. For more information about the layout of USIM interface, see the hardware design document of the module.
7. USIM_DET can be multiplexed from any GPIO pin of the module, which is at 1.8 V power domain.

UART Interface Design

UART Level-shifting Circuit - Transistor Solution



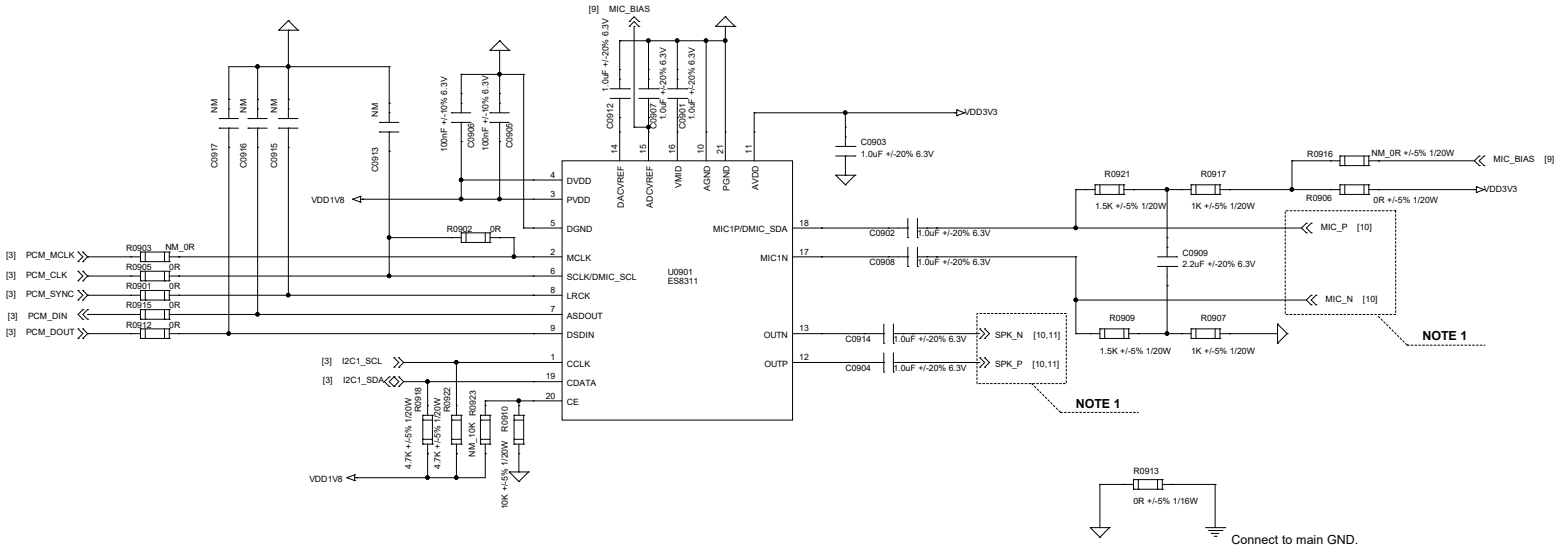
UART Level-shifting Circuit - IC Solution



NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, and the latter one is recommended.
2. The power supply of TXS0104EPWR's VCCA should not exceed that of VCCB. For more information, see the datasheet of TXS0104EPWR.
3. The transistor solution is not suitable for applications with baud rates exceeding 460 kbps. The capacitors C0803 and C0804 of 1 nF can improve the signal quality.
4. MAIN_RTS transistor circuit is similar to that of the MAIN_RXD. MAIN_CTS transistor circuit is similar to that of the MAIN_TXD.

Audio Codec Design (ES8311)



NOTE:

1. Differential signal that can be connected to an audio power amplifier.
2. If you needs PCM_MCLK, you can use pin 26 of the module.

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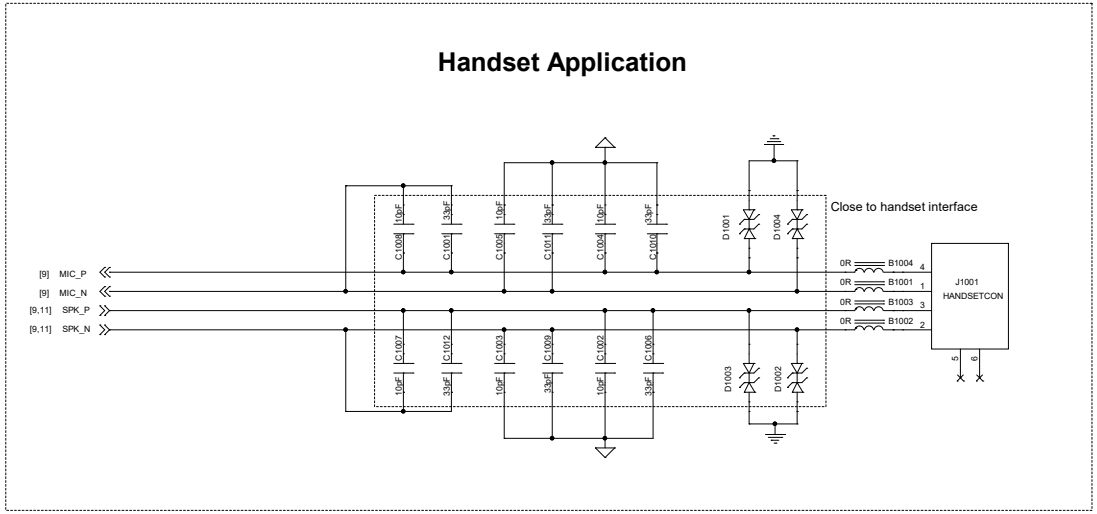
Audio Codec Interface Design



NOTE:

1. The codec analog output can drive handset. For larger power loads such as loudspeaker, add an audio power amplifier in the design.
2. In handset application, route the MIC and SPK signal traces as differential pairs.
3. Surround all MIC and SPK signal traces with ground on the same layer and with ground planes above and below to minimize noise interference, such as clock and DC-DC signals.

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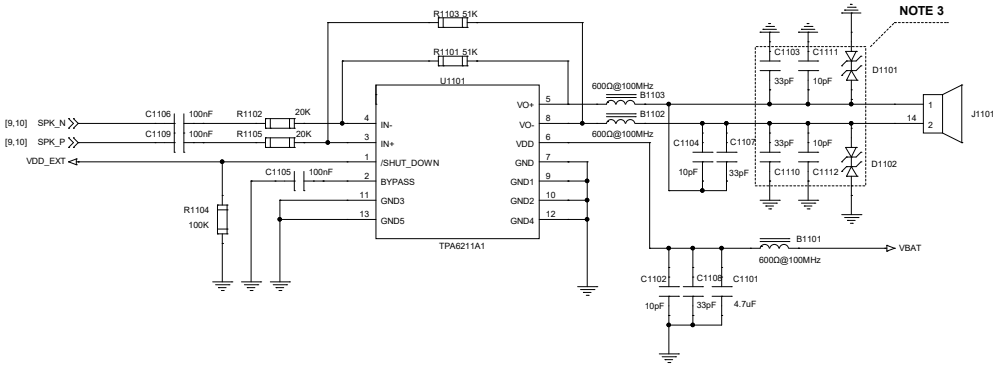
Analog Audio Design (Audio Power Amplifier)



NOTE:

1. SPK_P and SPK_N channels are differential output channels intended for connecting to an external audio amplifier.
   To eliminate POP noise, it is recommended to utilize VDD_EXT of the module as the control signal for the audio power amplifier's enable pin.
2. The audio power amplifier model in this design is for reference only. Select the amplifier with appropriate power according to actual needs.
3. When designing the layout, ensure that filter capacitors and ESD protection components are placed close to the loudspeaker to filter out interference and provide adequate protection.
4. The selection of ESD protection components should consider the output voltage range of the audio power amplifier. Ensure that the output voltage of the audio power amplifier remains within the maximum reverse working voltage range of ESD protection components under normal operating conditions. This precaution helps prevent damage to the ESD protection components.

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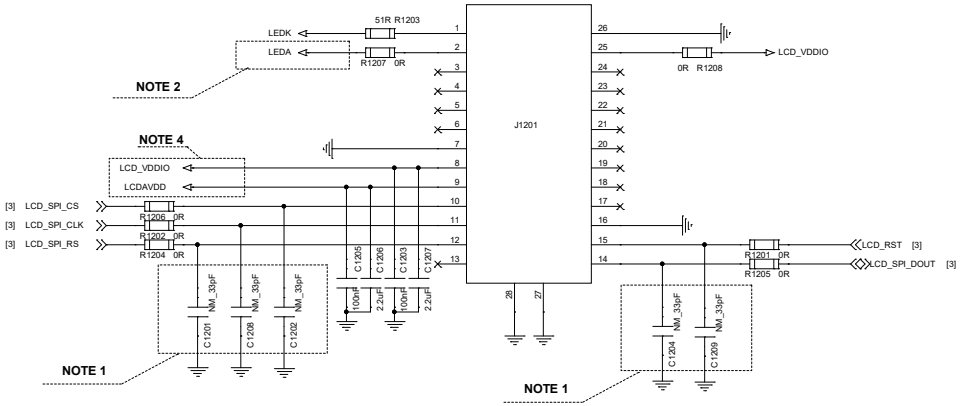
LCM Interface Design



NOTE:

1. The 33 pF capacitors of the signal pins are reserved, and can be used as per the actual debugging situation.
2. The power supply pin LEDA of the backlight is provided by external power supply circuit, and you can design the circuit by yourself.
3. It is strongly recommended to use switch control for all power supplies, otherwise there may be leakage and power consumption increase.
4. To avoid abnormal LCD display caused by power fluctuation, the filter capacitors of the LCD power supply pins, LCDAVDD and LCD_VDDIO, must be mounted.

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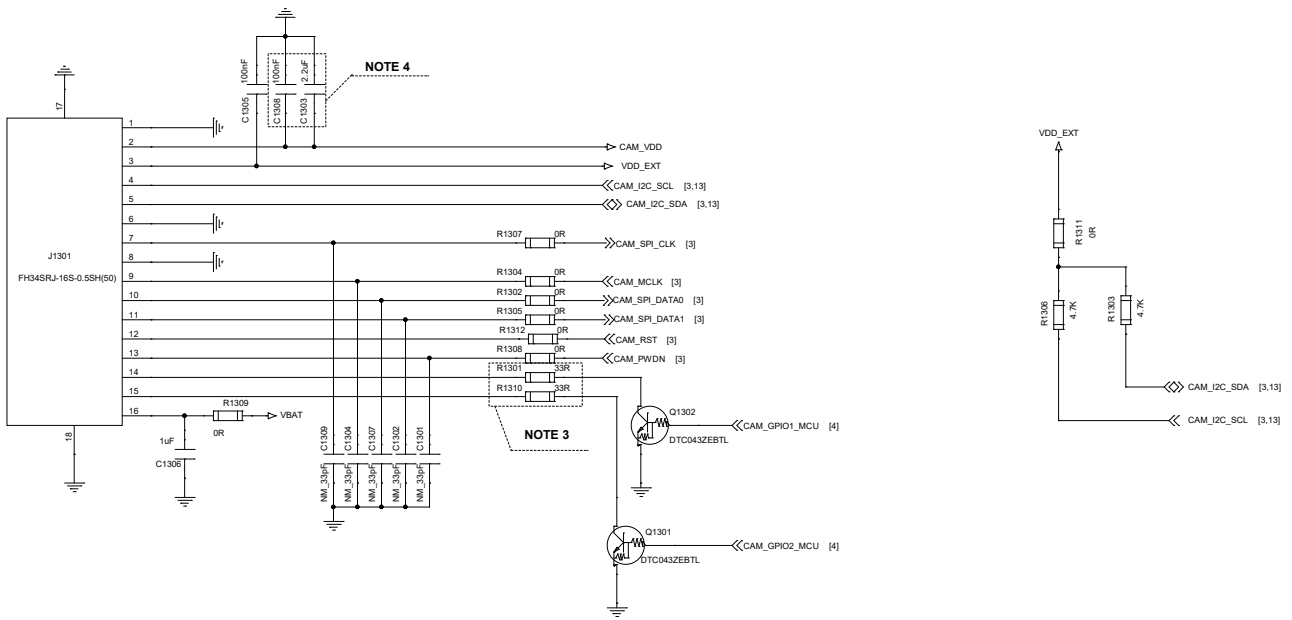
Camera Interface Design



NOTE:

1. By controlling the triode switching circuit, CAM_GPIO1_MCU controls the cathode of the positioning light of the camera, and CAM_GPIO2_MCU controls the cathode of the supplement light of the camera.
   It is recommended to select default pull-down GPIO pins as the two control pins.
2. The 33 pF capacitors of signal pins should be reserved, and be used according to the actual debugging situation.
3. The values of current limiting resistors of positioning light and supplement light (R1301 and R1310) should be varied according to the required brightness.
4. The capacitors of the CAM_VDD power supply should be connected to the GND layer directly, otherwise, power supply noise may lead to abnormalities such as white dots on the preview screen.
5. It is recommended to design camera power supply by yourself.
6. It is strongly recommended to use switch control for all power supplies, otherwise there may be leakage and power consumption increase.

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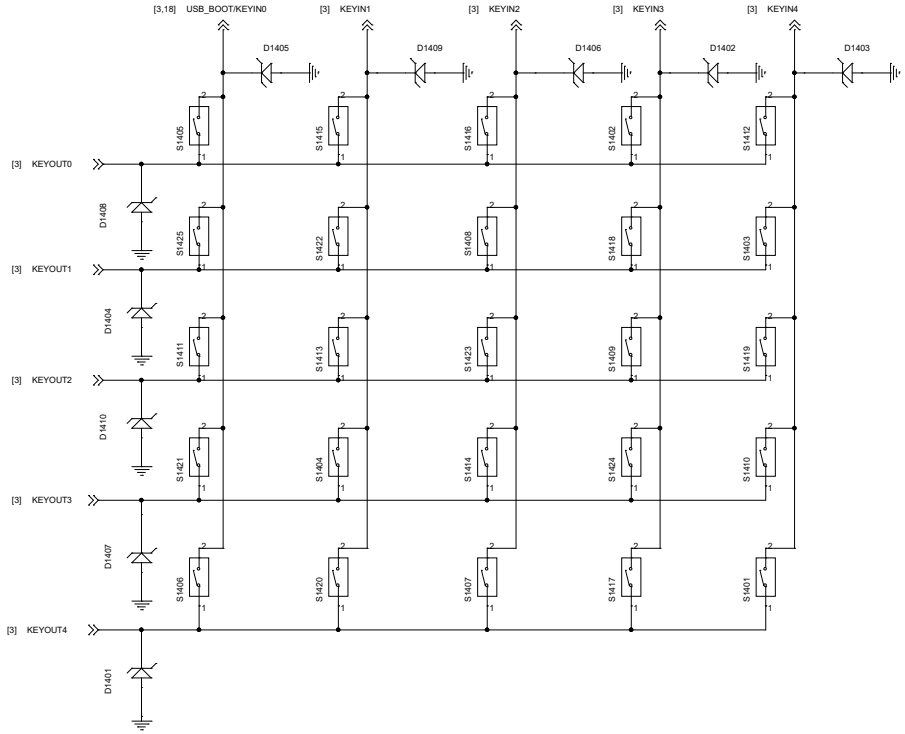
Matrix Keypad Interface Design



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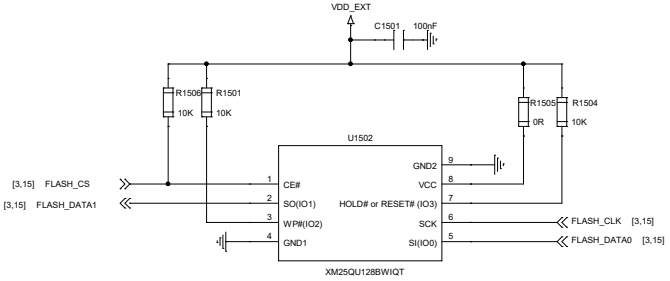
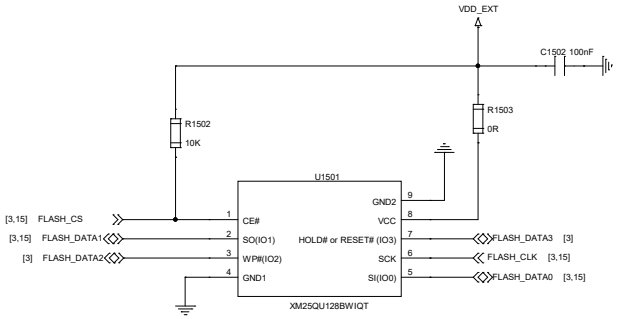
External Flash Interface Design

Four-wire NOR Flash Circuit



Six-wire NOR Flash Circuit



NOTE:

1. The filter capacitors C1501 and C1502 need to be placed close to the power supply pins of the flash chip.
2. For the four-wire NOR flash circuit, it is recommended to connect WP# and HOLD# pins with pull-up resistors to avoid damaging flash chips caused by abnormal levels, resulting in abnormal transmission or data loss.

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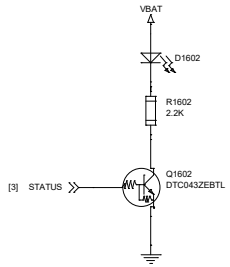
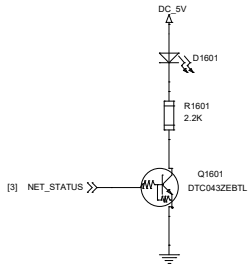
Indicators

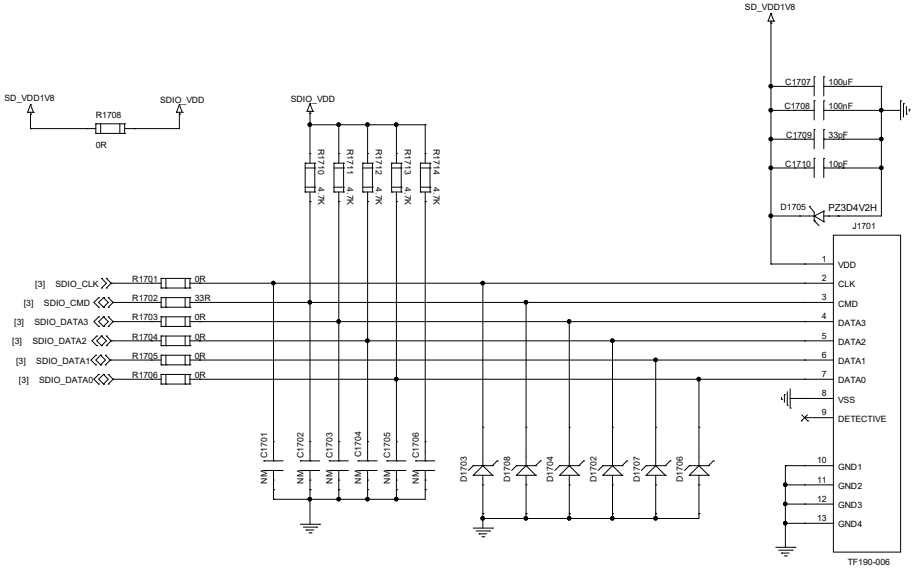




NOTE:

1. For more details about STATUS and NET_STATUS, see the hardware design document of the module.
2. If the low power consumption is required when your application is in sleep status, replace the power supplies (VBAT and DC_5V) of STATUS and NET_STATUS indication LEDs with the external controllable ones, which can be turned off to reduce the power consumption during module sleep status.

SD Card Interface Design



NOTE:

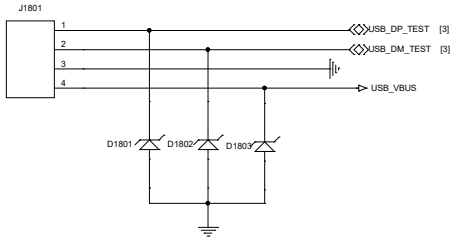
1. Only 1.8 V SD card is supported.
2. To avoid bus jitter, it is recommended to add pull-up resistors R1710–R1714 to the SDIO signal traces. The recommended value is 4.7 kΩ.

   The pull-up power supply must select the SDIO_VDD.
3. To improve signal quality, it is recommended to add resistors R1701–R1706 in series between the module and the SD card connector.

   The bypass capacitors C1701–C1706 are reserved and not mounted by default.
4. It is recommended to add ESD protection components near the pins of SD card connector. The parasitic capacitance of ESD protection components should be less than 15 pF.
5. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, as well as noisy signals such as clock and DC-DC signals.
6. Route SDIO signals with 50 Ω ±10 % impedance. It is important to route SDIO signals surrounded with ground on the same layer and with ground planes above and below, and the total trace length should be less than 50 mm.
7. It is recommended to keep the traces among SDIO_CLK and SDIO_DATA[0:3]/SDIO_CMD with equal length (the difference among them is less than 1 mm).
8. Make sure the adjacent trace spacing is twice the trace width and the bus capacitance is less than 15 pF.

Test Points

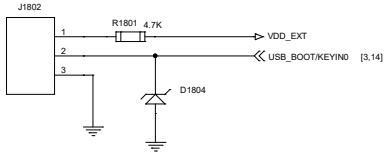
USB Interface Test Points



NOTE:

1. Test points must be reserved for USB interface.
2. The module can upgrade firmware and debug the software over USB interface.
   The parasitic capacitance of the ESD protection components on USB data traces should be less than 2 pF.

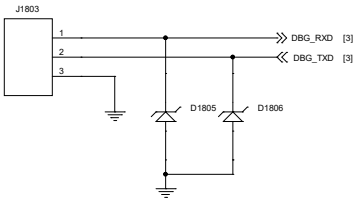
Forced Download Interface Test Point



NOTE:

1. It is recommended to reserve a test point for forced download interface.
2. Pull down the USB_BOOT/KEYIN0 to GND before the module starts up, and the module will enter the forced download mode when it is turned on. In this mode, the module supports firmware upgrading over USB interface.

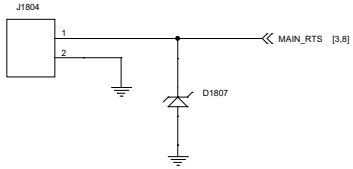
Debug UART Test Points



NOTE:

1. Test points must be reserved for DBG_TXD and DBG_RXD to capture AP logs.
2. The debug UART supports 1.8 V power domain, and a level-shifting circuit should be used if the power domain of your application is 3.3 V. For details, see the sheet "UART Interface Design".
3. The debug UART only supports the baud rate of 2000000 bps.

MAIN_RTS Test Point



NOTE:

1. A test point must be reserved for MAIN_RTS to capture CP logs.
2. MAIN_RTS supports 1.8 V power domain, and a level-shifting circuit should be used if the power domain of your application is 3.3 V. For details, see the sheet "UART Interface Design".
3. When capturing CP logs, set the baud rate to 8000000 bps.

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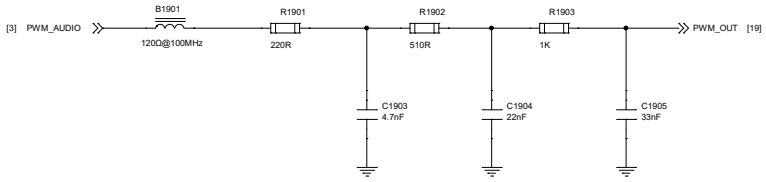
PWM Design

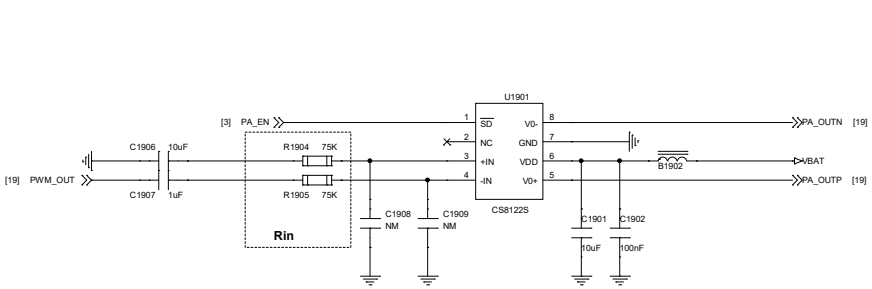
RC-filter Circuit

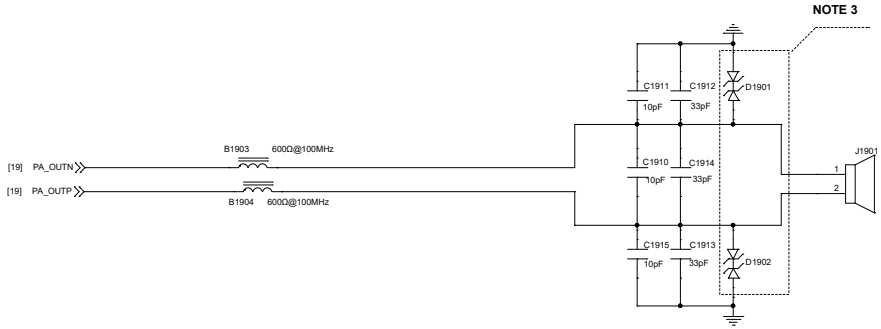


NOTE:

1. You can reserve a second-order or third-order RC low-pass filter circuit, and the capacitance and resistance need to be adjusted according to the audio effect and the matched audio PA. This circuit is for reference only.
2. You can use low-pass filters such as first-order, second-order or third-order RC or LC according to the needs.

PA Design





NOTE:

1. Rin is the input resistance. By adjusting the resistance of the input resistor, the amplification factor of the audio PA can be set.
   The calculation formula is: Gain = 2 × 150 kΩ / Rin.
2. Choose the audio power amplifier with appropriate power according to the actual needs.
3. The selection of ESD protection components should consider the output voltage range of the audio power amplifier. Ensure that the output voltage of the audio power amplifier remains within the maximum reverse working voltage range of ESD protection components under normal operating conditions. This precaution helps prevent damage to the ESD protection components.

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