EC800Z-CN QuecOpen Reference Design

LTE Standard Module Series

Version: 1.0

Date: 2024-04-25

Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2023-12-28	George OU	Creation of the document
1.0	2024-04-25	George OU/Leon LIANG	First official release

Contents

1 Reference Design

1.1. Introduction

This document is only applicable to EC800Z-CN industrial-grade module in QuecOpen® solution.

This document provides the reference design for Quectel EC800Z-CN module in QuecOpen® solution. The reference design mainly includes block diagrams, power supply design, UART and USIM interfaces, antenna interface, analog audio interface, audio codec design, LCM and camera interfaces and other designs.

The module has two versions, and the recommended operating voltage ranges are as follow.

- Normal-voltage version (without built-in DC-DC converter): 3.3–4.3 V.
- Low-voltage version (with built-in DC-DC converter): 2.3–3.8 V.

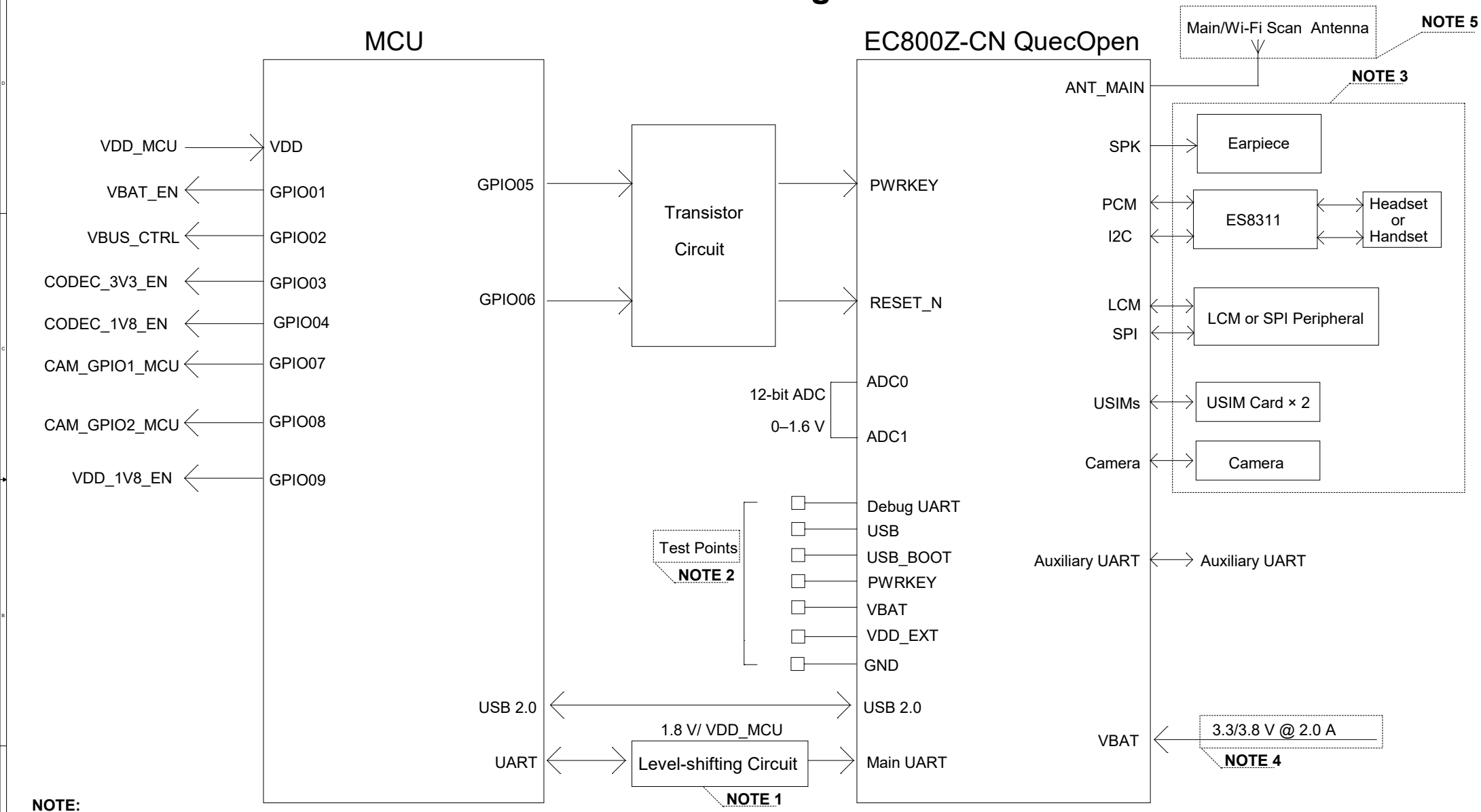
1.2. Schematics

The schematics illustrated in the following pages are provided for reference only.

NOTE

It is required to confirm the applicability and price from the supplier about the IC involved in the reference design.

Block Diagram



NOTE:

1. A transistor solution or an IC solution TXS0104EPWR provided by Texas Instruments is recommended.
2. Test points of DBG_TXD/RXD, USB_VBUS, USB_DP/DM, USB_BOOT and VDD_EXT must be reserved. It is recommended to reserve the test points of PWRKEY (only for normal-voltage version) and VBAT. A test point of RESET_N is recommended to be reserved if unused.
3. Analog audio, LCM and Camera interfaces are only supported by normal-voltage version, and the interfaces are optional. The PCM interface is supported by low-voltage version and is optional for normal-voltage version. USIM2 interface and camera interface cannot be used at the same time.
4. The typical value of power supply is 3.8 V for normal-voltage version and 3.3 V for low-voltage version.
5. Wi-Fi scan function is optional. This function and LTE network cannot be used simultaneously since they share the same antenna interface.

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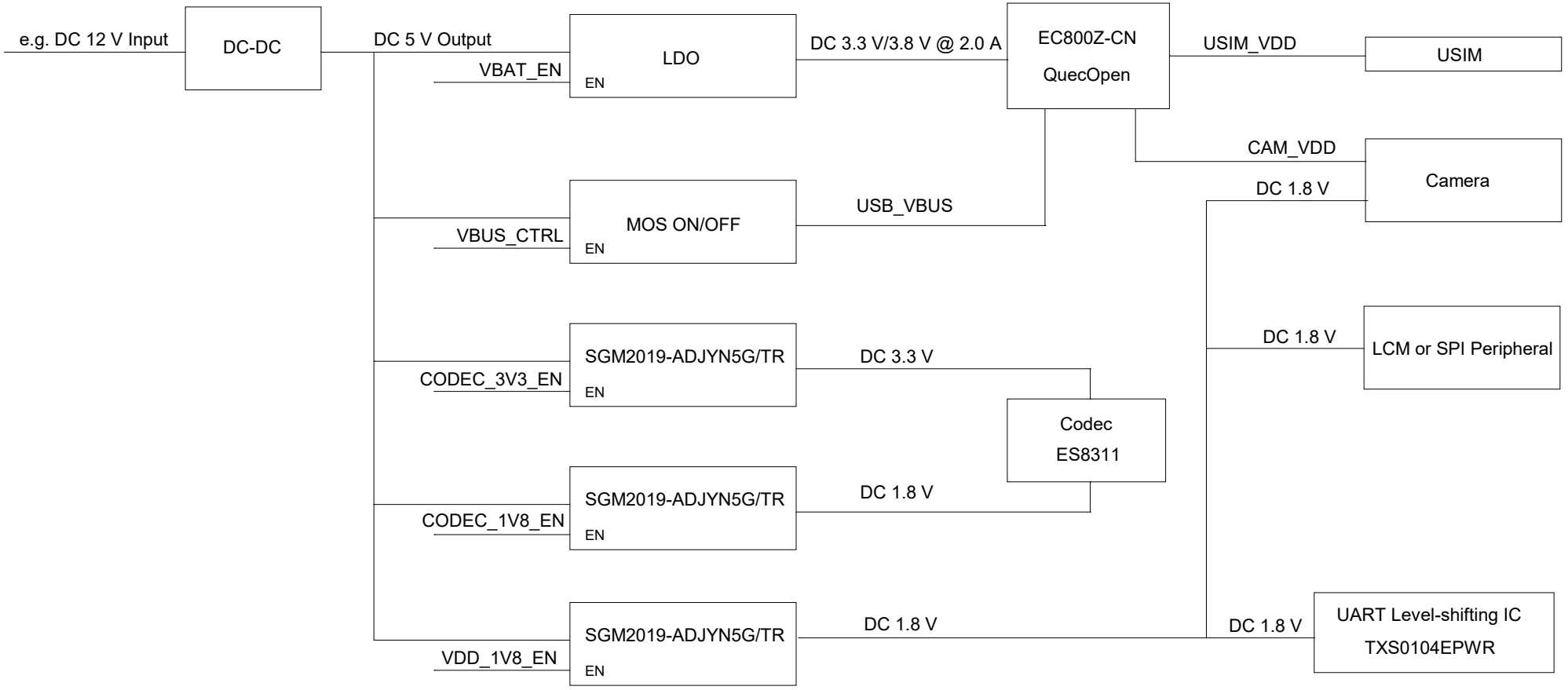
Power System Block Diagram

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to 5.0 V, and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V to power the module, Codec, LCM, SPI, Camera and UART level-shifting IC.



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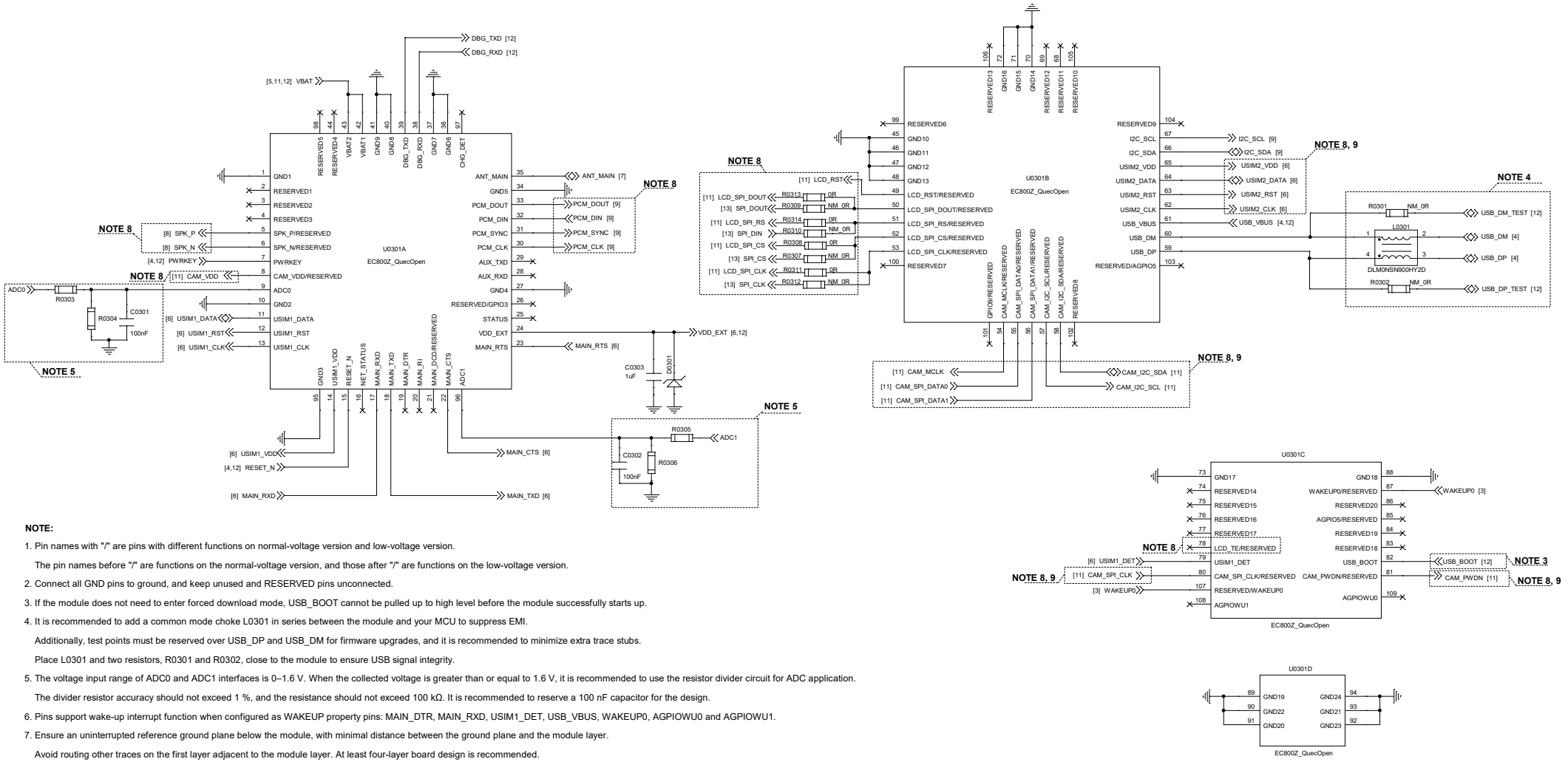
Module Interfaces



NOTE:

1. Pin names with "/" are pins with different functions on normal-voltage version and low-voltage version.
   The pin names before "/" are functions on the normal-voltage version, and those after "/" are functions on the low-voltage version.
2. Connect all GND pins to ground, and keep unused and RESERVED pins unconnected.
3. If the module does not need to enter forced download mode, USB_BOOT cannot be pulled up to high level before the module successfully starts up.
4. It is recommended to add a common mode choke L0301 in series between the module and your MCU to suppress EMI.
   Additionally, test points must be reserved over USB_DP and USB_DM for firmware upgrades, and it is recommended to minimize extra trace stubs.
   Place L0301 and two resistors, R0301 and R0302, close to the module to ensure USB signal integrity.
5. The voltage input range of ADC0 and ADC1 interfaces is 0–1.6 V. When the collected voltage is greater than or equal to 1.6 V, it is recommended to use the resistor divider circuit for ADC application.
   The divider resistor accuracy should not exceed 1 %, and the resistance should not exceed 100 kΩ. It is recommended to reserve a 100 nF capacitor for the design.
6. Pins support wake-up interrupt function when configured as WAKEUP property pins: MAIN_DTR, MAIN_RXD, USIM1_DET, USB_VBUS, WAKEUP0, AGPIOWU0 and AGPIOWU1.
7. Ensure an uninterrupted reference ground plane below the module, with minimal distance between the ground plane and the module layer.
   Avoid routing other traces on the first layer adjacent to the module layer. At least four-layer board design is recommended.
8. Analog audio, camera and LCM interfaces are only supported by normal-voltage version, and the interfaces are optional. The PCM interface is supported by low-voltage version and is optional for normal-voltage version. GPIO9 and MAIN_DCD are only supported by normal-voltage version; GPIO3 is only supported by low-voltage version.
   If you need these functions, please contact Quectel Technical Support.
9. Pins 62-64 of USIM2 interface and pins 55, 80 and 81 of camera interface cannot be used at the same time.
10. The module supports SPI:
    (1) For the module of normal-voltage version, the SPI can be multiplexed from LCM interface. For more details, see the GPIO configuration document of the module.
    (2) For the module of low-voltage version, the SPI is also supported. For more details, please contact Quectel Technical Support.
11. The power domain of the module's GPIO pins is 1.8 V by default and can be configured to 3.3 V. For more details, please contact Quectel Technical Support.

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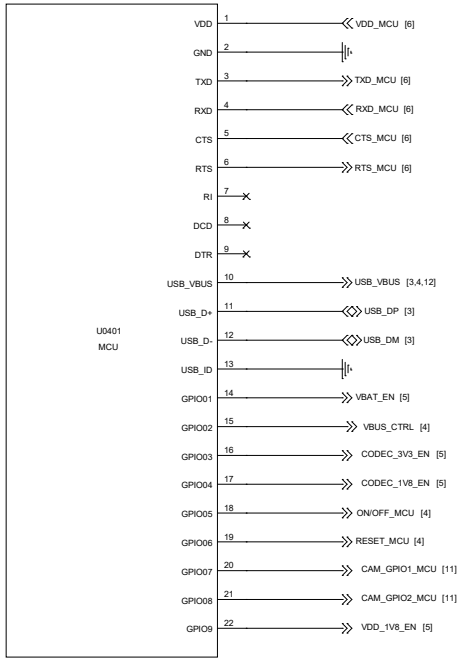
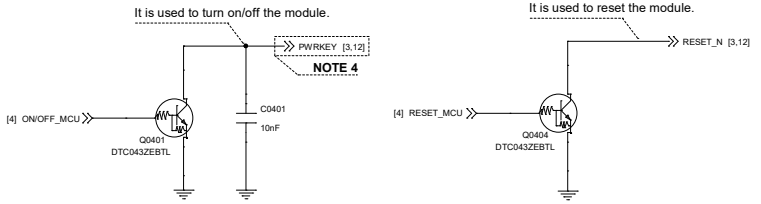
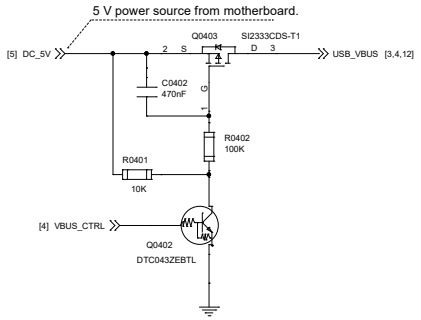
MCU Interfaces







NOTE:

1. If the voltage domain of the module interface is the same as that of the MCU interface, the level-shifting circuit is not necessary .
2. The USB interface of the module can only serve as a slave device, and supports full-speed and high-speed modes. To communicate with the USB interface, MCU needs to support USB host mode or OTG function.
   For USB detection, the USB_VBUS pin of the module should be powered by an external power system. Use VBUS_CTRL to control the on/off state of the USB_VBUS power supply.
3. It is recommended to choose MCU GPIO pins with a default low level to control the module's PWRKEY and RESET_N pins. Ensure that the load capacitance on these pins does not exceed 10 nF.
4. For the module of low-voltage version, it is turned on automatically after powering up and the PWRKEY pin should be kept unconnected. It can only be turned off by disconnecting the VBAT power supply.

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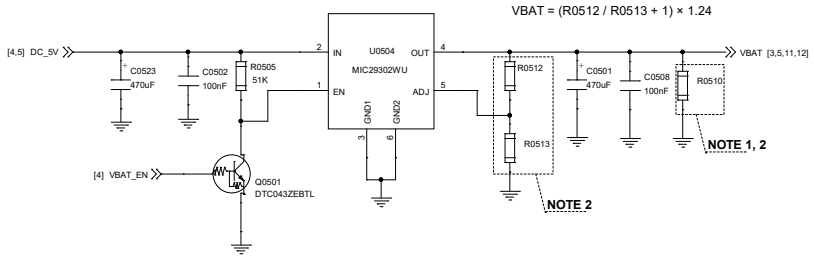
Power Supply Design

LDO Application

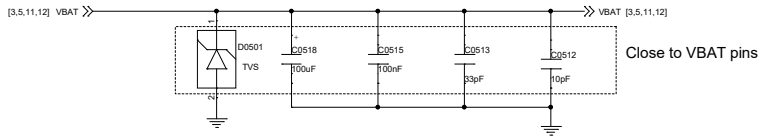
When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.3 V/3.8 V.



NOTE:

1. The recommended load current should exceed 10 mA.
2. Please adjust the parameters of R0510, R0512 and R0513 in accordance with the actual situation.

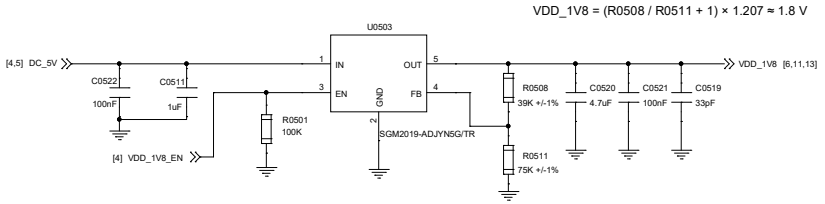
VBAT Design



NOTE:

1. The power supply for the module should be capable of supplying a minimum current of 2.0 A.
2. The width of each VBAT trace should be at least 2 mm.
3. The module has two versions: normal-voltage version (without built-in DC-DC converter) and low-voltage version (with built-in DC-DC converter).
   (1) Normal-voltage version: The recommended operating voltage range for VBAT is 3.3 V to 4.3 V, with a typical value of 3.8 V.
   (2) Low-voltage version: The recommended operating voltage range for VBAT is 2.3 V to 3.8 V, with a typical value of 3.3 V.

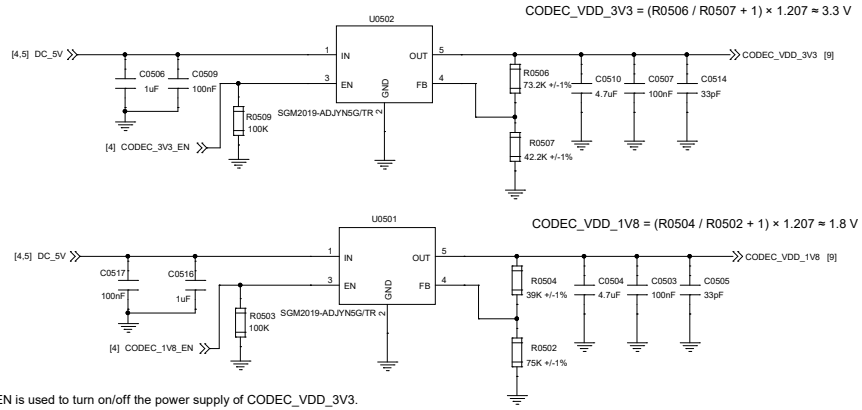
Power Supply for LCM & Camera & SPI Flash & UART Level-shifting IC



NOTE:

VDD_1V8_EN is used to turn on/off the power supply of VDD_1V8.

Power Supply for PCM Codec



NOTE:

1. CODEC_3V3_EN is used to turn on/off the power supply of CODEC_VDD_3V3.
   CODEC_1V8_EN is used to turn on/off the power supply of CODEC_VDD_1V8.
2. For ES8311 codec, CODEC_VDD_3V3 and CODEC_VDD_1V8 are powered up/down at the same time.

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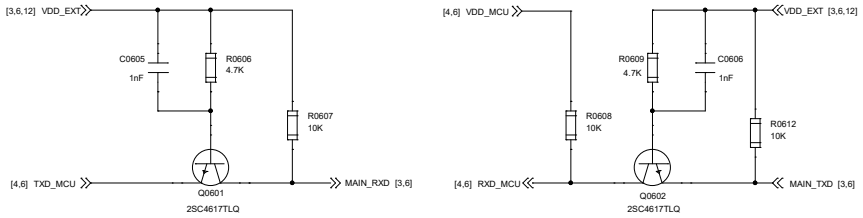
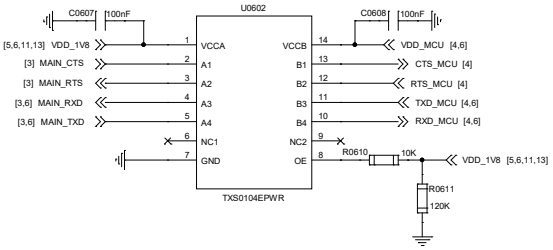
UART and USIM Interfaces

UART Level-shifting Circuit - Transistor Solution



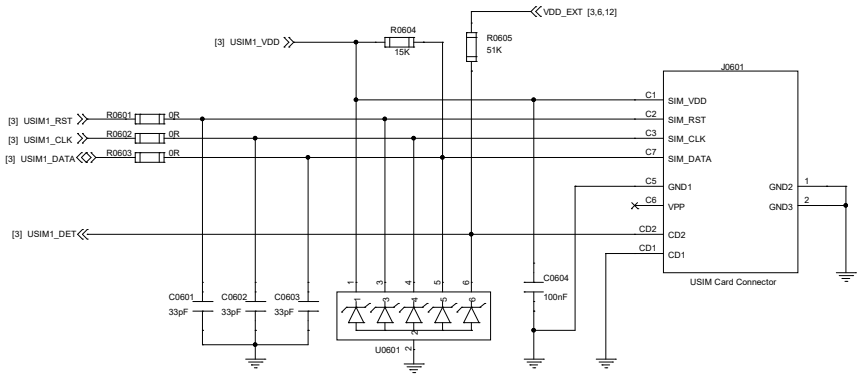
UART Level-shifting Circuit - IC Solution



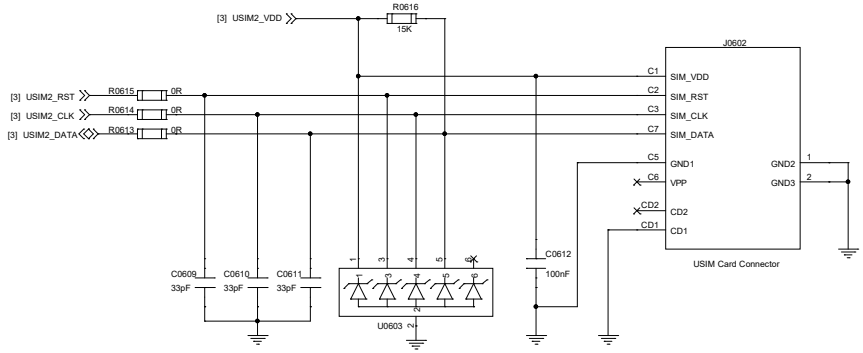
NOTE:

1. There are two level-shifting circuits: transistor solution and IC solution, and it is recommended to select the latter one.
2. The power supply of TXS0104EPWR's VCCA should not exceed that of VCCB. For more information, refer to the datasheet of TXS0104EPWR.
3. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C0605 and C0606 of 1 nF can improve the signal quality.
4. If the power domain of external MCU is the same as that of the module's UART, and MAIN_TXD is directly connected to the MCU's RXD, the module's MAIN_TXD should be pulled up to VDD_EXT via a 10 kΩ resistor to prevent the MCU from receiving error messages when the module is in sleep mode.
5. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.
6. The above "UART Level-shifting Circuit - IC Solution" are only applicable to the module's 1.8 V UART.

USIM1 Interface Design



USIM2 Interface Design



NOTE:

1. USIM2 interface (pins 62–65) is optional. If you need this function, please contact Quectel Technical Support.
2. Pins 62-64 of USIM2 interface and pins 55, 80 and 81 of camera interface cannot be used at the same time.
3. Only USIM1 interface of the module supports hot-plug detection.
4. It is recommended to use U0601 and U0603 for effective ESD protection with a parasitic capacitance below 15 pF.
5. For USIM1_DATA and USIM2_DATA, it is recommended to add 15 kΩ pull-up resistors R0604 and R0616 near the USIM card connectors to improve the anti-jamming capability of the USIM cards.
6. R0601–R0603 and R0613–R0615 are used for debugging, and C0601–C0603 and C0609–C0611 are used for filtering out RF interference.
7. The capacitance of C0604 and C0612 should be less than 1 μF and they should be placed close to the USIM card connectors.
8. If USIM1 and USIM2 interfaces are used simultaneously, ensure that both USIM interfaces use 1.8 V USIM cards.
9. For more information about the layout of USIM interfaces, see the hardware design document of the module.

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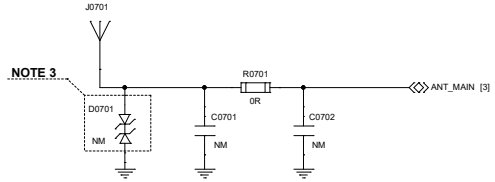
Antenna Interface

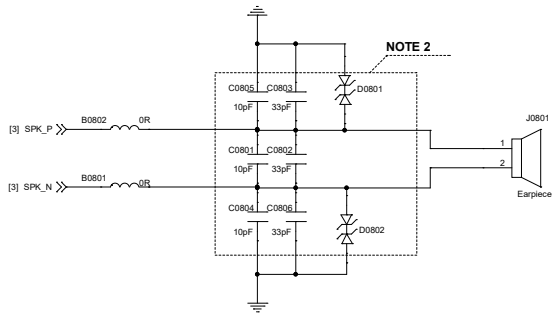


NOTE:

1. Use a Π-type matching circuit for the antenna interface.
2. The single-ended impedance of the RF antenna is 50 Ω, and the trace length should be minimized.
3. It is recommended to reserve an ESD protection component for the antenna interface and the junction capacitance should not exceed 0.05 pF.
4. Wi-Fi scan function is optional. This function and LTE network cannot be used simultaneously since they share the same antenna interface.
5. Main antenna and Wi-Fi scan only support passive antennas.

Analog Audio Interface

Earpiece Application



NOTE:

1. The analog audio interface (pins 5 and 6) is only supported by normal-voltage version, and the interface is optional.
   If you need this function, please contact Quectel Technical Support.
2. Place filter capacitors and ESD protection components close to the earpiece connector.

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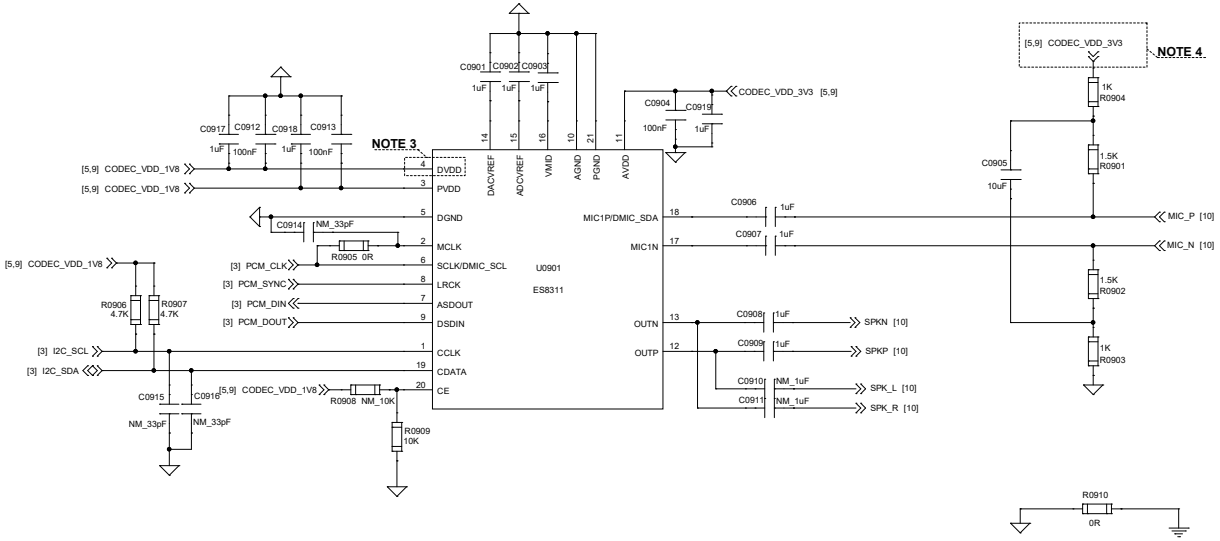
Audio Codec Design (ES8311)



NOTE:

1. PCM interface (pins 30–33) is supported by low-voltage version and is optional for normal-voltage version. If you need this function, please contact Quectel Technical Support.
2. ES8311 power-up/down sequences: AVDD, PVDD and DVDD are powered up/down at the same time.
3. When the sampling frequency is 8 kHz and the clock frequency is 512 kHz, DVDD must be connected to 1.8 V.
4. The bias voltage needs to be stable and the ripple should be as small as possible.
5. Differentiate between analog ground and digital ground. Connect analog ground and digital ground using a 0 Ω resistor.
6. For more details, see the datasheet of ES8311.

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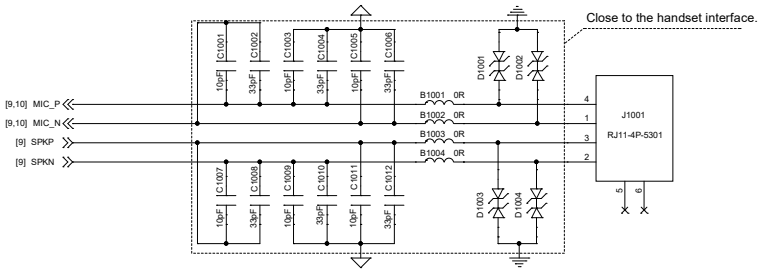
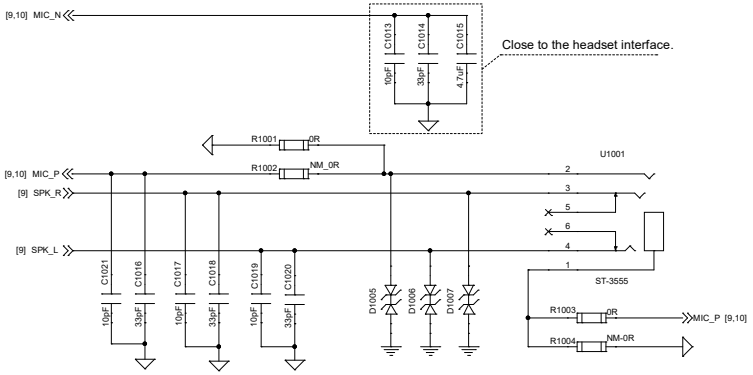
Audio Codec Interface Design

Handset Application



Headset Application



	CTIA	OMTP
R1002/R1004	NM	M
R1001/R1003	M	NM

NOTE:

1. The Codec analog output can drive handset and headset. For larger power loads such as loudspeaker, add an audio power amplifier in the design.
2. In handset applications, route the MIC and SPK signal traces as differential pairs.
3. In headset applications, route the MIC signal traces as a differential pair.
4. Surround all MIC and SPK signal traces with ground on the same layer and with ground planes above and below to minimize noise interference, such as clock and DC-DC signals.

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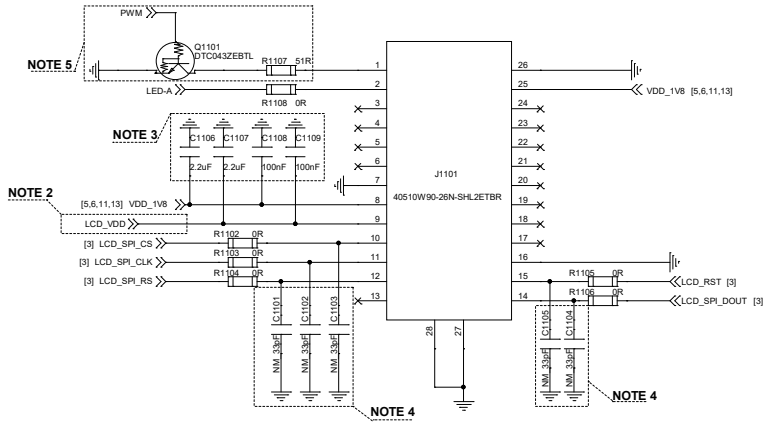
LCM & Camera Interfaces

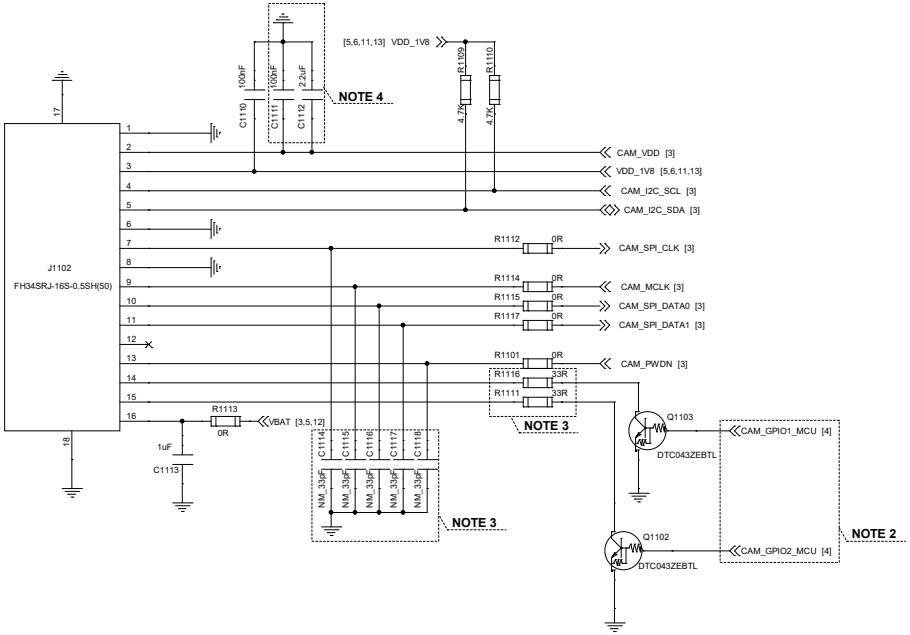
LCM Interface Design



NOTE:

1. LCM interface (pins 49–53, 78) is only supported by normal-voltage version, and the interface is optional.
   If you need this function, please contact Quectel Technical Support.
2. It is recommended to design the power supply of LCM interface by yourself.
3. To avoid abnormal LCM display caused by power fluctuation, it is recommended to mount filter capacitors.
4. Reserve 33 pF capacitors for the signal pins for debugging.
5. The LED-A backlight power supply should be designed by yourself. Select an appropriate resistor (R1107) based on the rated current of the digital transistor and the LED-A voltage value.

Camera Interface Design



NOTE:

1. Camera interface (pins 8, 54–58, 80, 81) is only supported by normal-voltage version, and the interface is optional.
   If you need this function, please contact Quectel Technical Support.
2. To control the cathode of the camera's positioning light, use CAM_GPIO1_MCU with a triode switching circuit. Similarly, CAM_GPIO2_MCU controls the cathode of the camera's supplement light. It is recommended to choose MCU's GPIO pins which are in pull-down status by default as these two control pins.
3. Reserve 33 pF capacitors for the signal pins to facilitate debugging. The values of current limiting resistors for the positioning light and supplement light (R1111 and R1116) should be adjusted based on the required brightness level.
4. Connect the capacitors (C1111 and C1112) of the CAM_VDD power supply directly to the GND layer.
   Failing to do so may result in power supply noise causing abnormalities such as white dots on the preview screen.

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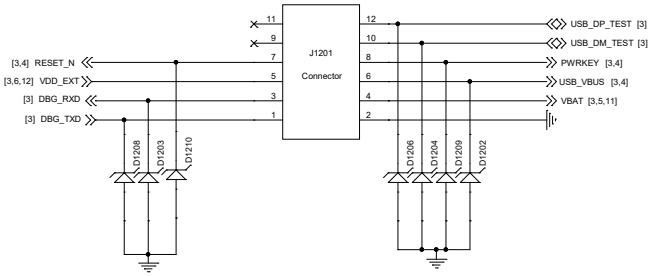
Other Designs

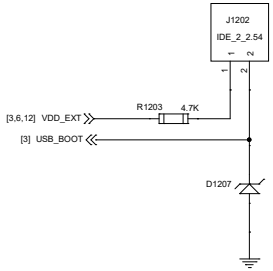
Reserved Test Points



NOTE:

1. Test points of USB interface must be reserved for firmware upgrade, software debugging and log output.
2. The junction capacitance of the ESD protection components on USB data traces should be less than 2 pF.
3. The debug UART interface supports a 1.8 V power domain. If your application operates at 3.3 V, use a voltage-level translator.
4. For the PWRKEY pin of nomal-voltage version: it is recommended to reserve a test point.
   For the PWRKEY pin of low-voltage version: keep it open.

Forced Download Interface



NOTE:

1. Make sure to reserve the forced download interface design and a test point must be reserved for USB_BOOT.
2. Before turning on the module, pull USB_BOOT up to VDD_EXT to activate the forced download mode.
   This mode enables firmware upgrades via the USB interface.

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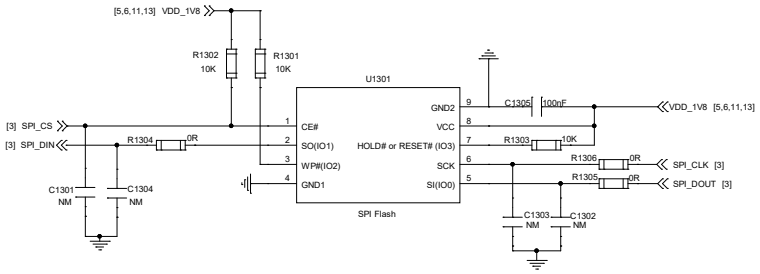
SPI (Master Mode)



NOTE:

1. The module supports SPI:

   (1) For the module of normal-voltage version, the SPI can be multiplexed from LCM interface (pins 50–53). For more details, see the GPIO configuration document of the module.

   (2) For the module of low-voltage version, the SPI is also supported. For more details, please contact Quectel Technical Support.

2. The module's SPI supports master mode only.

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