EC800E-CN QuecOpen Reference Design

LTE Standard Module Series

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Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2023-03-01	Maffie ZHANG	Creation of the document
1.0	2023-07-14	Maffie ZHANG	First official release

Contents

1 Reference Design

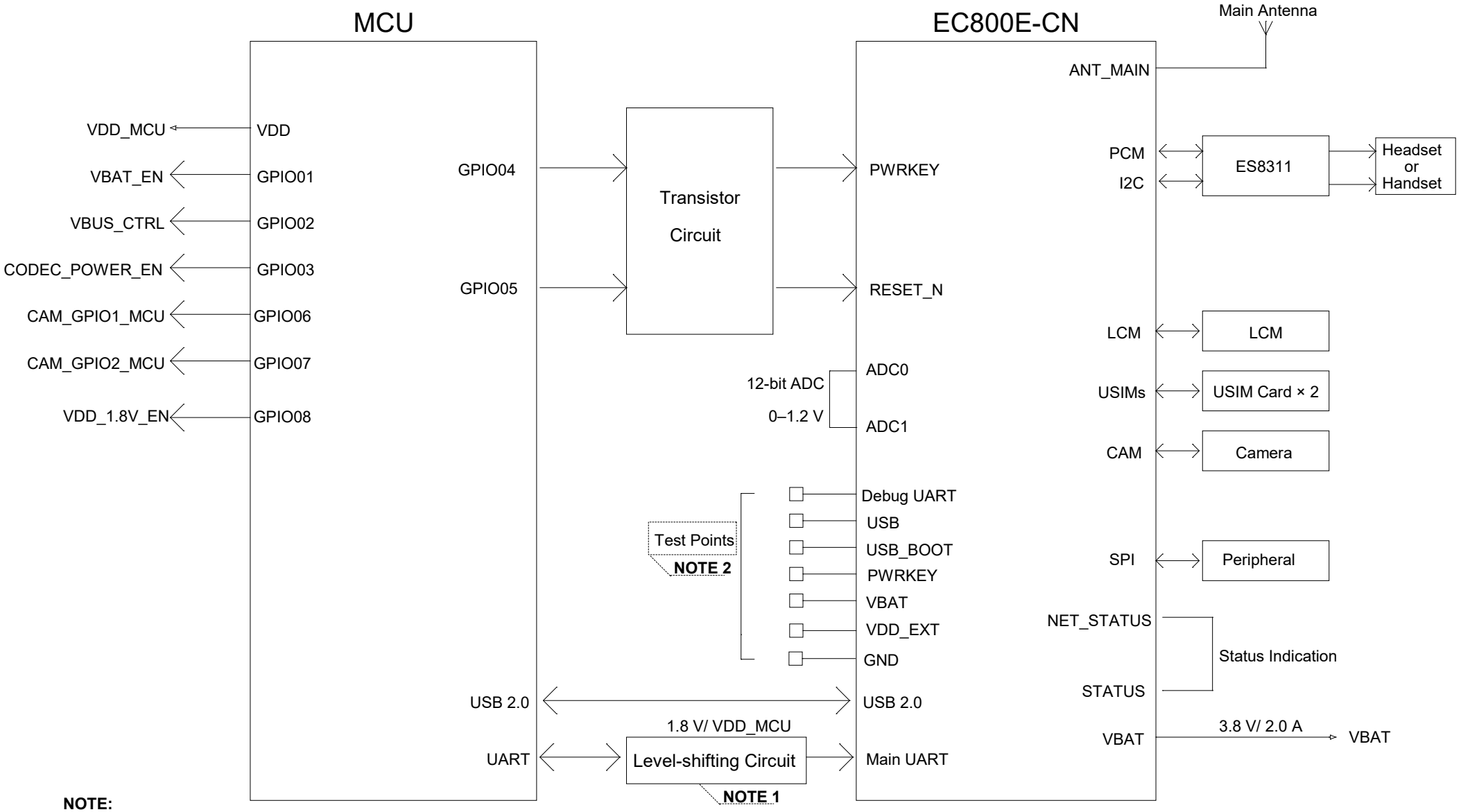
1.1. Introduction

This document provides the reference design for Quectel EC800E-CN QuecOpen® module. The reference design mainly includes block diagrams of power supply, UART interfaces, USIM interfaces, antenna interface, audio codec design, LCM interface, camera interface etc.

1.2. Schematics

The schematics illustrated in the following pages are provided for reference only.

Block Diagram



NOTE:

1. A transistor solution or an IC solution TXS0108EPWR provided by Texas Instruments is recommended.
2. Test points of USB_VBUS, USB_DP/DM, USB_BOOT must be reserved. It is recommended to reserve the test points of DBG_TXD/RXD, VDD_EXT, PWRKEY and VBAT.
3. Camera Interface (pins 8, 54–58, 80, 81), LCM interface (pins 49–53, 78) and USIM2 interface (pins 62–65) are optional.
   If you need these functions, please contact Quectel Technical Support.
4. The SPI interface is multiplexed from LCM interface pins.

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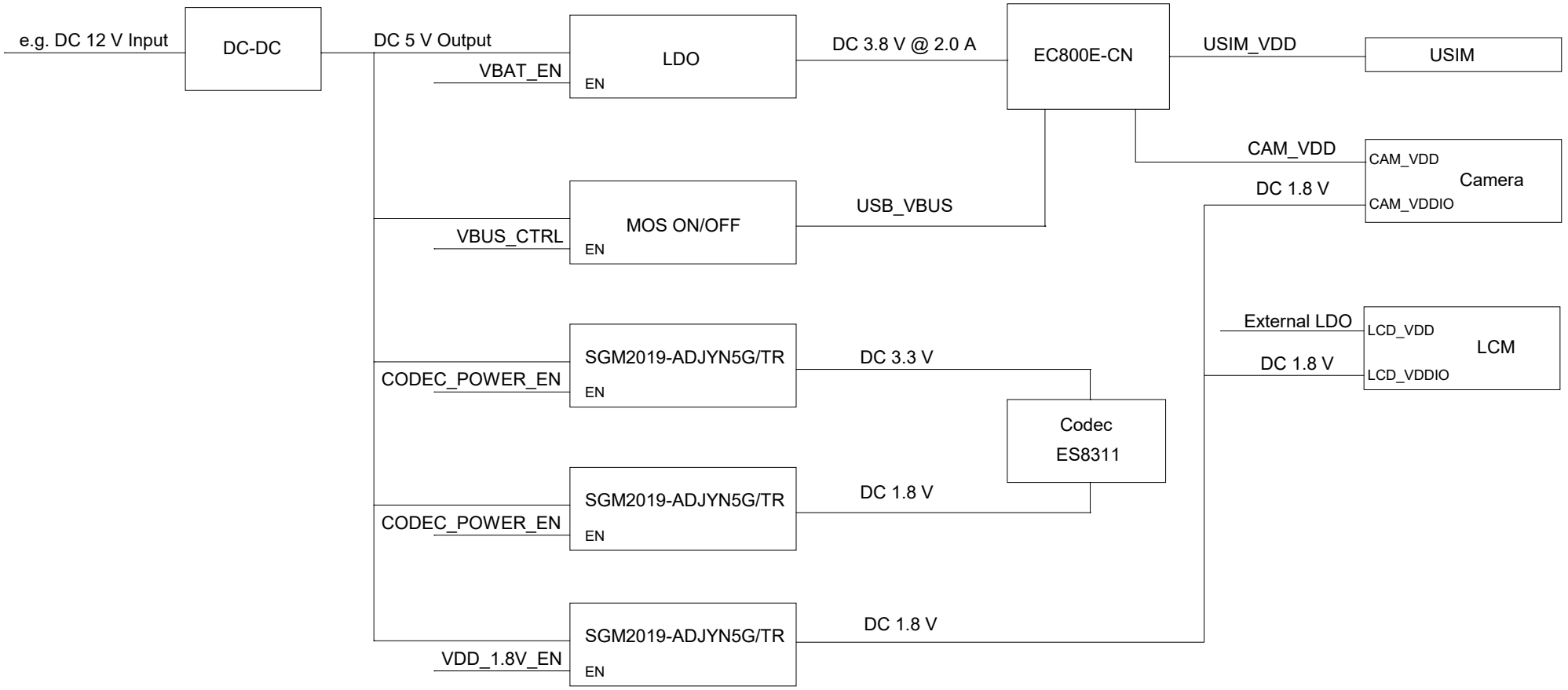
DATE: Friday, July 14, 2023	SHEET: 1 OF 12	

Power System Block Diagram



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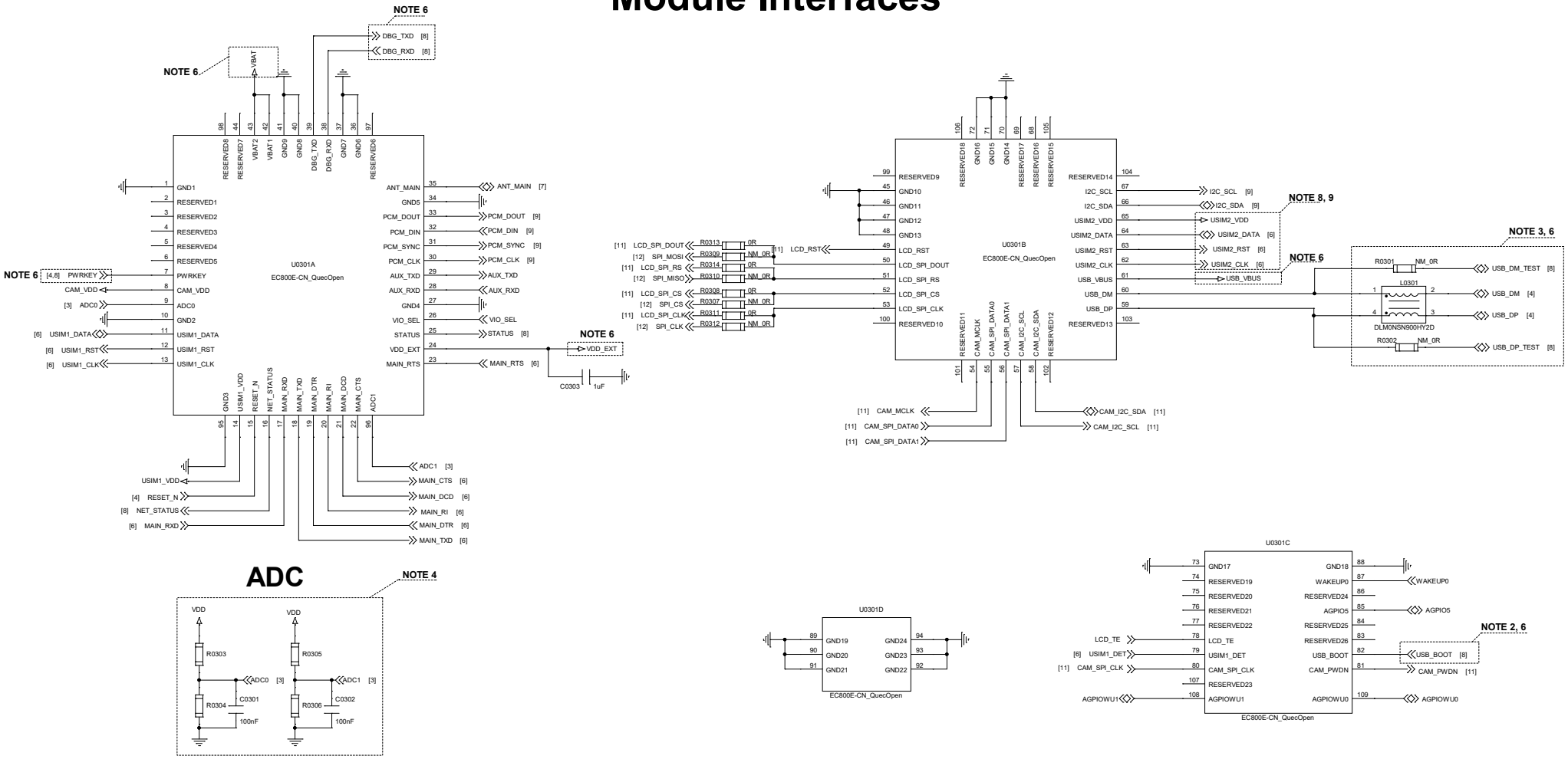
DATE: Friday, July 14, 2023	SHEET: 2 OF 12	

Module Interfaces



NOTE:

1. All GND pins should be connected to ground, and keep unused and RESERVED pins unconnected.
2. If the module does not need to enter emergency download mode, USB_BOOT cannot be pulled down to low level before the module successfully starts up.
3. A common mode choke L0301 is recommended to be added in series between the module and your MCU in order to suppress EMI spurious transmission, and it should be placed close to the module.
   Meanwhile, test points of USB interface must be reserved, which can be used for firmware upgrading. Keep extra stubs of the trace as short as possible.
   The two resistors R0301 and R0302 should be placed close to the module to ensure the integrity of the USB signals.
4. The voltage input range of ADC0 and ADC1 interfaces is 0–1.2 V. When the collected voltage is higher than 1.2 V, it is recommended to use the resistor divider circuit for ADC application.
   The divider resistor accuracy should be less than 1 %, and the resistance should not exceed 100 kΩ. It is recommended to reserve a 100 nF capacitor for the design.
5. Pins with wake-up interrupt: MAIN_DTR, MAIN_RXD, USIM1_DET, USB_VBUS, WAKEUP0, AGPIOWU0 and AGPIOWU1.
   For the version that VDD_EXT is powered down in sleep mode, these pins cannot be pulled up to VDD_EXT.
6. Test points of USB_VBUS, USB_DP/DM, USB_BOOT must be reserved. It is recommended to reserve the test points of DBG_TXD/RXD, VDD_EXT, PWRKEY and VBAT.
7. Ensure there is a complete reference ground plane below the module, and the gound plane should be placed as close to the module layer as possible.
   Other traces cannot be routed on the first layer below the module, and at least four-layer board design is recommended.
8. Camera Interface (pins 8, 54–58, 80, 81), LCM interface (pins 49–53, 78), USIM2 interface (pins 62–65), VIO_SEL (pin 26), WAKEUP0 (pin 87), AGPIO5 (pin 85), AGPIOWU0 (pin 109), AGPIOWU1 (pin 108) are optional.
   If you need these functions, please contact Quectel Technical Support.
9. The pins 62–64 of the USIM2 interface and the pins 55, 80 and 81 of the camera interface cannot be used at the same time.
10. For details about GPIO multiplexing function, refer to *Quectel_EC800E-CN_QuecOpen_GPIO_Configuration.*

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PROJECT: EC800E-CN QuecOpen	VER: V1.0	
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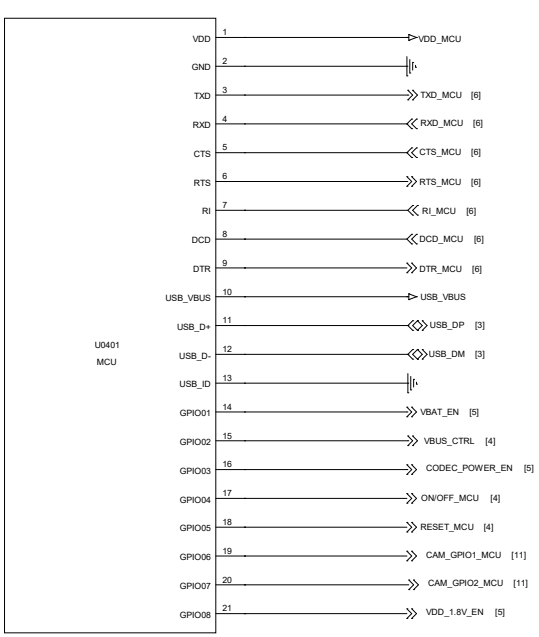
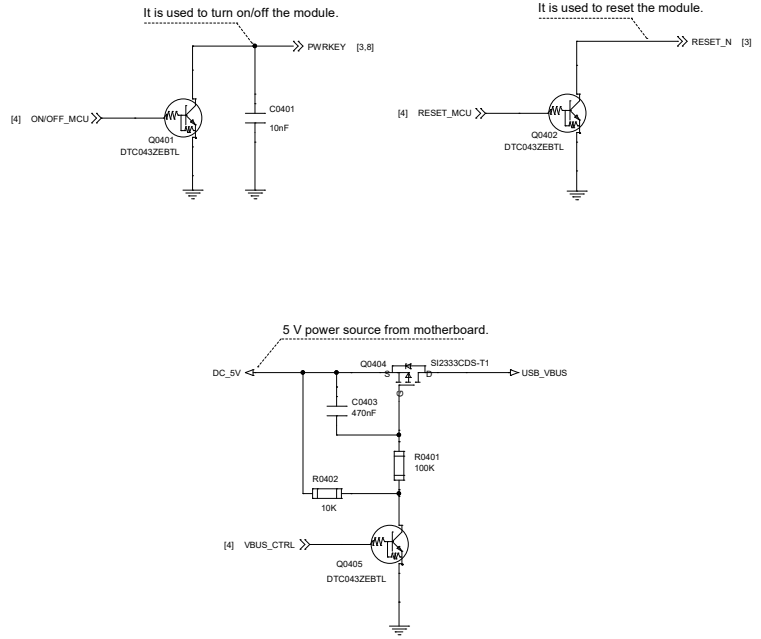
DATE: Friday, July 14, 2023	SHEET: 3 OF 12	

MCU Interfaces





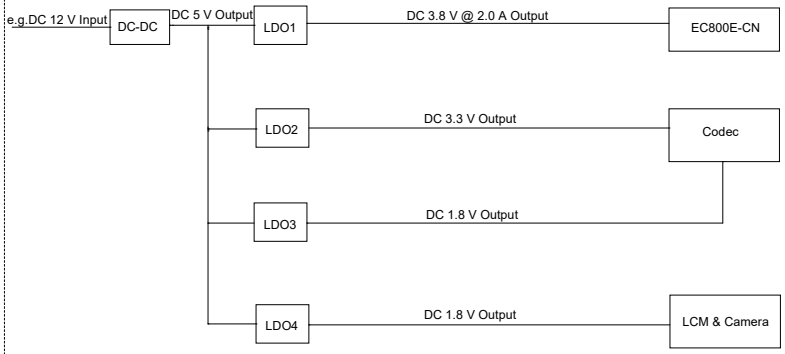
NOTE:

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V. If the power domain of GPIO interfaces of U0401 is also 1.8 V, then the related level-shifting circuit is not needed.
2. The USB interface of the module can only serve as a slave device, and supports full-speed and high-speed modes. To communicate with the USB interface, MCU needs to support USB host mode or OTG function.
   The USB_VBUS pin of the module should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the power supply of USB_VBUS.
3. The reset function of the module requires the PWRKEY and RESET_N pins to work together. See the hardware design document of the module.
4. It is recommended to select the MCU's default low-level GPIO pins as the control pins for the module's PWRKEY and RESET_N pins. Ensure that the load capacitance does not exceed 10 nF on PWRKEY and RESET_N pins.

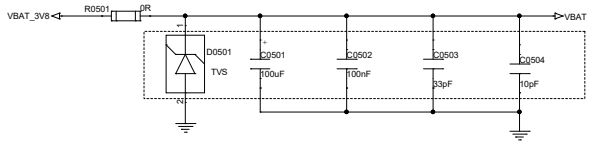
Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to 5.0 V, and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V to power the module, Codec, LCM and Camera.



VBAT Design

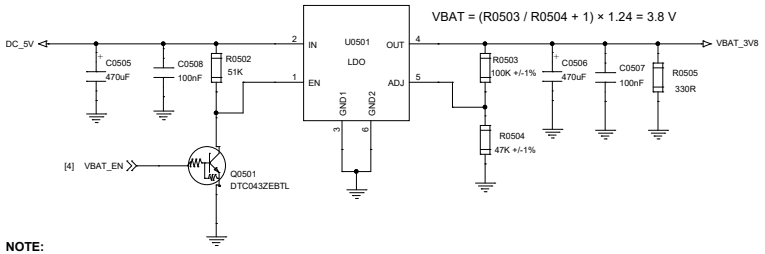


NOTE:

1. The power supply should be able to provide sufficient current of at least 2.0 A for the module.
2. The width of VBAT trace should be not less than 2 mm.
3. The recommended operating voltage of VBAT ranges from 3.3 V to 4.3 V, and the typical value is 3.8 V.

LDO Application

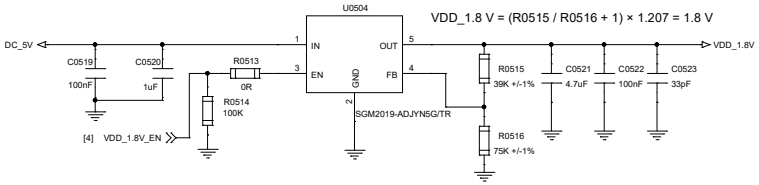
When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



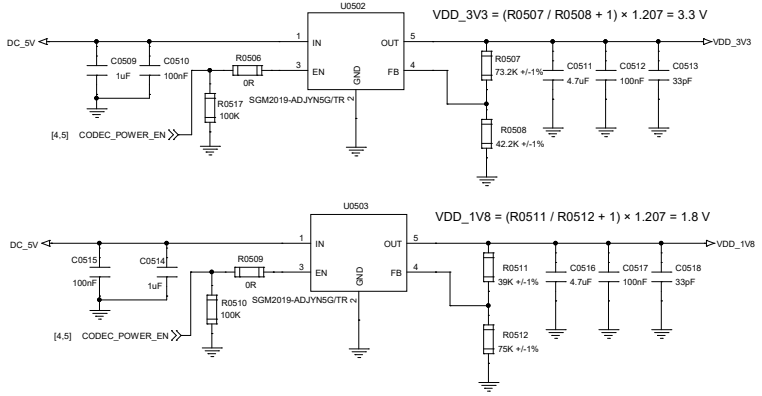
NOTE:

1. The recommended load current should be greater than 10 mA.
2. You can adjust related device parameters according to the actual design.

Power Supply for LCM & Camera Interfaces



Power Supply for PCM Codec



NOTE:

1. CODEC_POWER_EN is used to power on/off the VDD_1V8 and VDD_3V3 power supply.
2. For ES8311 codec, the power-on/off interval between 1.8 V and 3.3 V power supplies should not exceed 10 ms.

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PROJECT: EC800E-CN QuecOpen	VER: V1.0	
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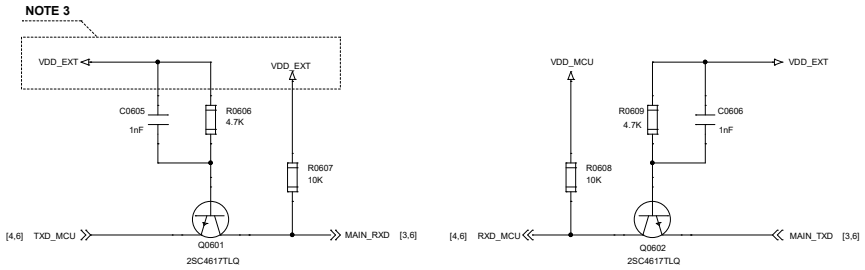
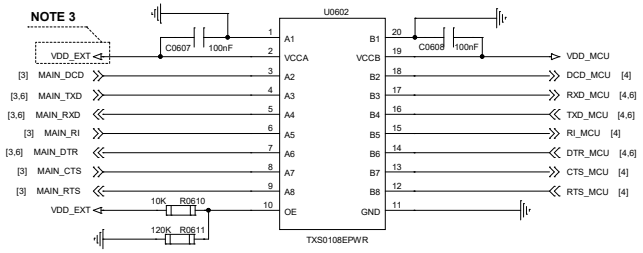
DATE: Friday, July 14, 2023	SHEET: 5 OF 12	

UART and USIM Interfaces

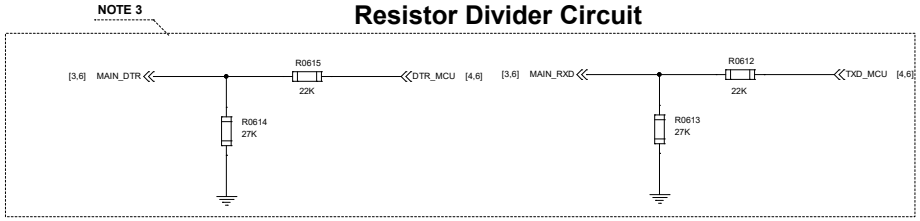
UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



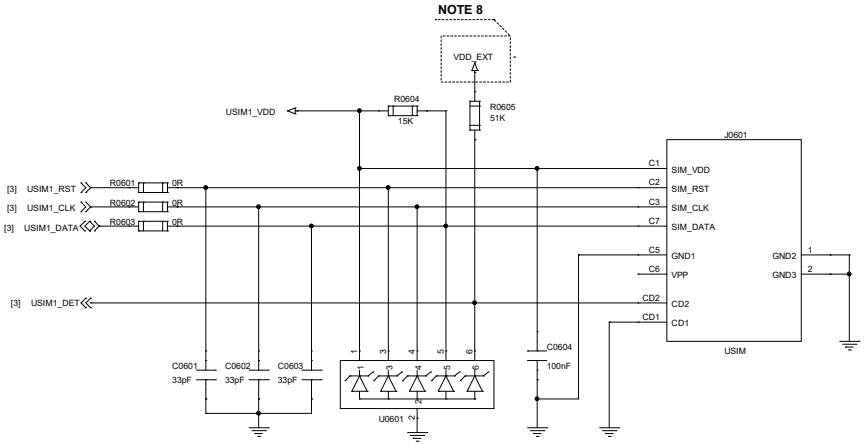
Resistor Divider Circuit



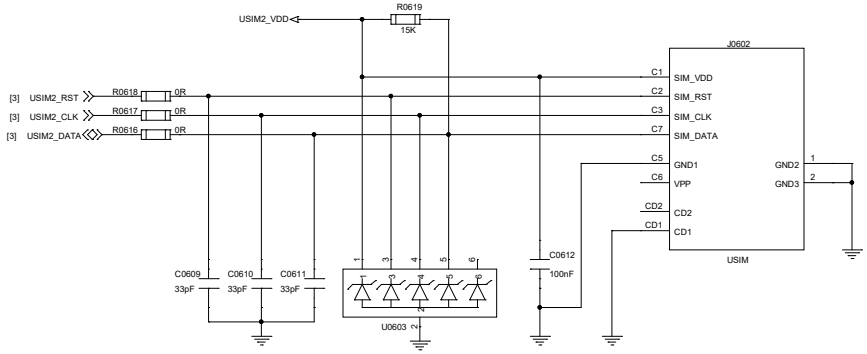
NOTE:

1. There are two level-shifting circuits: transistor solution and IC solution, and it is recommended to select the latter one.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, please refer to the datasheet of TXS0108EPWR.
3. For the version that VDD_EXT is not powered down in sleep mode, the pull-up power supply of MAIN_RXD and VCCA can be connected to VDD_EXT.
   For the version that VDD_EXT is powered down in sleep mode, VDD_EXT cannot be used as the pull-up power supply for MAIN_RXD and MAIN_DTR.
   So there are two options to choose from:
   a. Use an external 1.8 V power supply instead of VDD_EXT to connect to the pull-up power supply of MAIN_RXD and VCCA.
   b. MAIN_RXD and MAIN_DTR should be designed with resistor divider circuit. Pay attention to adjusting the resistance value of R0612–R0615 according to the actual situation.
4. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C0605 and C0606 of 1 nF can improve the signal quality.
5. If the level of the external host is 1.8 V and the module's MAIN_RXD and MAIN_TXD are directly connected to the host's TXD and RXD, the MAIN_TXD of the module should be pulled up to 1.8 V via a 10 kΩ resistor to prevent the host from receiving error messages when the module is in sleep mode.

USIM1 Interface Design



USIM2 Interface Design



NOTE:

1. USIM2 interface (pins 62–65) is optional. If you need this function, please contact Quectel Technical Support.
2. The pins 62-64 of the USIM2 interface and the pins 55, 80 and 81 of the camera interface cannot be used at the same time.
3. USIM2 interface of the module does not support hot-plug detection.
4. It is recommended to use U0601 and U0603 to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.
5. The pull-up resistors R0604 and R0619 can improve anti-jamming capability, and should be placed close to the USIM card connector.
6. R0601–R0603 and R0616–R0618 are used for debugging, and C0601–C0603 and C0609–C0611 are used for filtering out RF interference.
7. The capacitances of C0604 and C0612 should be less than 1 μF and they should be placed close to the USIM card connector.
8. For the version that VDD_EXT is powered down in sleep mode, the pull-up power supply of USIM1_DET needs to be connected to an external 1.8 V power supply.
   For the version that VDD_EXT is not powered down in sleep mode, the pull-up power supply of USIM1_DET can be connected to VDD_EXT.
9. If USIM1 and USIM2 interfaces are used at the same time, ensure that the voltage domain of the USIM interfaces is 1.8 V.

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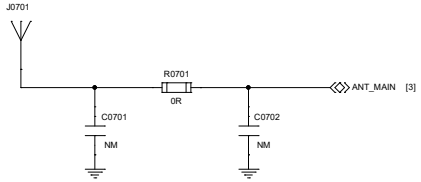
PROJECT: EC800E-CN QuecOpen		VER: V1.0
DRWAN BY: Maffie ZHANG	CHECKED BY: Woody WU	SIZE: A2
DATE: Friday, July 14, 2023	SHEET: 6 OF 12	

Antenna Interface



NOTE:

1. Use a Π-type matching circuit for the antenna interface.
2. The single-ended impedance of the RF antenna is 50 Ω, and the trace length should be as short as possible.

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PROJECT: EC800E-CN QuecOpen		VER: V1.0
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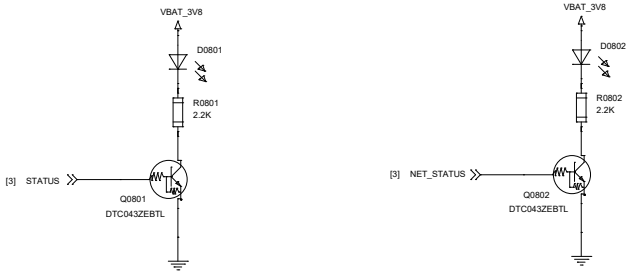
DATE: Friday, July 14, 2023	SHEET: 7 OF 12	

Other Designs

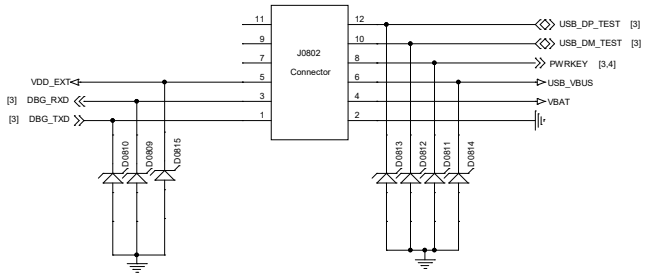
Indicators



NOTE:

1. For more details about STATUS and NET_STATUS, see the hardware design document of the module.
2. If the low power consumption is required when your device is in sleep, replace the power supply VBAT_3V8 of the STATUS and NET_STATUS indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

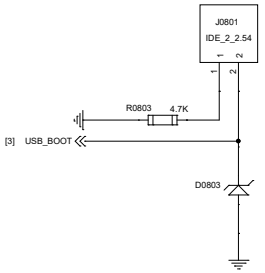
Reserved Test Points



NOTE:

1. Test points of USB interface must be reserved for firmware upgrade, software debugging and log output to analyze your problems.
2. The junction capacitance of the ESD protection components on USB data traces should be less than 2 pF.
3. The debug UART interface supports 1.8 V power domain, and a voltage-level translator should be used if the power domain of your application is 3.3 V.

Emergency Download Mode



NOTE:

1. Make sure to reserve the USB_BOOT interface design and a test point must be reserved for USB_BOOT.
2. Pull down USB_BOOT to GND before the module starts up, and the module will enter emergency download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

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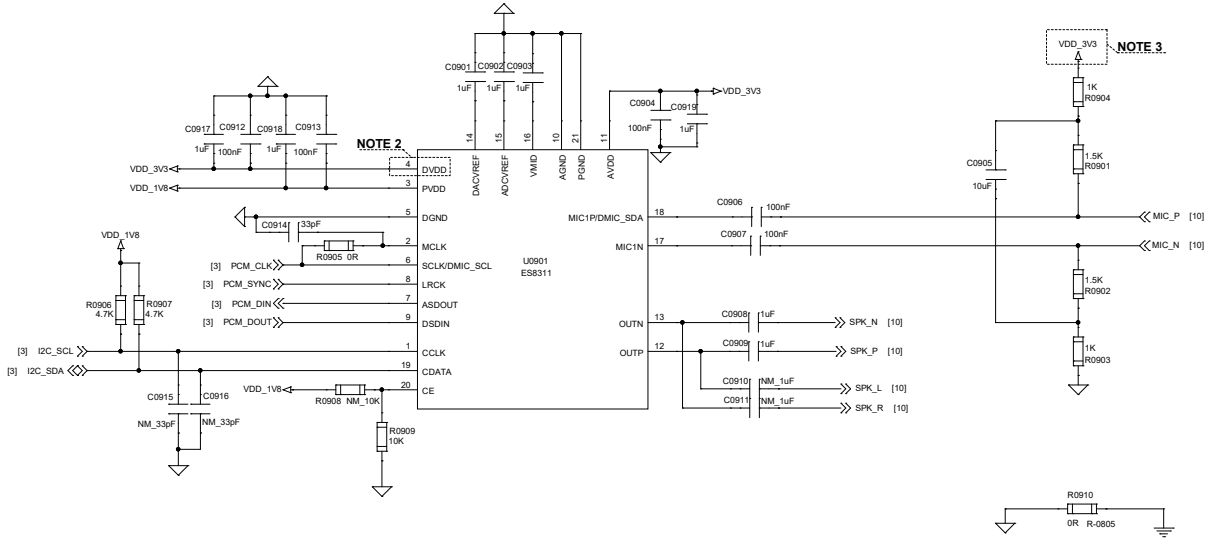
PROJECT: EC800E-CN QuecOpen		VER: V1.0
DRWAN BY: Maffie ZHANG	CHECKED BY: Woody WU	SIZE: A2
DATE: Friday, July 14, 2023	SHEET: 8 OF 12	

Audio Codec Design (ES8311)



NOTE:

1. ES8311 power-up/down sequences: AVDD, PVDD and DVDD are powered on and off at the same time, or with the interval less than 10 ms.
2. When the sampling frequency is 8 kHz and the clock frequency is 512 kHz, DVDD must be connected to 1.8 V.
3. The bias voltage needs to be stable and the ripple should be as small as possible.
4. Pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805.
   For more details, see the Sheet "Audio Codec Interface".
5. For more details, see the datasheet of ES8311.

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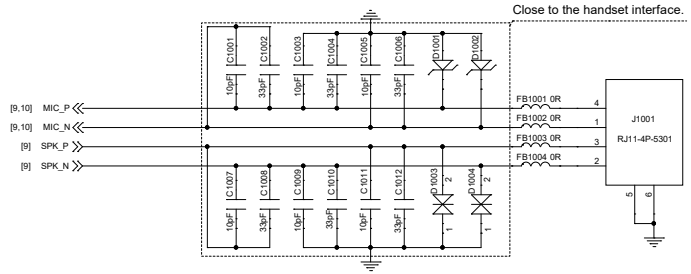
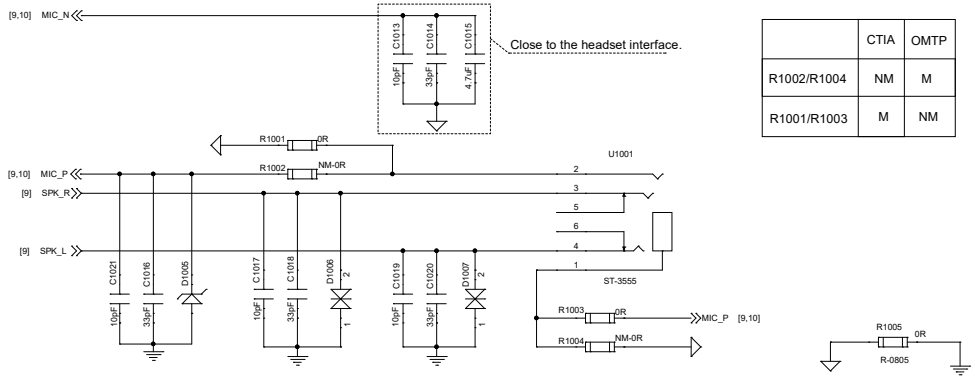
PROJECT: EC800E-CN QuecOpen		VER: V1.0
DRWAN BY: Maffie ZHANG	CHECKED BY: Woody WU	SIZE: A2
DATE: Friday, July 14, 2023	SHEET: 9 OF 12	

Audio Codec Interface

Handset Application



Headset Application



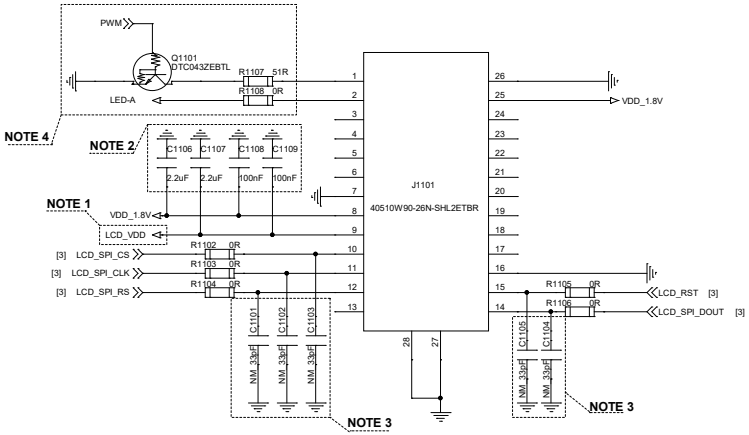
	CTIA	OMTP
R1002/R1004	NM	M
R1001/R1003	M	NM

NOTE:

1. The Codec analog output can drive handset and headset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.
2. In handset applications, route the MIC and SPK signal traces as differential pairs respectively.
3. In headset applications, route the MIC signal traces as a differential pair.
4. All MIC and SPK signal traces should be surrounded with ground on the layer and with ground planes above and below, and far away from noise such as clock and DC-DC signals.
5. Pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805 (short-circuit through single point grounding).

LCM & Camera Interfaces

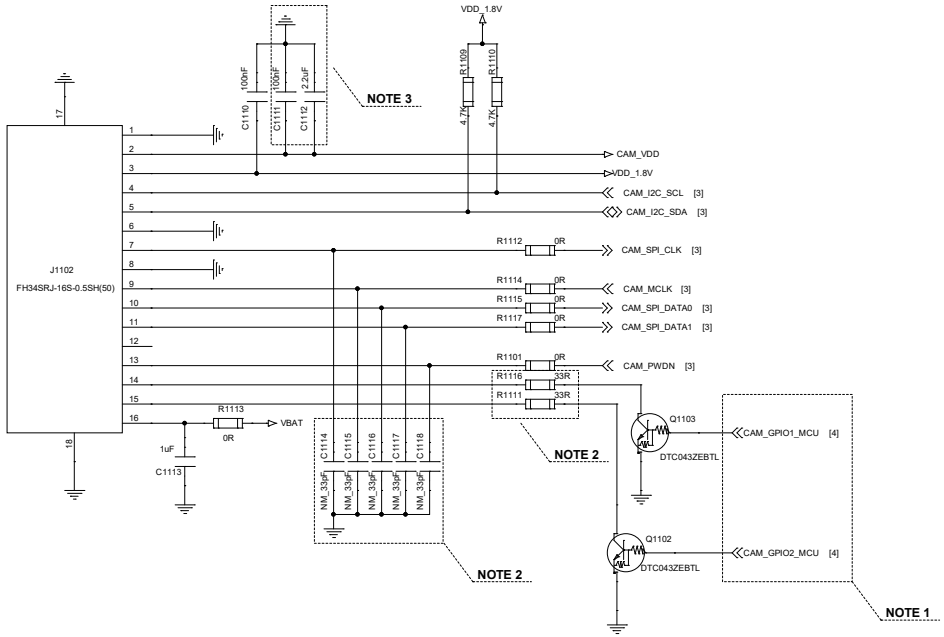
LCM Interface Design



NOTE:

1. It is recommended to design the power supply of LCM interface by yourself.
2. To avoid abnormal LCM display caused by power fluctuation, it is recommended to mount filter capacitors.
3. The 33 pF capacitors of the signal pins should be reserved, and can be used according to the actual debugging situation.
4. The LED-A backlight power supply is designed by youself, and you can select the approriate resistor (R1107) according to the triode rated current and LED-A voltage value.
5. LCM interface (pins 49–53, 78) is optional. If you need this function, please contact Quectel Technical Support.

Camera Interface Design



NOTE:

1. By controlling the triode switching circuit, CAM_GPIO1_MCU controls the cathode of the positioning light of the camera, and CAM_GPIO2_MCU controls the cathode of the supplement light of the camera.
   It is recommended to select default pull-down GPIO pins as the two control pins.
2. The 33 pF capacitors of the signal pins should be reserved, and can be used according to the actual debugging situation.
   The values of current limiting resistors of positioning light and supplement light (R1116 and R1111) should be varied according to the required brightness.
3. The capacitors (C1111 and C1112) of the CAM_VDD power supply should be connected to the GND layer directly.
   Otherwise, the power supply noise may lead to abnormalities such as white dots on the preview screen.
4. Camera interface (pins 8, 54–58, 80, 81) is optional. If you need this function, please contact Quectel Technical Support.

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PROJECT: EC800E-CN QuecOpen		VER: V1.0
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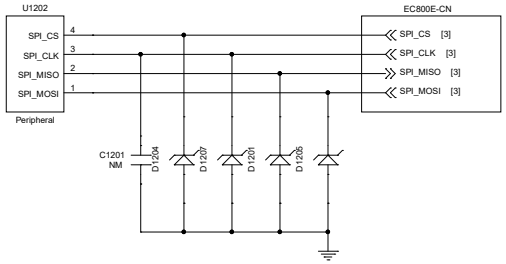
DATE: Friday, July 14, 2023	SHEET: 11 OF 12	

SPI Interface (Master Mode)



NOTE:

The SPI interface is multiplexed from LCD_SPI_RS, LCD_SPI_CS, LCD_SPI_DOUT and LCD_SPI_CLK.

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DATE: Friday, July 14, 2023	SHEET: 12OF 12	