EC600U Series QuecOpen Reference Design

LTE Standard Module Series

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Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2021-07-28	Manli CHEN	Creation of the document
1.0	2021-08-24	Manli CHEN	First official release
1.1	2022-01-28	Manli CHEN	1. Added the note on I2C interface (Sheet 8). 2. Updated the note on ESD protection components (Sheet 9). 3. Changed the unidirectional TVS diodes to bidirectional ones (Sheet 10). 4. Updated the formation of matrix keypad to 5 × 6 (Sheet 13).
1.2	2022-08-22	Denny QIN	1. Selected pin names have been updated: Pin 64: from LCD_SPI_RST to LCD_RST; Pin 65: from LCD_CS to LCD_SPI_CS (Sheet 3). 2. Added ADC voltage divider circuit and NOTE 4, and a TVS on VDD_EXT and NOTE 8 (Sheet 3). 3. Added the circuit for waking up the module from PSM (Sheet 4). 4. Added the design for camera MIPI (Sheet 8). 5. Changed the position of TVS diodes of the handset circuit (Sheet 10). 6. Added filter capacitors for LCD_VDDIO (Sheet 12). 7. Added the design for LCM MIPI (Sheet 12).

1.3	2023-01-05	Denny QIN	1. Updated the default function of pins 39, 40, 48–51, 53 (MAIN_DTR, MAIN_RI, MAIN_DCD, WAKEUP_IN, AP_READY, W_DISABLE#, SLEEP_IND) to GPIO and deleted related reference designs. 2. Updated the description on reserved test points for USB interface, debug UART and UART2_RTS (Sheets 3 and 15). 3. Added a note on R0207 resistance selection in USB_BOOT reference design (Sheet 4). 4. Added the description on VBAT voltage requirement in VBAT design (Sheet 5). 5. Added the description on reserved test points for USB_BOOT, RESET_N and VDD_EXT (Sheet 15). 6. Added Note 4 on signal trace requirement of external flash interface (Sheet 16). 7. Updated the maximum output current of SDIO_VDD to 150 mA; Updated the recommended resistance of pull-up resistors R1504–R1508 to 4.7 kΩ; Updated the recommended resistance of resistor R1510 on SDIO1_CMD trace to 33 Ω (Sheet 17).

Contents

1 Reference Design

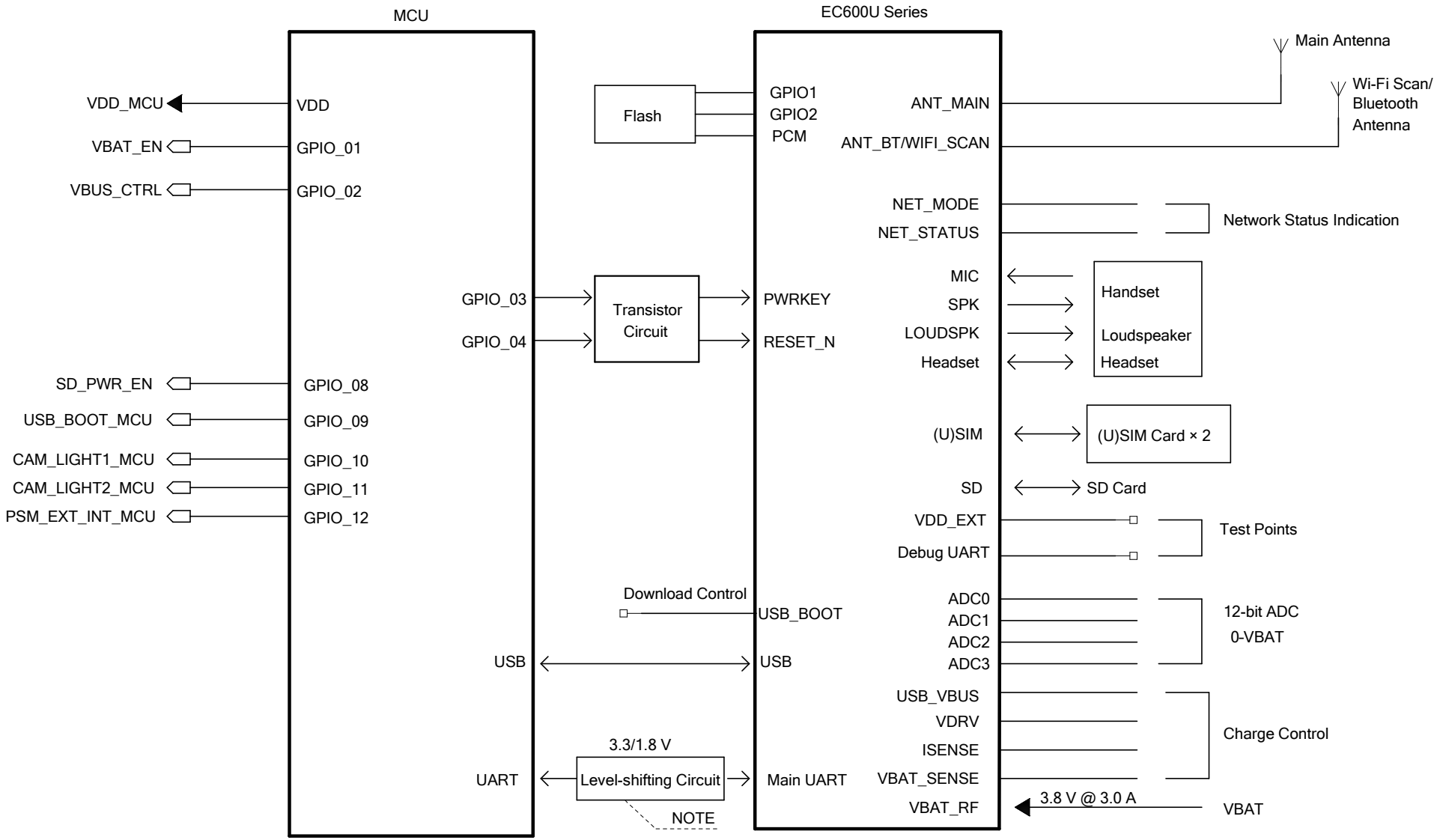
1.1. Introduction

This document provides the reference design for Quectel EC600U series QuecOpen® module. This reference design mainly includes block diagrams of module design, power supply, antenna interfaces, (U)SIM interfaces, camera interface, analog audio interfaces, UART, LCM interface, matrix keypad, external flash interface, SD card interface, and indicators.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Reference Design Block Diagram



NOTE:

A level-shifting circuit with a transistor or a voltage-level translator TXS0104EPWR provided by Texas Instruments is recommended.

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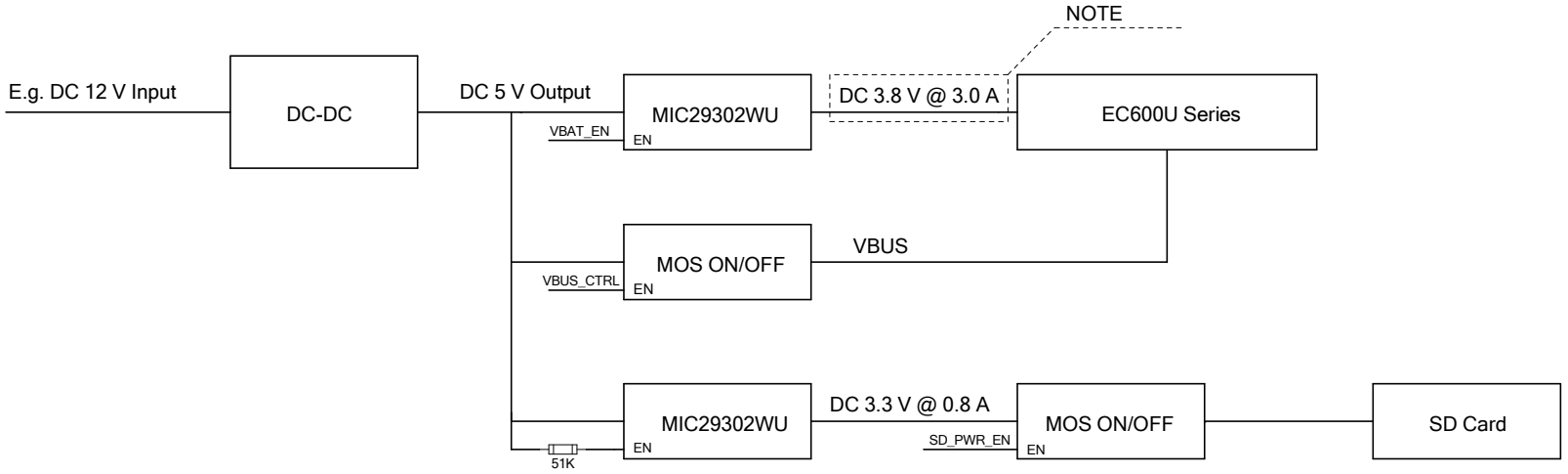
Power Supply Block Diagram



NOTE:

The power supply for EC600U-CN should be at least 2 A of current and at least 3 A of current for EC600U-EU.

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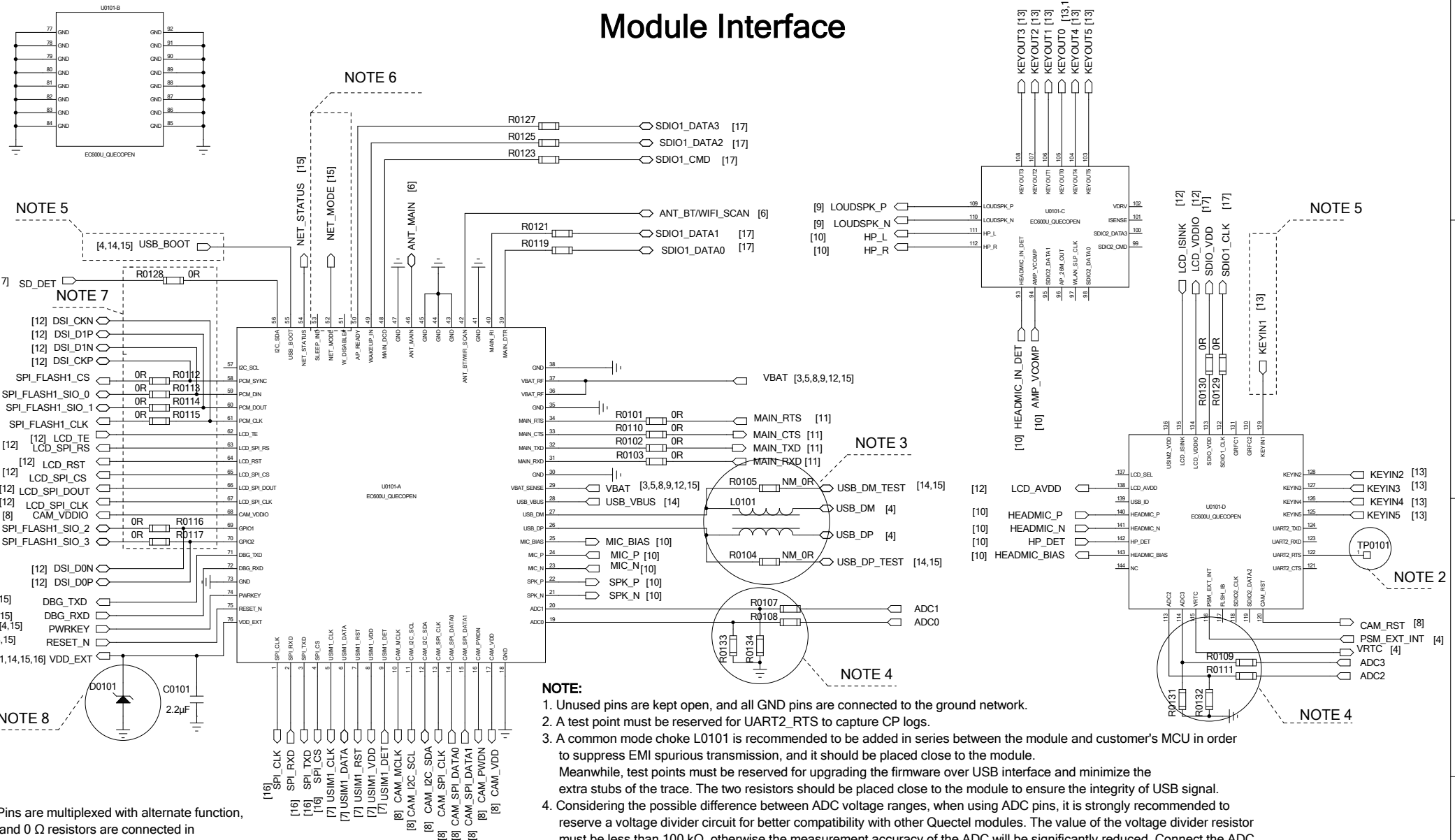
Module Interface



NOTE:

1. Unused pins are kept open, and all GND pins are connected to the ground network.
2. A test point must be reserved for UART2_RTS to capture CP logs.
3. A common mode choke L0101 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission, and it should be placed close to the module. Meanwhile, test points must be reserved for upgrading the firmware over USB interface and minimize the extra stubs of the trace. The two resistors should be placed close to the module to ensure the integrity of USB signal.
4. Considering the possible difference between ADC voltage ranges, when using ADC pins, it is strongly recommended to reserve a voltage divider circuit for better compatibility with other Quectel modules. The value of the voltage divider resistor must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced. Connect the ADC pins in series with a 1 kΩ resistor when the divider circuit is not used.
5. Do not pull up KEYIN1 before turning on the module. Do not pull up USB_BOOT before turning on the module if emergency download function is not required.
6. There are hardware conflicts between pins 51-53 and 145-147. If pins 145-147 of (U)SIM2 interface are used, pins 51-53 must be kept unconnected; if pins 51-53 are used, that is, the (U)SIM2 interface is not used, pins 145-147 must be kept unconnected. (U)SIM2 is optional. Please note that the software for using one (U)SIM card is different from that for using dual (U)SIM operation. Please consult Quectel Technical Support for more information about how to use (U)SIM2.
7. Pins are multiplexed with alternate function, and 0 Ω resistors are connected in series for the selection of functions in compatible design.
8. To offer good ESD protection, it is recommended to add a TVS on VDD_EXT trace.
9. MAIN_DTR, MAIN_RI, MAIN_DCD WAKEUP_IN, AP_READY, W_DISABLE#, and SLEEP_IND do not have the functions described by the pin names and their default functions are GPIOs.

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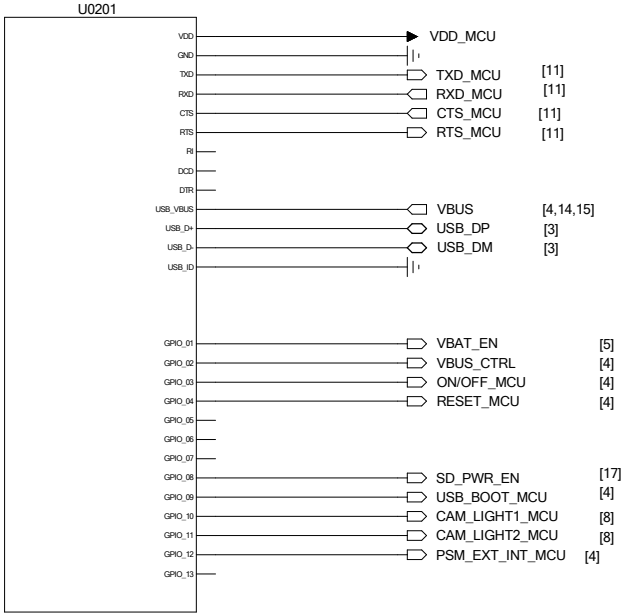
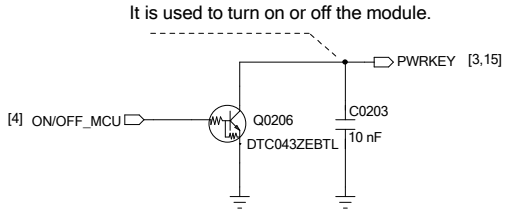
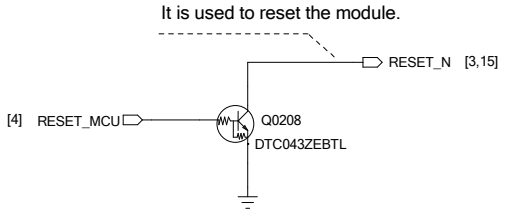
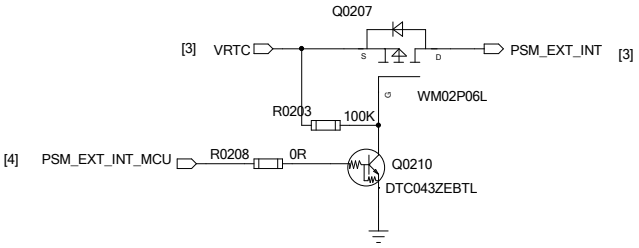
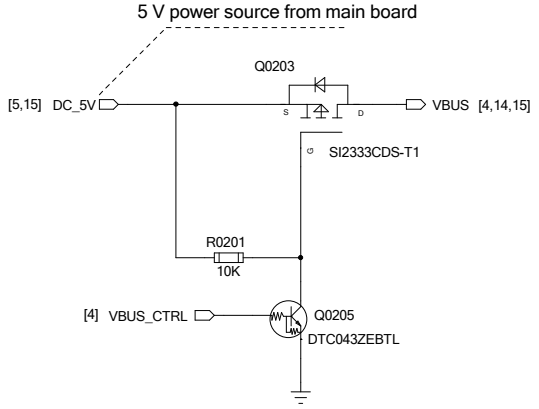
MCU Interface

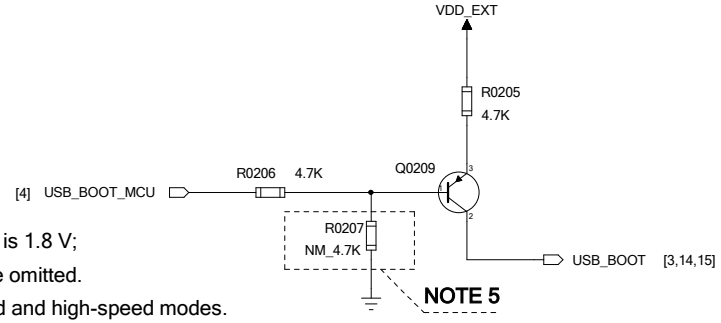












NOTE:

1. U0201 represents customer's MCU. The power domain of GPIO interfaces of EC600U series module is 1.8 V; if the GPIO interfaces of U0201 share the same power domain, the related level-shifting circuit can be omitted.
2. The USB 2.0 interface of the module can only be used in the USB salve mode and supports full-speed and high-speed modes. To communicate with the USB interface, MCU needs to support USB host mode or USB OTG. The USB_VBUS pin of the module should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the default low-level GPIO pins of MCU as the control pins for PWRKEY and RESET_N of the module. Ensure that the maximum load capacitance of PWRKEY and RESET_N does not exceed 10 nF.
4. To prevent the module from staying in download mode due to that the triode Q0209 conducts after the MCU is powered on, the USB_BOOT_MCU pin needs to be at high level by default when the MCU is powered on. For the same purpose, if the triode control method is not used, the method of reserved pins or key press can be used.
5. The R0207 resistance value is selected according to the level of the USB_BOOT_MCU pin.

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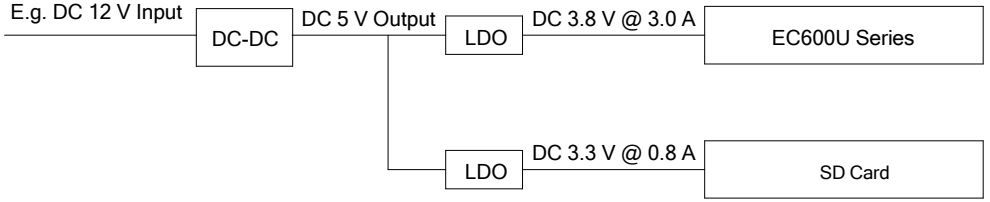
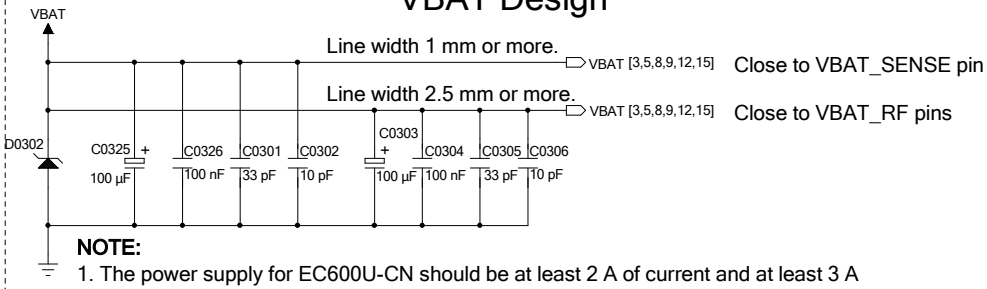
Power Supply Design

DC-DC Application

It is used when the input voltage is above 7.0 V. Use a DC-DC converter to convert a high input voltage to a 5.0 V output, and then use LDO ICs to convert to 3.8 V and 3.3 V for powering the module and SD card respectively.



VBAT Design

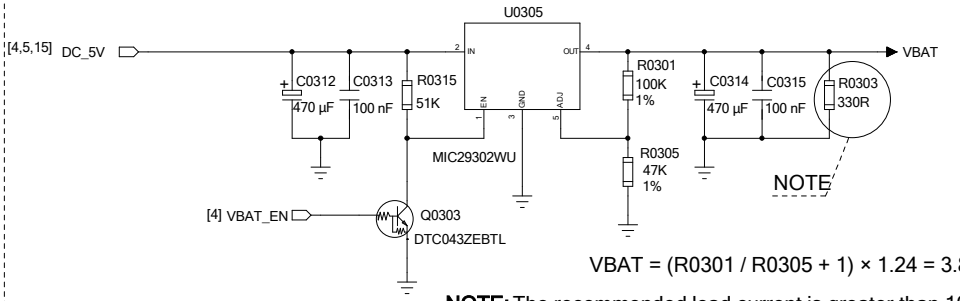


NOTE:

1. The power supply for EC600U-CN should be at least 2 A of current and at least 3 A of current for EC600U-EU.
2. VBAT traces should be routed in a star configuration to VBAT_SENSE and VBAT_RF pins.
3. The recommended operating voltage of VBAT is 3.3-4.3 V.
4. If you disconnect the VBAT power supply, ensure that the VBAT voltage is less than 0.5 V before power-on.

LDO Application

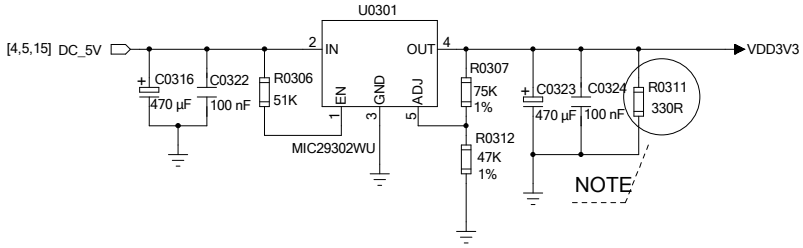
It is used when the input voltage is below 7.0 V. Use an LDO IC to convert the input voltage to 3.8 V.



VBAT = (R0301 / R0305 + 1) × 1.24 = 3.88 V

NOTE: The recommended load current is greater than 10 mA.

Power Supply for SD Card



VDD3V3 = (R0307 / R0312 + 1) × 1.24 = 3.3 V

NOTE: The recommended load current is greater than 10 mA.

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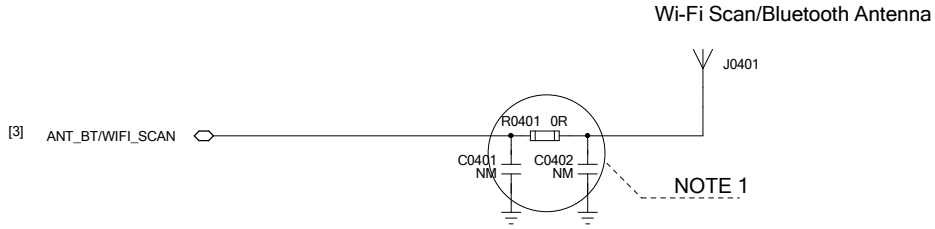
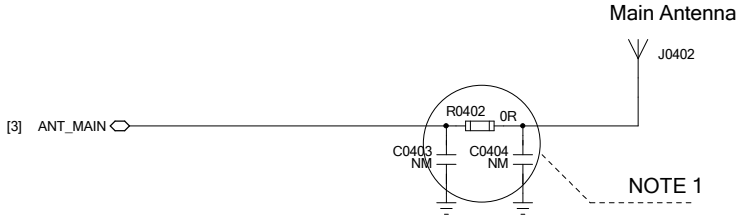
Antenna Interface Design





NOTE:

1. It is highly recommended to reserve a Π type matching circuit to facilitate future debugging.
2. The single-ended impedance of the RF antenna is 50 Ω.

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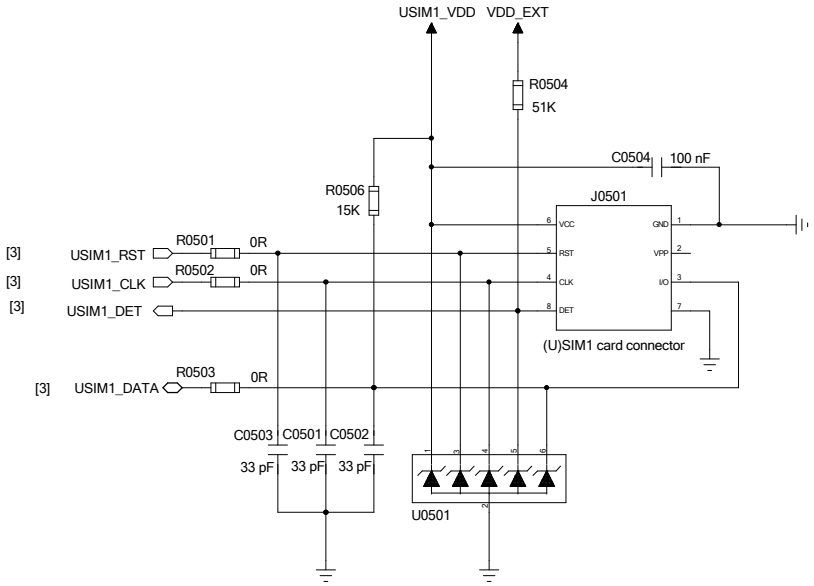
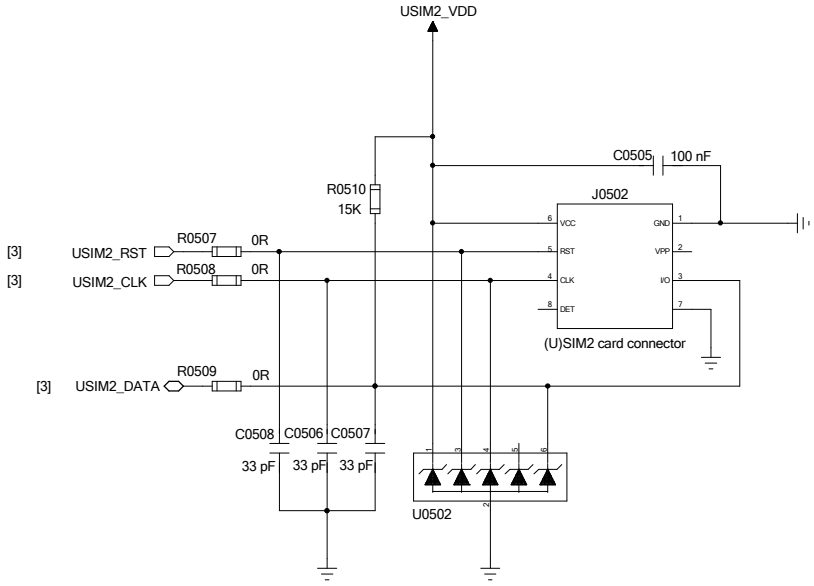
(U)SIM Interface Design

(U)SIM1 Interface



(U)SIM2 Interface



NOTE:

1. U0501 and U0502 are recommended to be used to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.
2. The pull-up resistors R0506 and R0510 can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.
3. R0501-R0503 and R0507-R0509 are used for debugging. C0501-C0503 and C0506-C0508 are used for filtering out RF interference.
4. The capacitance of C0504 and C0505 should be less than 1 μF and they should be placed close to the (U)SIM card connector.
5. The GND of the (U)SIM card connector is recommended to be connected to the GND layer of customer's PCB directly.
6. The (U)SIM2 interface of the module does not support hot-plug detection.
7. For more information about the layout of (U)SIM interfaces, please refer to *Quectel_EC600U_Series_QuecOpen_Hardware_Design.*

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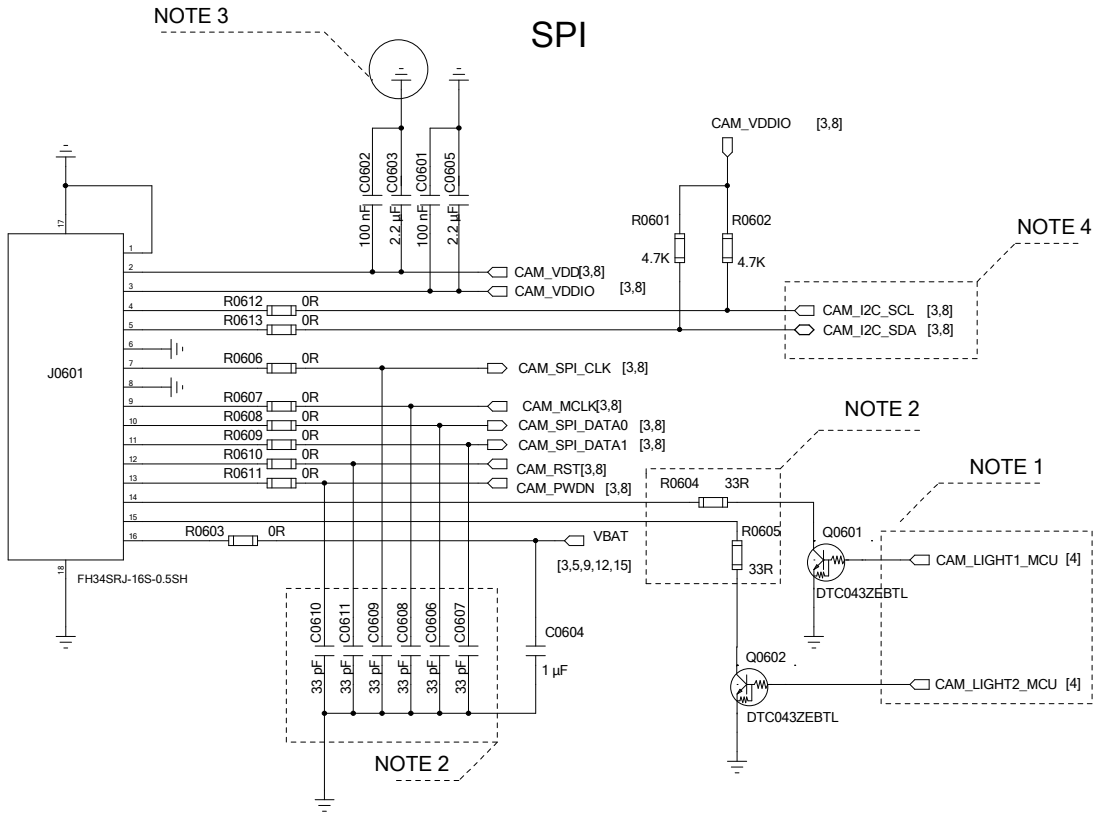
Camera Interface Design

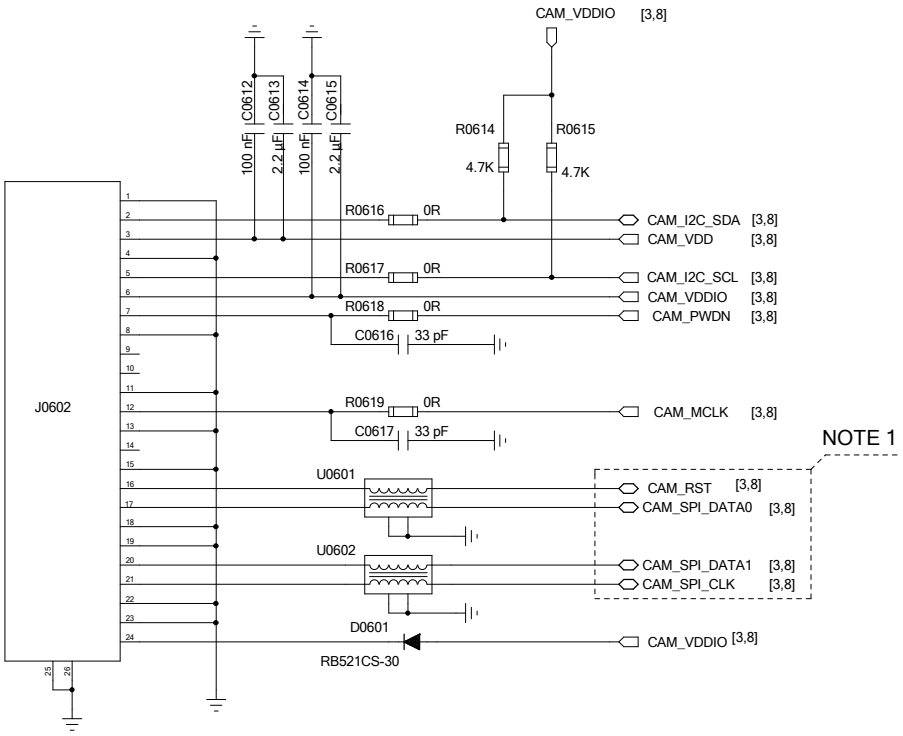
SPI



NOTE:

1. CAM_LIGHT1_MCU controls the cathode of the position lamp of the camera by controlling the triode switching circuit; CAM_LIGHT2_MCU controls the cathode of the fill light of the camera by controlling the triode switching circuit. Choose GPIO pins with default pull-down status as CAM_LIGHT1_MCU and CAM_LIGHT2_MCU.
2. The 33 pF capacitors of the signal pins are reserved, and they are used according to the actual debugging situation. The values of current limiting resistors of position lamp and fill light, R0604 and R0605, should be varied according to brightness requirements.
3. The capacitors of the CAM_VDD power supply should be connected to the GND layer directly, otherwise there may be power noise leading to abnormalities such as white dots on the preview screen.
4. If the camera interface is not required, CAM_I2C_SCL and CAM_I2C_SDA can be used as an I2C interface to connect other peripherals.

MIPI



NOTE:

1. CAM_RST can be multiplexed as the CSI_CKN function of MIPI.
   CAM_SPI_DATA0 can be multiplexed as the CSI_CKP function of MIPI.
   CAM_SPI_DATA1 can be multiplexed as the CSI_D0N function of MIPI.
   CAM_SPI_CLK can be multiplexed as the CSI_D0P function of MIPI.
2. The position lamp and fill light can be designed by yourself.

NOTE:

You can use either SPI or MIPI in the camera interface design, and it is recommended to choose the former.

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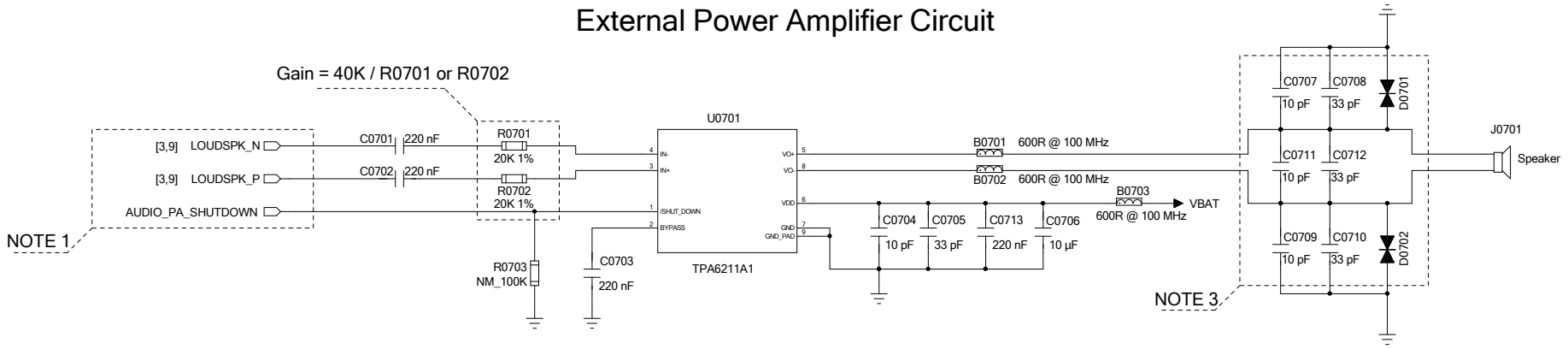
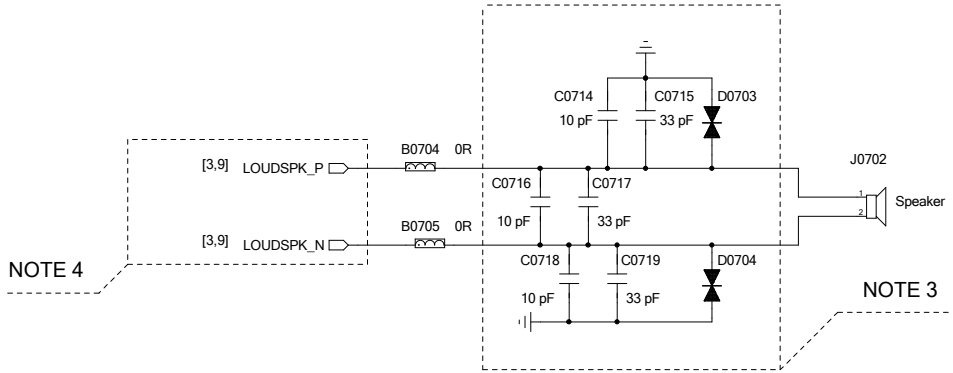
Analog Audio Design (Loudspeaker)

External Power Amplifier Circuit



Internal Power Amplifier Circuit



NOTE:

1. LOUDSPK_N and LOUDSPK_P are differential outputs. To eliminate POP, it is recommended to choose one of the GPIO pins of the module as the AUDIO_PA_SHUTDOWN pin of the power amplifier. For details, please contact Quectel Technical Support.
2. Choose the audio power amplifier with appropriate power according to actual needs.
3. Place filter capacitors and ESD protection components close to the speaker. Choose ESD protection components according to the output voltage amplitude of the PA. To avoid damages to the ESD protection components, please ensure that the output voltage amplitude of the PA is within their maximum reverse working voltage under normal working conditions.
4. The module has an internal power amplifier, of which the maximum drive power is 800 mW (8 Ω load) when set to Class D, and 500 mW (8 Ω load) when set to Class AB. The default configuration is Class AB.

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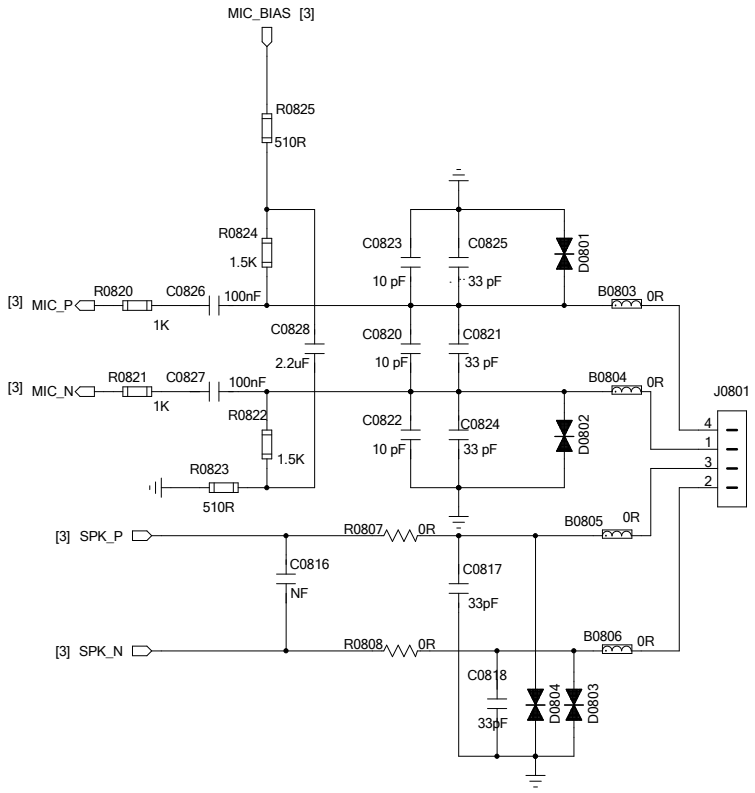
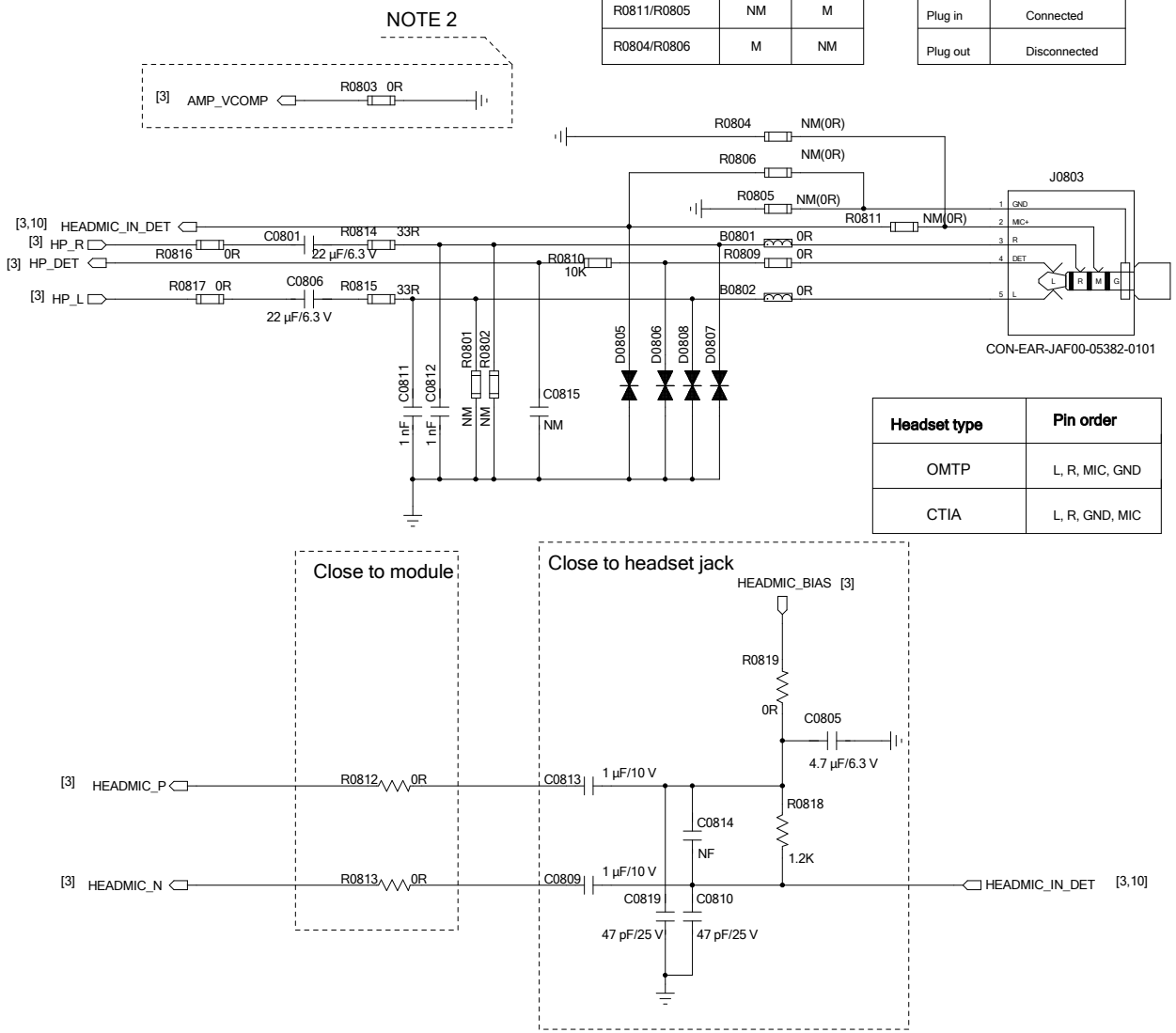
Analog Audio Design

Handset (Microphone and Receiver)



Headset Jack



NOTE:

1. Both the MIC and SPK signal traces need to be routed as differential pairs. All MIC and SPK signal traces should be surrounded with ground on the layer and with ground planes above and below, and far away from noise sources.
2. AMP_VCOMP pin is the dedicated GND pin for headset. It should be traced between the left and right channels, and connected to the GND of the headset jack, and then directly connected to the main GND layer. Be sure to isolate it from other GNDs to avoid noise interferences.

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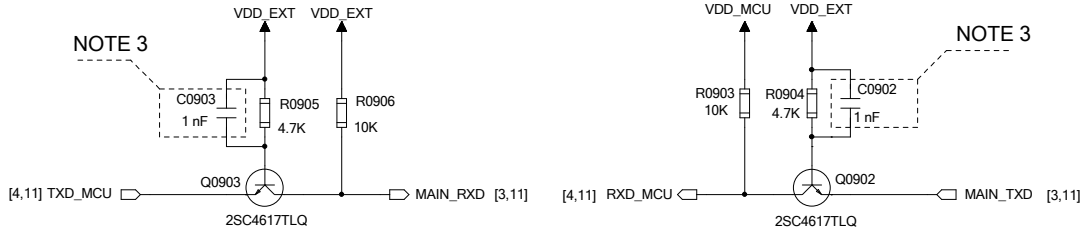
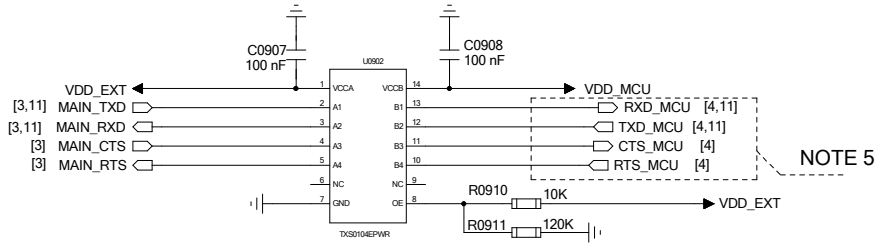
UART Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



NOTE:

1. There are two solutions: transistor solution and IC solution, and it is recommended to select the latter.
2. The power supply of TXS0104EPWR's VCCA should not exceed that of VCCB.
   For more information, please refer to the datasheet of TXS0104EPWR.
3. The transistor solution is not suitable for applications with baud rates exceeding 460 kbps.
   The capacitors C0902 and C0903 of 1 nF can improve the signal quality.
4. The MAIN_RTS level-shifting circuit is similar to that of the MAIN_RXD.
   The MAIN_CTS level-shifting circuit is similar to that of the MAIN_TXD.
5. The hardware flow control pins CTS and RTS adopt the direct connection mode, that is, the module CTS is connected to MCU CTS, and the module RTS is connected to the MCU RTS. In addition, pay attention to the direction of connection.
   TXD and RXD adopt a cross connection mode, that is, the TXD and RXD of the module are connected to the RXD and TXD of the MCU respectively.

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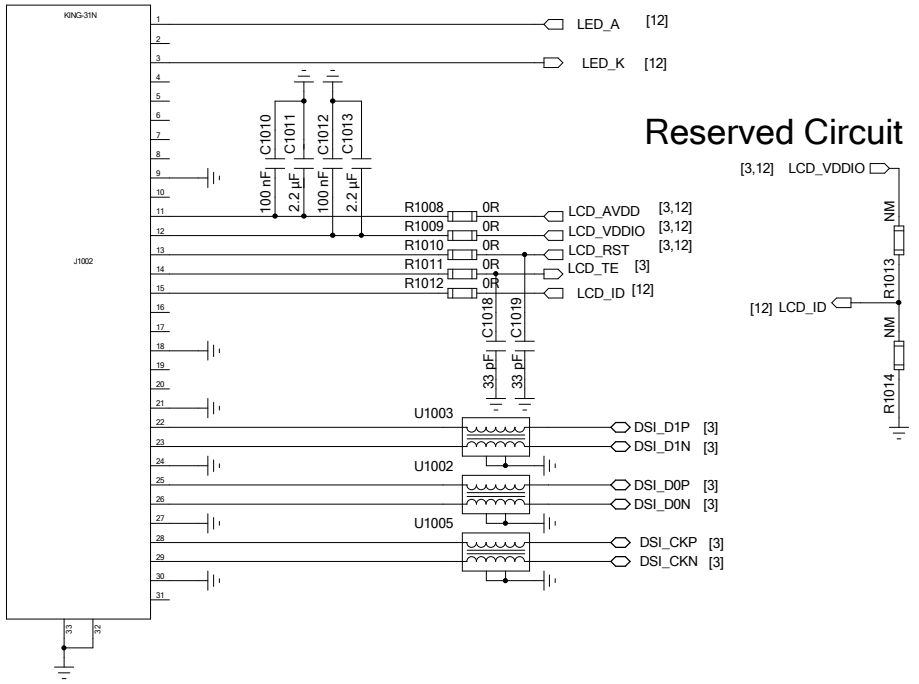
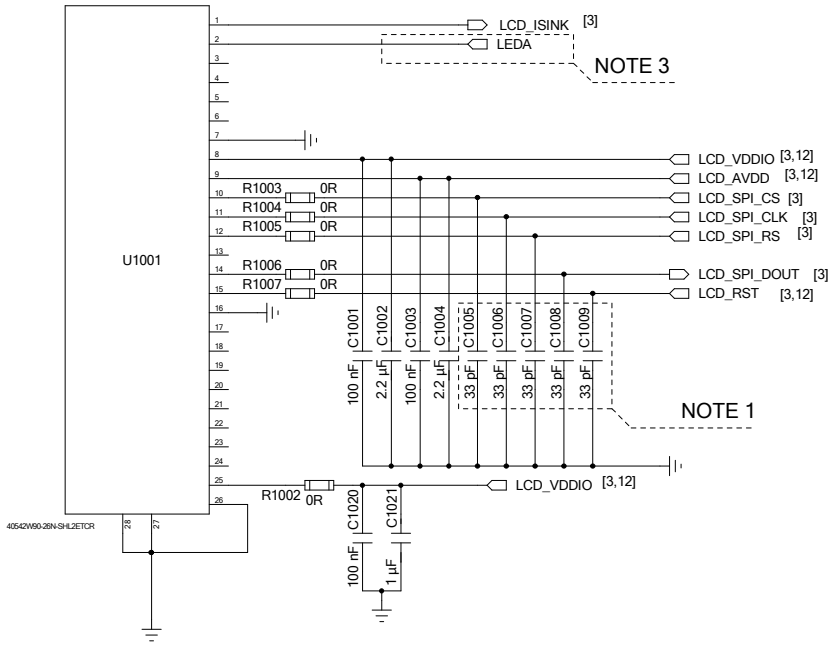
LCM Interface Design

MIPI

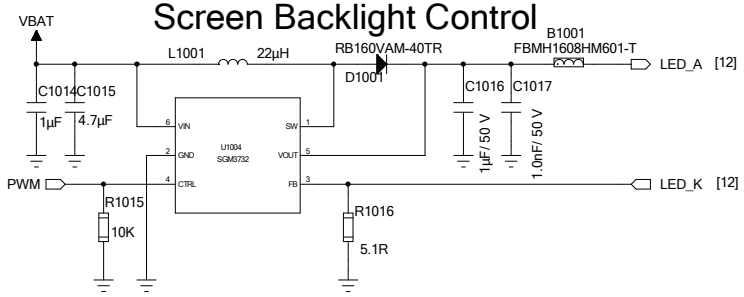


Reserved Circuit

SPI



Screen Backlight Control



NOTE:

1. Please determine the resistance value of R1016 according to the current value in the backlight chip data sheet.
2. Any available GPIO of the module can be connected to the PWM pin to simulate the frequency and duty cycle. The recommended frequency range is 3-5 kHz. Contact Quectel Technical Support for details on this pin.

NOTE:

1. The 33 pF capacitors of the signal pins are reserved, and can be used as per the actual debugging situation.
2. To avoid abnormal LCD display caused by power fluctuation, the filter capacitors of the LCD power supply pins, LCD_AVDD and LCD_VDDIO, must be attached.
3. The power supply pin LEDA of the backlight is provided by an external power supply circuit, and you can design the circuit by yourself.

NOTE:

You can use either SPI or MIPI in the LCM interface design, and it is recommended to choose the former.

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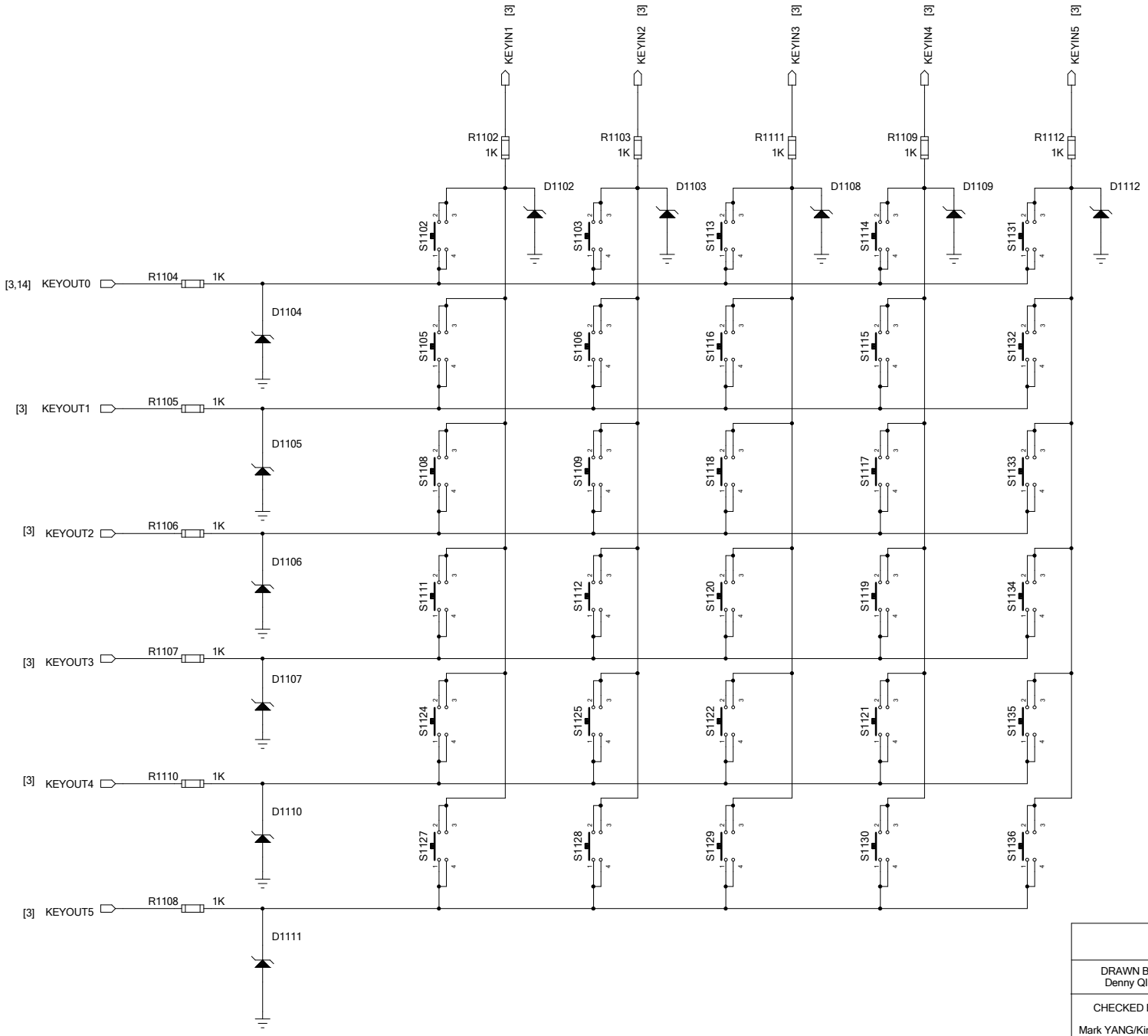
Matrix Keypad Design



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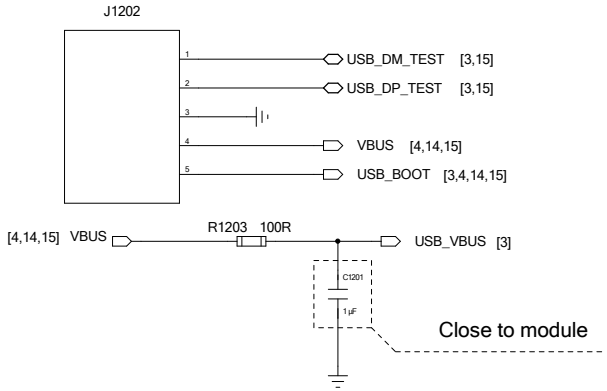
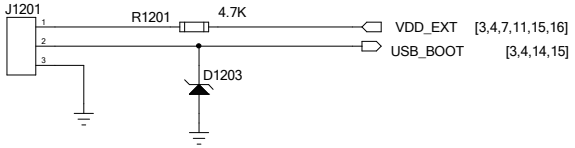
Download Methods

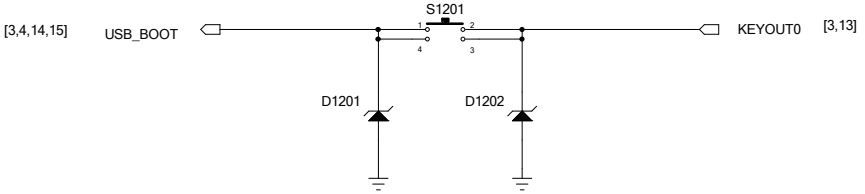
USB Interface Download Design



USB_BOOT Interface Design Method I



USB_BOOT Interface Design Method II



NOTE:

1. Put the module into the download mode before upgrading the firmware. There are two ways to enter the download mode:
   Method I: Connect the USB_BOOT with VDD_EXT before power-up and the module will enter download mode when it is turned on;
   Method II: Before powering on the module, press the scan button composed of "USB_BOOT + KEYOUT0", and the module will enter the download mode when it is turned on.
2. Be sure to reserve the USB_BOOT interface circuit (choose one of the two methods) to upgrade the firmware. If the application device has a scan button, it is recommended to adopt the download circuit design of the second method, that is, entering the download mode by pressing the button, to facilitate the firmware upgrade of the final product.
3. The circuit of USB_BOOT Interface Design Method I is a compatible method for EC600x series modules to enter the download mode. For example, pulling up USB_BOOT pin for EC600U series (connect pins 1 and 2 of J1201), and pulling it down for EC600N-CN (connect pins 2 and 3 of J1201).

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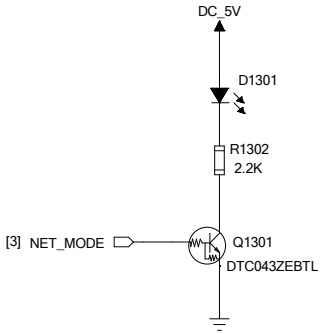
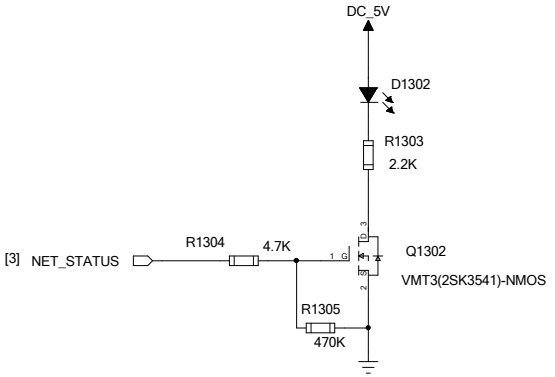
Other Designs

Indicators

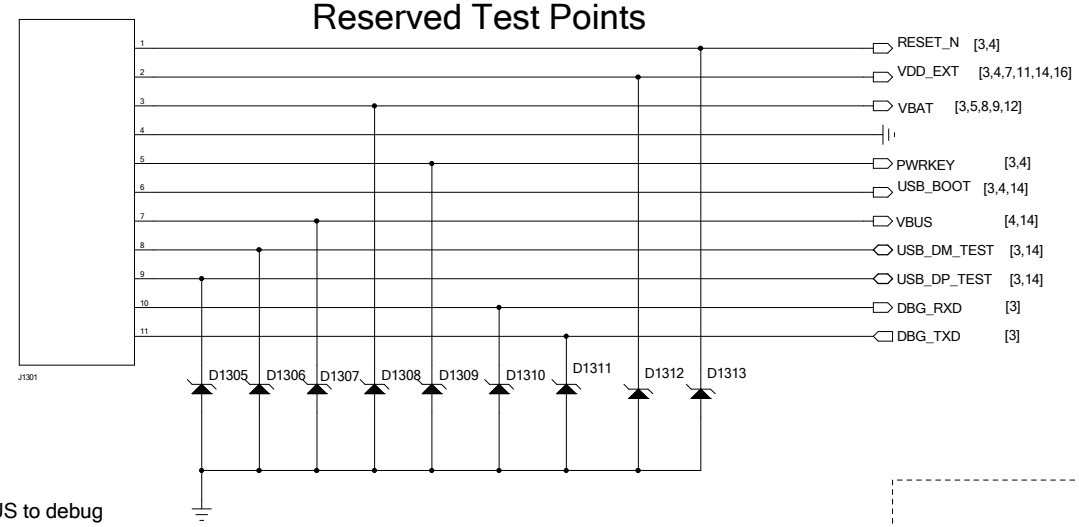




NOTE:

1. For more details about NET_MODE and NET_STATUS, please refer to *Quectel_EC600U_Series_QuecOpen_Hardware_Design.*
2. If the low power consumption is required when the customer's device is in sleep, replace the power supply DC_5V of the NET_MODE and NET_STATUS indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

Reserved Test Points



NOTE:

1. Test points must be reserved for USB_DP, USB_DM and USB_VBUS to debug software and upgrade firmware, and for DBG_RXD and DBG_TXD to capture AP logs, and for UART2_RTS to capture CP logs.
2. The parasitic capacitance of the ESD protection components on USB data lines should be less than 2 pF.
3. The debug UART interface supports 1.8 V power domain, and a level-shifting circuit should be used if the power domain of customer's application is 3.3 V. For details, please refer to the "UART Interface Design". The debug UART only supports the baud rate of 921600 bps.
4. Put the module into the download mode before upgrading the firmware. Please refer to the "Download Methods" for the download circuit design.
5. Test points are recommended to be reserved for USB_BOOT, RESET_N and VDD_EXT.

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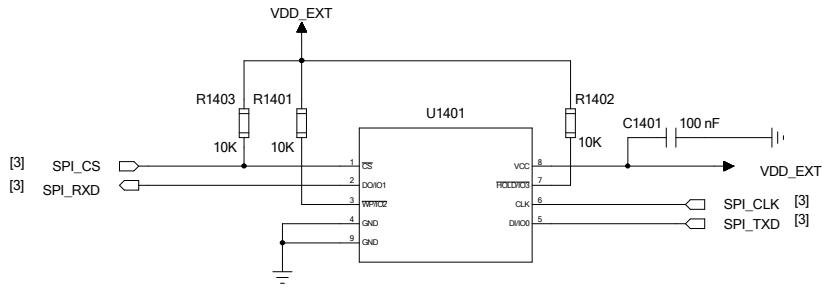
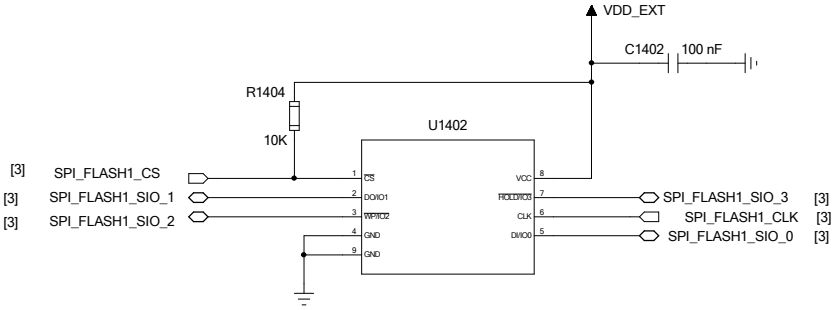
External Flash Interface Design

Four-wire NOR Flash Circuit Design



Six-wire NOR Flash Circuit Design



NOTE:

1. The power filter capacitors C1401 and C1402 need to be placed close to the power pins of the flash chip to achieve the expected filtering effect.
2. For the four-wire NOR flash circuit, it is recommended that the WP and HOLD pins be connected with pull-up resistors, to avoid abnormal levels causing the flash chip to malfunction, resulting in abnormal transmission or data loss.
3. The SPI interface of the module only supports master mode, that is, the module can only be a host when communicating with the peripherals through the SPI interface.
4. The signal traces of external Flash interface need to be equal in length, with a difference of less than 1 mm.

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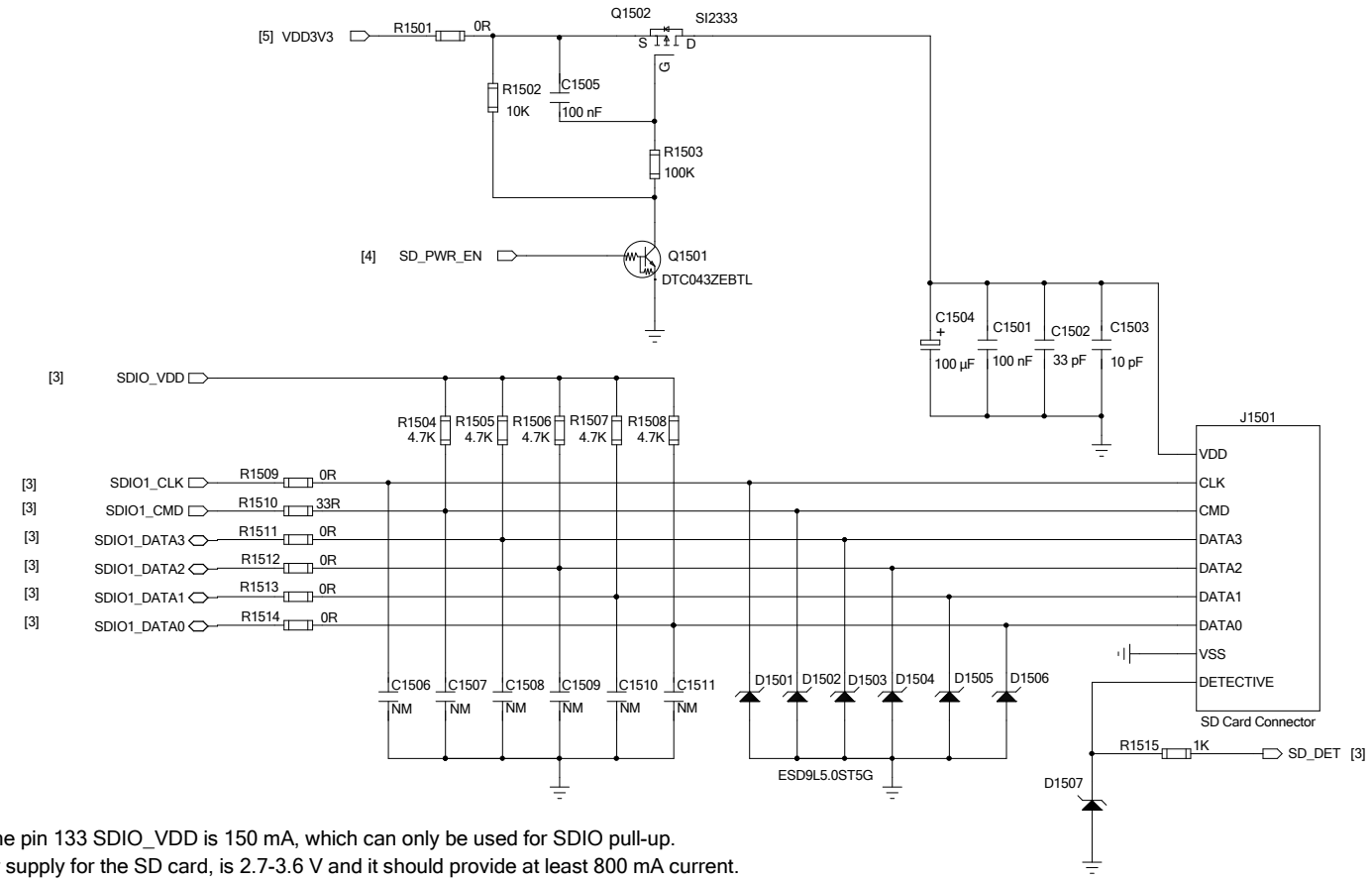
SD Card Interface Design



NOTE:

1. The maximum output current of the pin 133 SDIO_VDD is 150 mA, which can only be used for SDIO pull-up.
2. The voltage range of VDD, power supply for the SD card, is 2.7-3.6 V and it should provide at least 800 mA current.
3. To avoid the jitter of bus, pull-up resistors R1504-R1508 are recommended to be added to SDIO signal traces and the recommended value is 4.7 kΩ.
   The pull-up power supply should be the SDIO_VDD of the module.
4. In order to adjust the signal quality, it is recommended to connect resistors in series between the module and the SD card connector. The recommended resistance value is 0 Ω for R1509 and R1511-R1514 and 33 Ω for R1510. The bypass capacitors C1506-C1511 are reserved and not mounted by default.
5. For good ESD protection, add a TVS diode on each SD card pin, and place them as close to the SD card connector as possible.
   The parasitic capacitance of ESD components should be less than 15 pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noise signals such as clock and DC-DC signals.
7. Route SDIO signals with 50 Ω ±10 % impedance. It is important to route SDIO signals with ground surrounded, and the total routing length should be less than 50 mm.
   It is recommended to keep the trace length difference among SDIO1_CLK, SDIO1_DATA[0:3] and SDIO1_CMD less than 1 mm.
8. Keep the space between SDIO signal traces and other signal traces greater than twice the trace width and ensure that the bus capacitance is less than 15 pF.

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