EC600G-CN QuecOpen Reference Design

LTE Standard Module Series

Version: 1.0

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Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2023-02-14	Jayce JIANG/Nathan YANG	Creation of the document
1.0	2023-03-31	Jayce JIANG/Nathan YANG	First official release

Contents

1 Reference Design

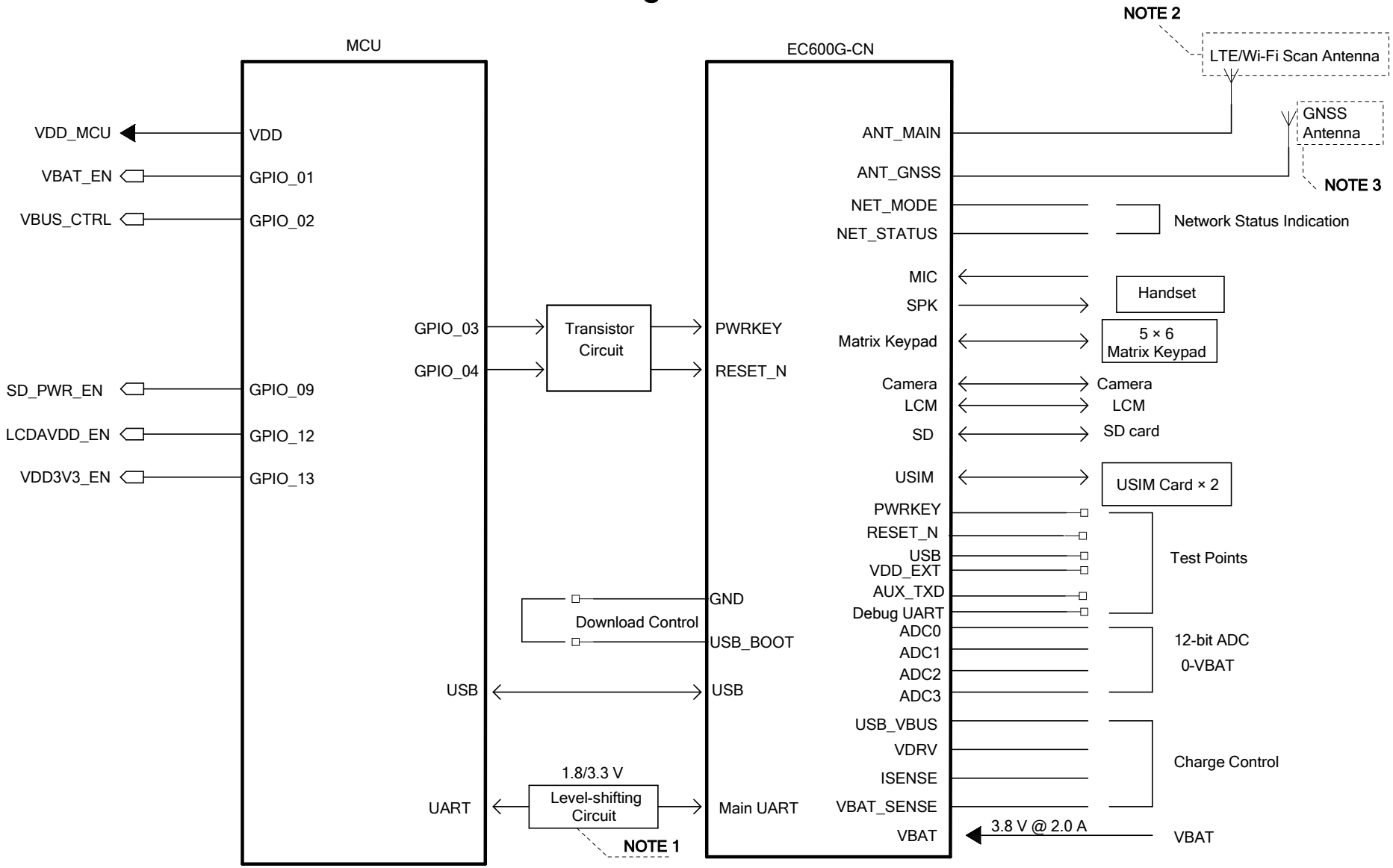
1.1. Introduction

This document provides the reference design for Quectel EC600G-CN QuecOpen® module, including block diagrams of the module design, power supply, antenna, USIM, camera, analog audio, UART and LCM interface design.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



NOTE:

1. A level-shifting circuit with a transistor or a voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.
2. Wi-Fi scan that only supports receiving, shares the same antenna interface with LTE antenna. The two functions cannot be used at the same time.
3. GNSS function is optional for the module.

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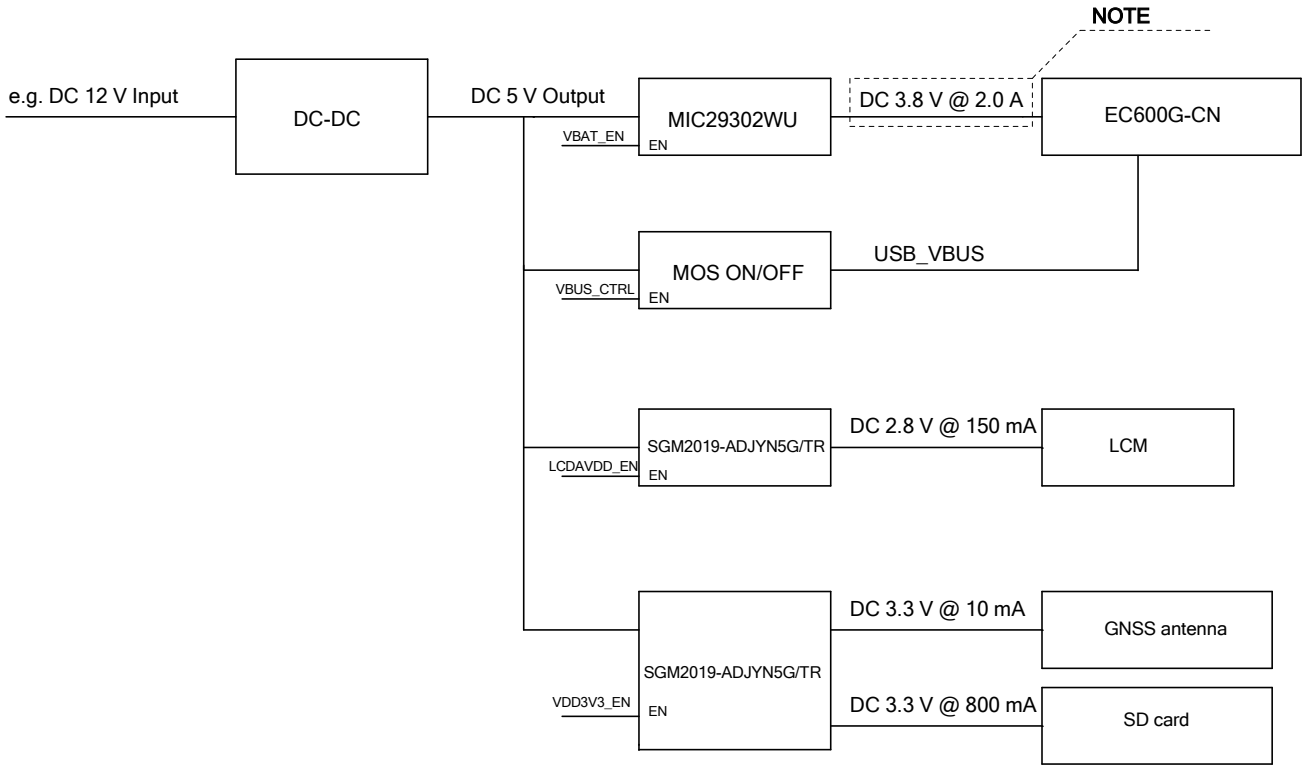
Power System Block Diagram



NOTE:

1. The power supply for the module should be at least 2 A.
2. GNSS function is optional for the module.

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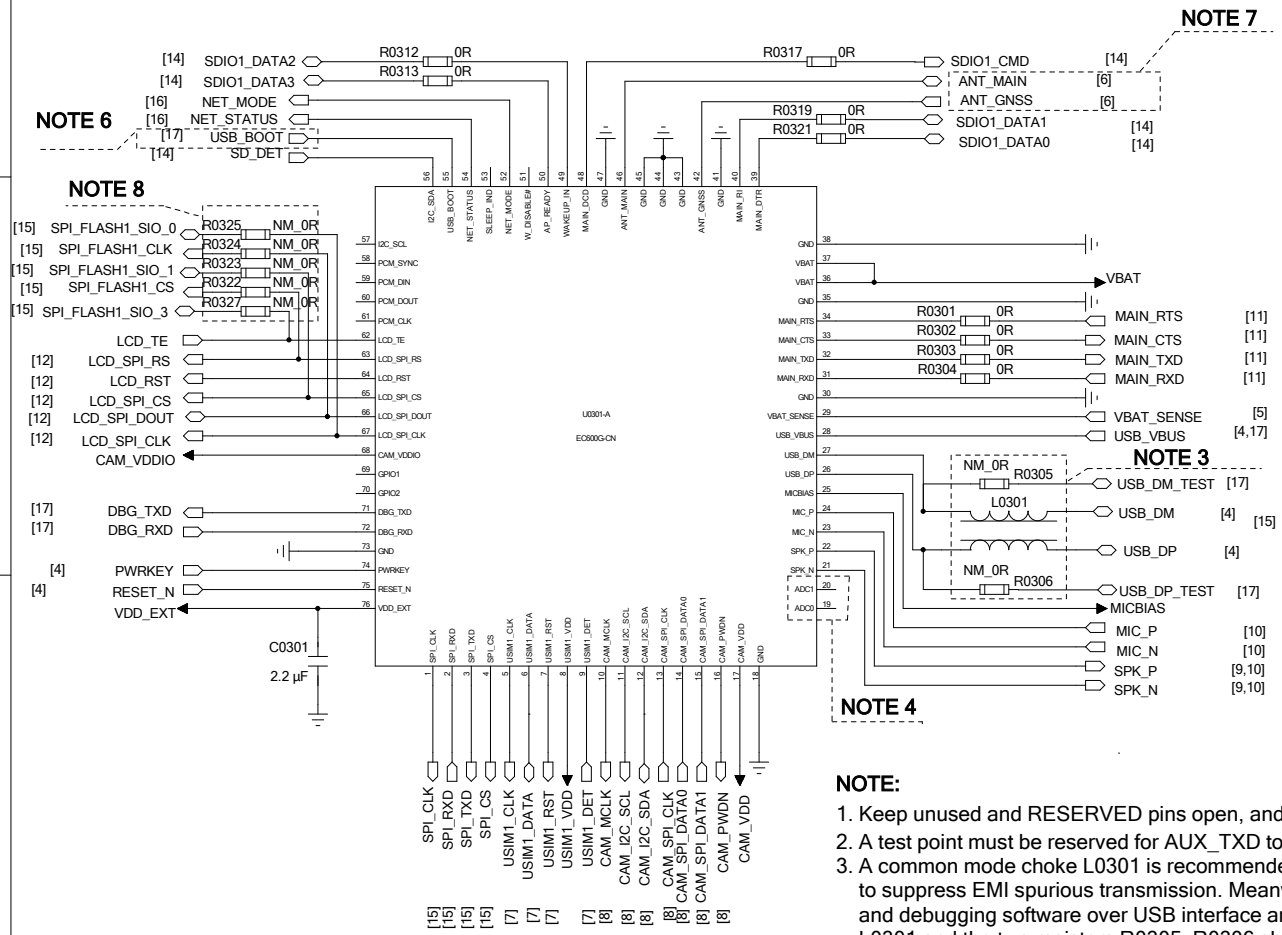
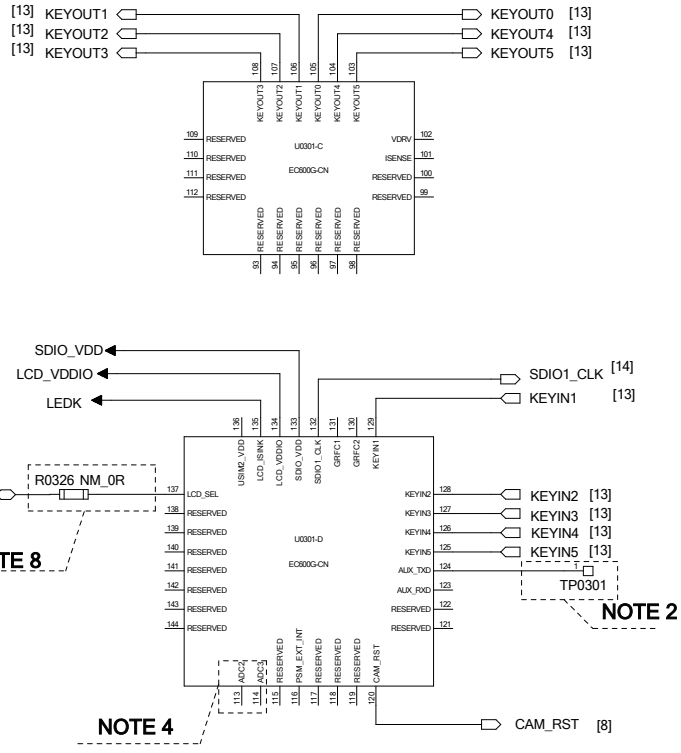
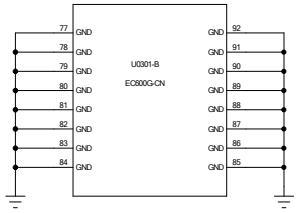
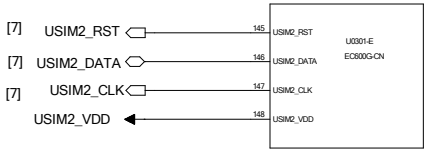
Module Interfaces









NOTE:

1. Keep unused and RESERVED pins open, and connect all GND pins to the ground network.
2. A test point must be reserved for AUX_TXD to capture CP logs.
3. A common mode choke L0301 is recommended to be added in series between the module and your MCU in order to suppress EMI spurious transmission. Meanwhile, reserve test points for upgrading the firmware and debugging software over USB interface and minimize the extra stubs of the trace. L0301 and the two resistors R0305, R0306 should be placed close to the module to ensure the integrity of USB signal.
4. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins, it is strongly recommended to reserve the voltage divider circuit for better compatibility with other Quectel modules. The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced. When the divider circuit is not used, the ADC pins require 1 kΩ resistors in series.
5. The module optionally supports a built-in codec. Since the built-in codec uses the same signals as the module's PCM interface (pins 58-61) for external digital audio design, when the built-in codec is used, the PCM interface cannot be used for other purposes (that is, keep pins 58-61 unconnected).
6. When emergency download function is not to be used, USB_BOOT cannot be pulled down or pulled up before the module starts up.
7. Wi-Fi scan that only supports receiving, shares the same antenna interface with LTE antenna. The two functions cannot be used at the same time. GNSS function is optional for the module.
8. When using the multiplexing function of these pins, 0 Ω resistors in series are needed for the selection of functions in compatible design.
9. MAIN_DTR, MAIN_RI, MAIN_DCD, WAKEUP_IN, AP_READY, W_DISABLE# and SLEEP_IND do not have the functions described by the pin names and their default functions are GPIOs.

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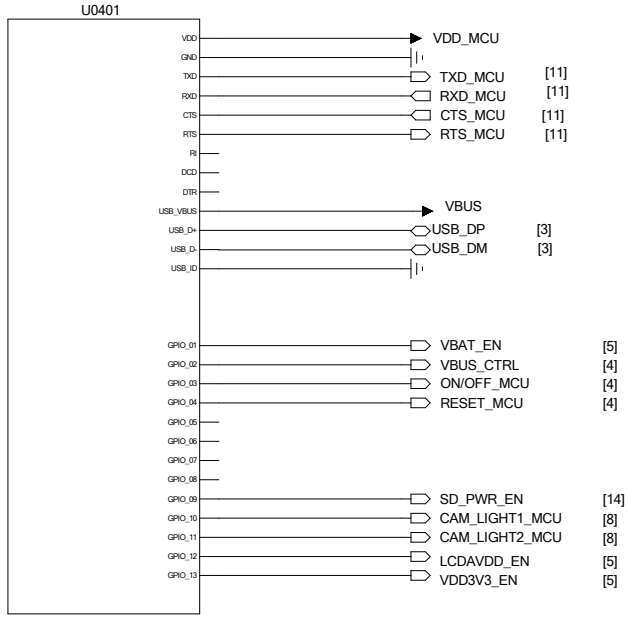
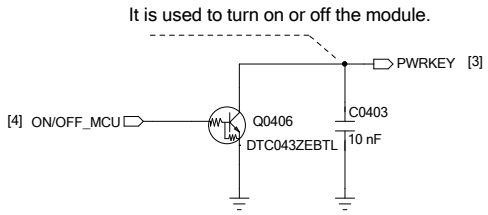
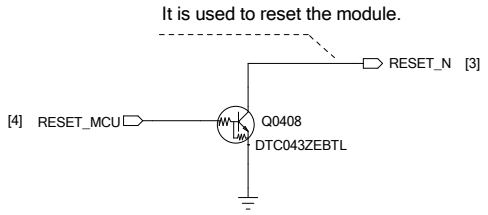
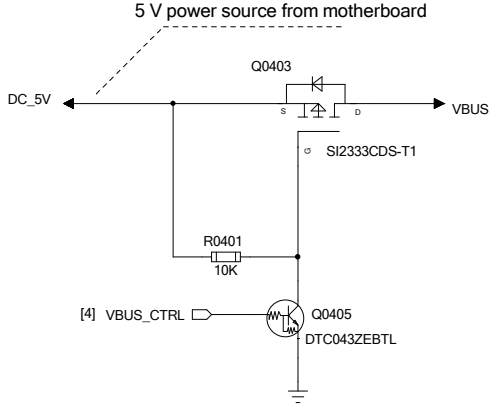
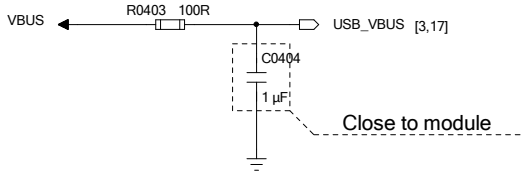
MCU Interfaces











NOTE:

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V;
   if the GPIO interfaces of U0401 share the same power domain, then the related level-shifting circuit can be omitted.
2. The USB 2.0 interface of the module only serves as a salve device and supports full-speed and high-speed modes.
   To communicate with the USB interface, MCU needs to support USB host mode or USB OTG. The USB_VBUS pin of the module should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the default low-level GPIO pins of MCU as the control pins for PWRKEY and RESET_N of the module.
   Ensure that the maximum load capacitance of PWRKEY and RESET_N does not exceed 10 nF.

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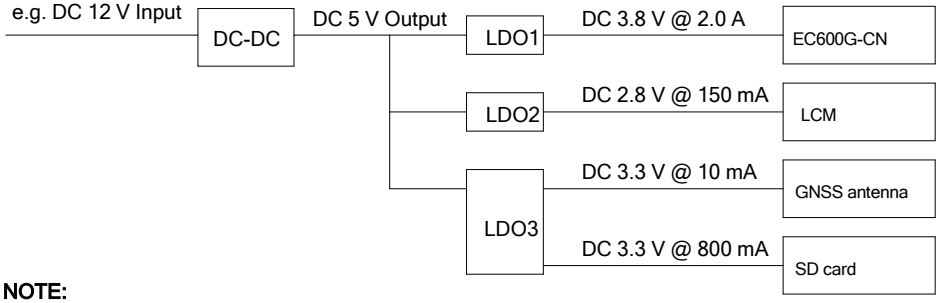
Power Supply Design

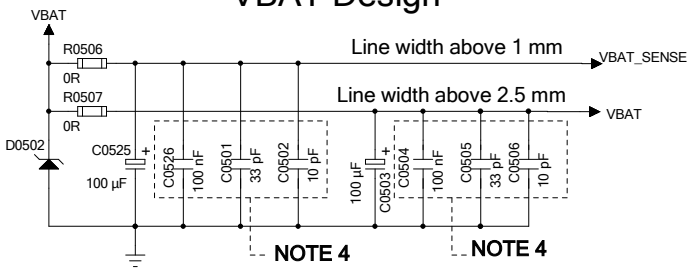
DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert a high input voltage into a 5.0 V, and use LDOs to convert it to 3.8 V and 2.8 V and 3.3 V.



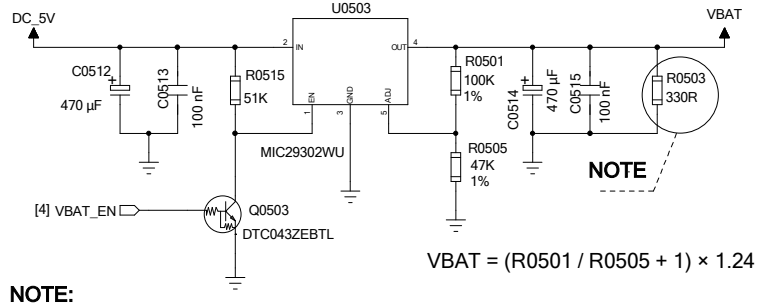
NOTE:
GNSS function of the module is optional.

VBAT Design



NOTE:
1. The power supply for the module should be at least 2 A.
2. The VBAT traces must be connected to pins VBAT_SENSE and VBAT in star configuration.
3. The recommended operating voltage of VBAT is 3.3-4.3 V, and the typical value is 3.8 V.
4. C0526, C0501 and C0502 should be placed close to VBAT_SENSE pin.
   C0504, C0505 and C0506 should be placed close to VBAT pins.

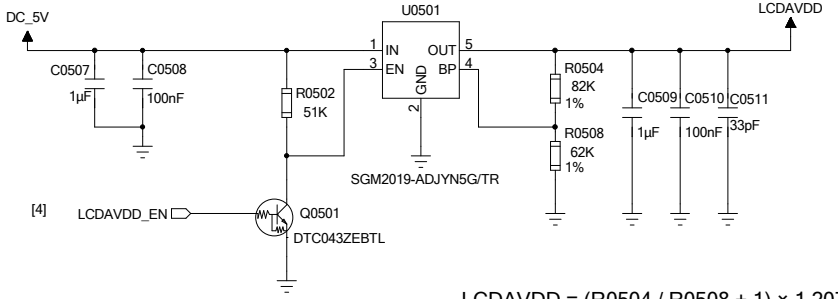
LDO Application



VBAT = (R0501 / R0505 + 1) × 1.24 = 3.88 V

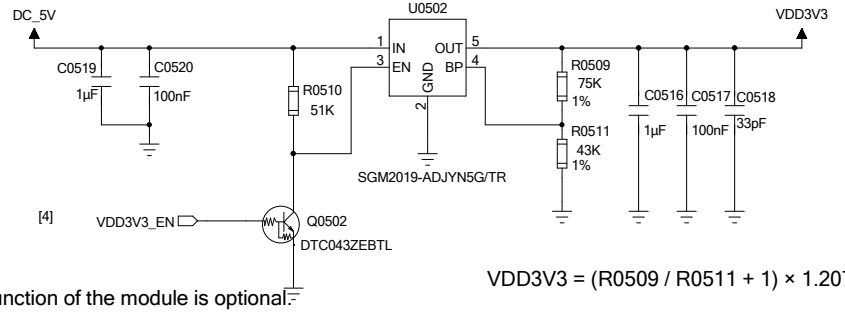
NOTE:
1. The recommended load current is greater than 10 mA.
2. When the input voltage is below 7.0 V, use an LDO to convert it to 3.8 V.

LCM Power Supply



LCDAVDD = (R0504 / R0508 + 1) × 1.207 = 2.8 V

GNSS & SD Card Power Supply



NOTE:
GNSS function of the module is optional.

VDD3V3 = (R0509 / R0511 + 1) × 1.207 = 3.3 V

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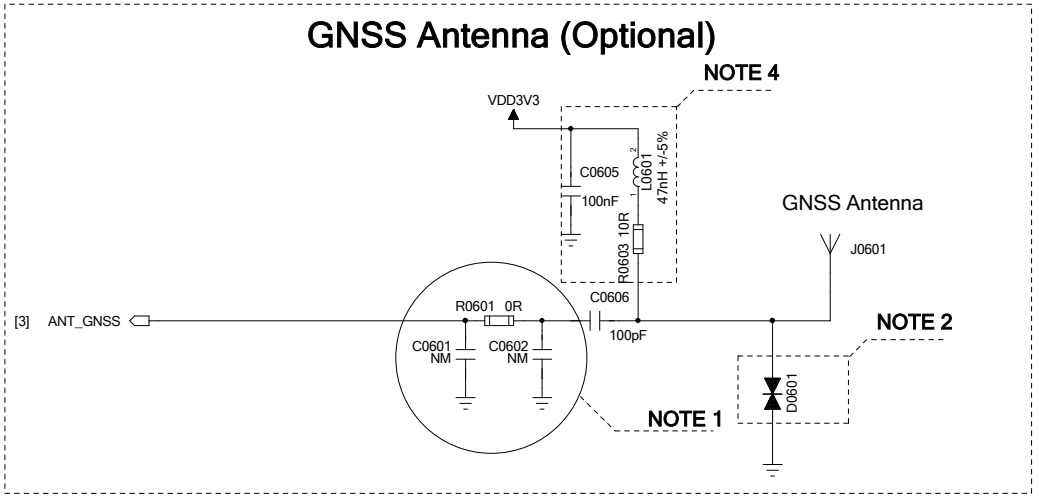
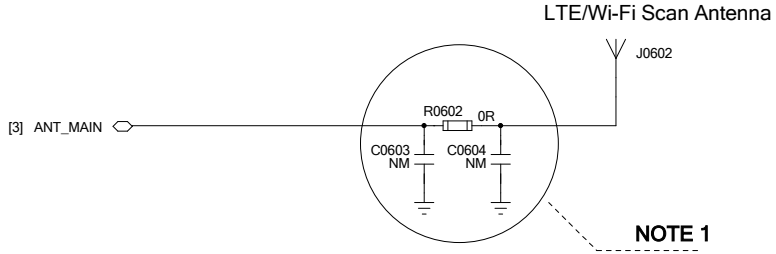
Antenna Interface Design

GNSS Antenna (Optional)



LTE/Wi-Fi Scan Antenna



NOTE:

1. It is highly recommended to reserve a Π-type matching circuit for further debugging.
2. It is recommended that the junction capacitance of the ESD protection components used for the antenna interface does not exceed 0.05 pF.
3. The single-ended impedance of the RF antenna is 50 Ω.
4. It is recommended to place C0605, R0603 and L0601 close to the RF traces in layout.
5. The power supply voltage range of external GNSS antenna is 2.8-4.3 V, and the typical value is 3.3 V.
   The power supply voltage can be designed according to the power supply requirements of the selected active antenna.
6. The active antenna is only suitable for GNSS function.

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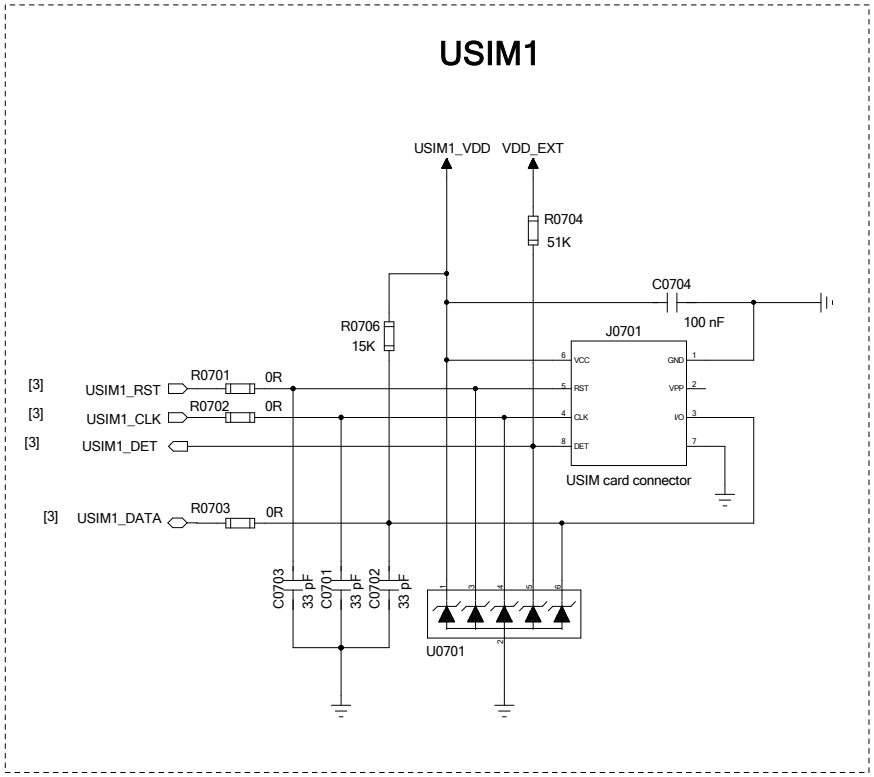
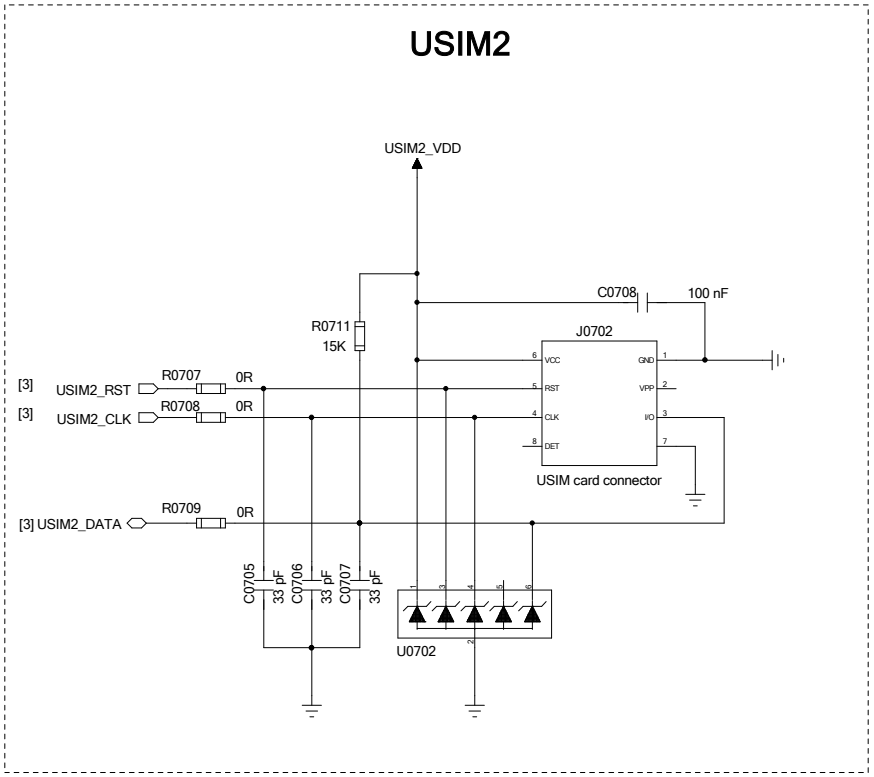
USIM Interface Design





NOTE:

1. U0701 and U0702 are recommended to be used to offer good ESD protection, and the parasitic capacitance should not exceed 15 pF.
2. The pull-up resistors R0706 and R0711 can improve anti-jamming capability, and should be placed close to the USIM card connector.
3. R0701-R0703 and R0707-R0709 are used for debugging, and C0701-C0703 and C0705-C0707 are used for filtering out RF interference.
4. C0704 and C0708's capacitance should be less than 1 μF and they should be placed close to the USIM card connector.
5. The GND of the USIM card connector is recommended to be connected to the GND layer directly.
6. For more information about the layout of USIM interfaces, refer to the hardware design document of the module.

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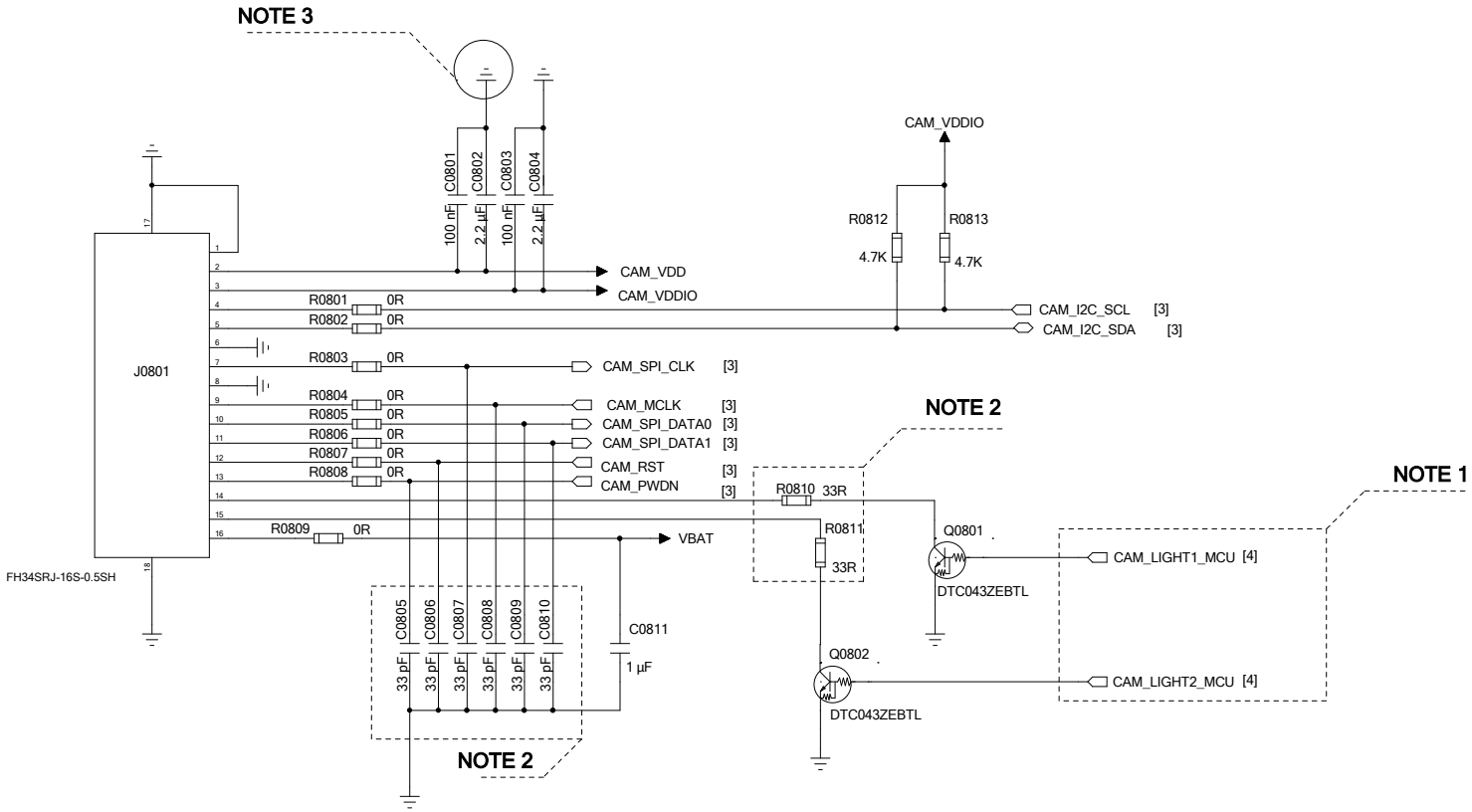
Camera Interface Design



NOTE:

1. CAM_LIGHT1_MCU controls the cathode of the positioning light of the camera by controlling the triode switching circuit;
   CAM_LIGHT2_MCU controls the cathode of the supplement light of the camera by controlling the triode switching circuit;
   it is recommended to select the default pull-down GPIO pins as the two control pins.
2. The 33 pF capacitors of the signal pins are reserved, and they are used according to the actual debugging situation.
   The values of current limiting resistors of positioning light and supplement light, R0810 and R0811, should be varied according to brightness requirements.
3. The capacitors (C0801 and C0802) of the CAM_VDD power supply should be connected to the GND layer directly, otherwise there may be power noise leading to abnormalities such as white dots on the preview screen.
4. If the camera interface is not required, the pins CAM_I2C_SCL and CAM_I2C_SDA can be used as an I2C interface to connect other peripherals.

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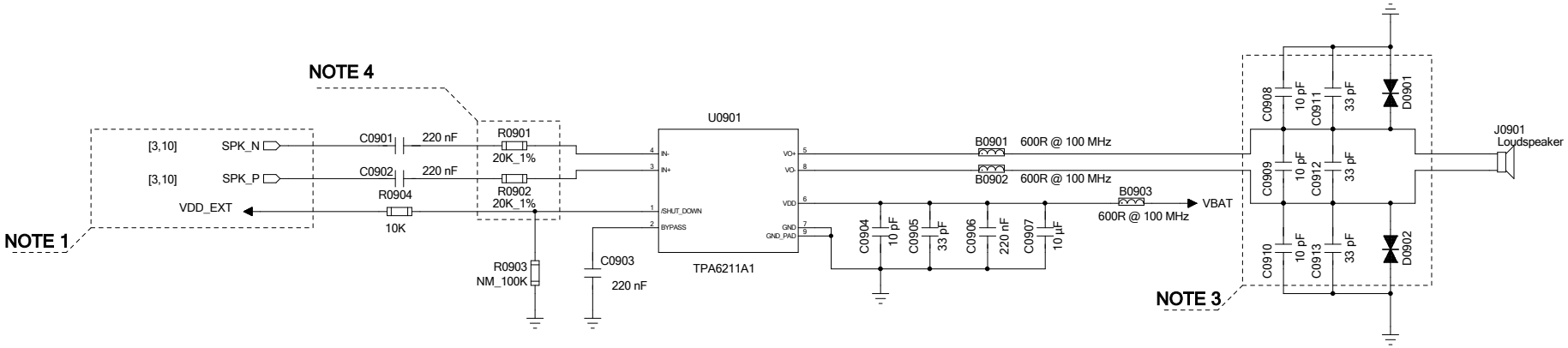
Analog Audio Design (Audio Power Amplifier)



NOTE:

1. SPK_N and SPK_P are differential output channels. When the channels are turned on or off, it is possible for the module to emit a pop sound, which can be eliminated by controlling the enable pin of the audio PA. For details, contact Quectel Technical Support.
2. The power amplifier in this design is for reference only. Choose the audio power amplifier with appropriate power according to the actual needs.
3. Place filter capacitors and ESD protection components close to the loudspeaker.
4. Audio PA Gain = 40 kΩ / R0901 or R0902.

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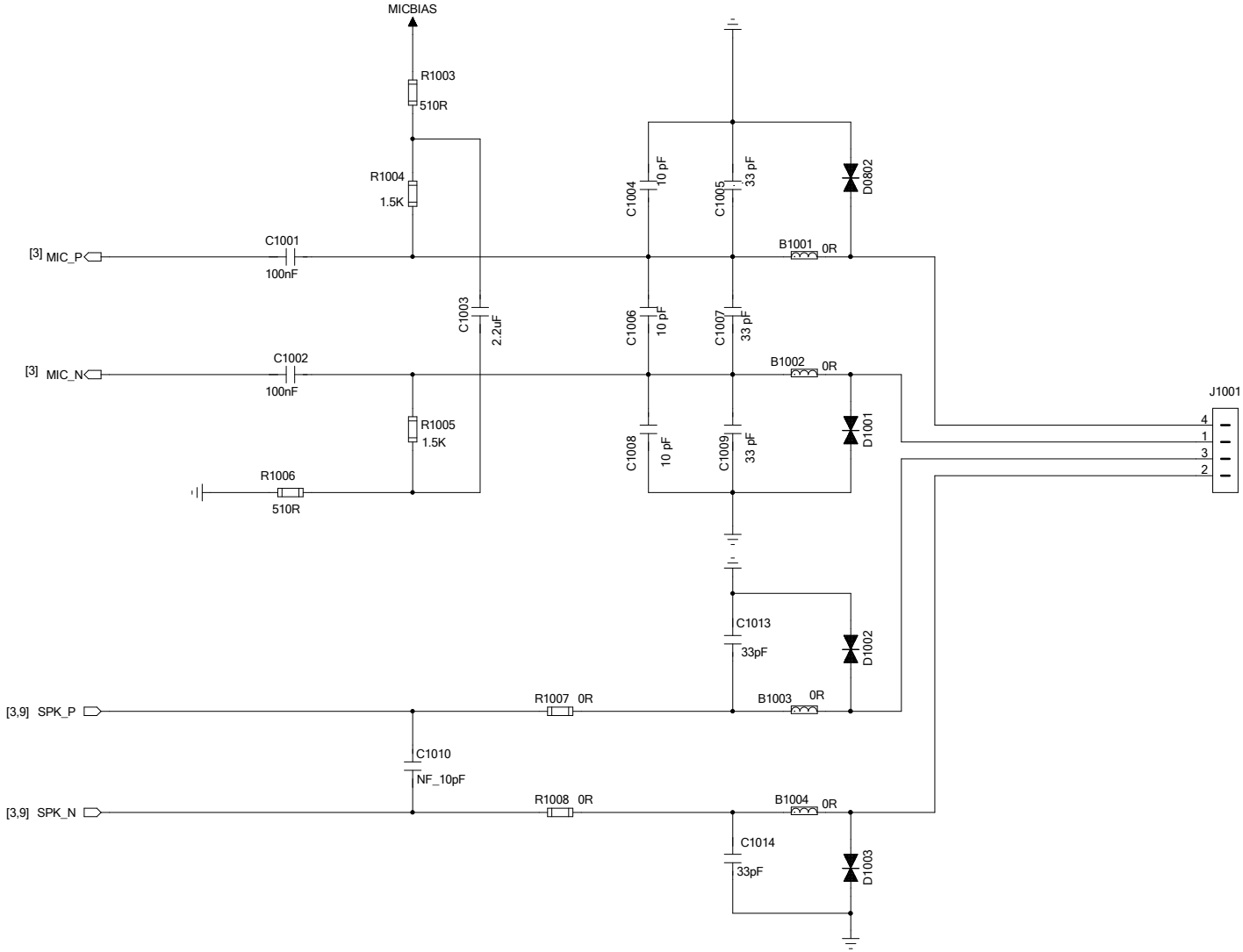
Analog Audio Design (Handset)



NOTE:

1. Both the MIC and SPK signal traces need to be routed as differential pairs.
2. All MIC and SPK signal traces should be surrounded with ground on the layer and with ground planes above and below, and far away from noise sources.

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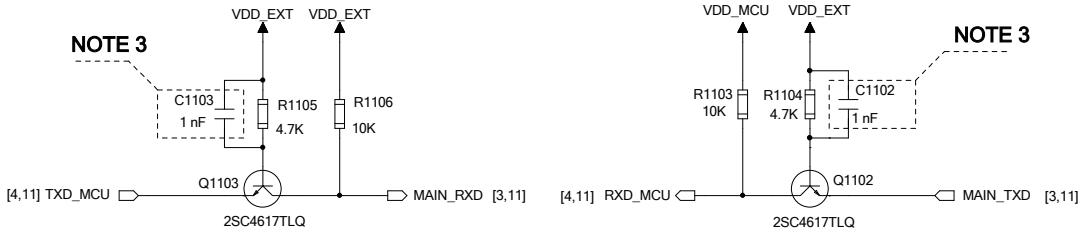
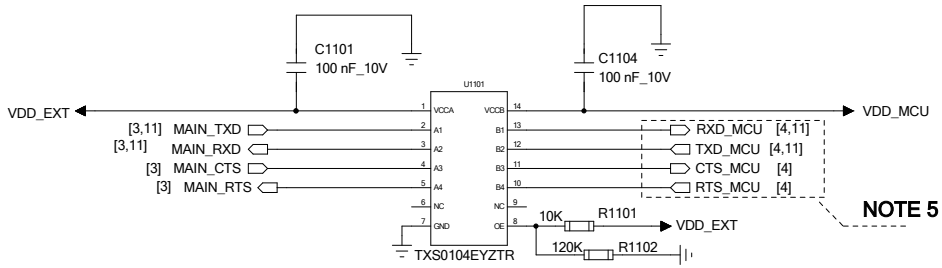
UART Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, the latter of which is recommended.
2. The power supply of TXS0104EYZTR's VCCA should not exceed that of VCCB.
   For more information, refer to the datasheet of TXS0104EYZTR.
3. The transistor solution is not suitable for applications with baud rates exceeding 460 kbps.
   The capacitors C1102 and C1103 of 1 nF can improve the signal quality.
4. The MAIN_RTS level-shifting circuit is similar to that of the MAIN_RXD.
   The MAIN_CTS level-shifting circuit is similar to that of the MAIN_TXD.
5. The hardware flow control pins MAIN_CTS and MAIN_RTS adopt the direct connection mode, that is, the module CTS is connected to the MCU CTS, and the module RTS is connected to the MCU RTS. In addition, pay attention to the direction of connection.
   MAIN_TXD and MAIN_RXD adopt a cross connection mode, that is, the TXD and RXD of the module are respectively connected to the RXD and TXD of the MCU.

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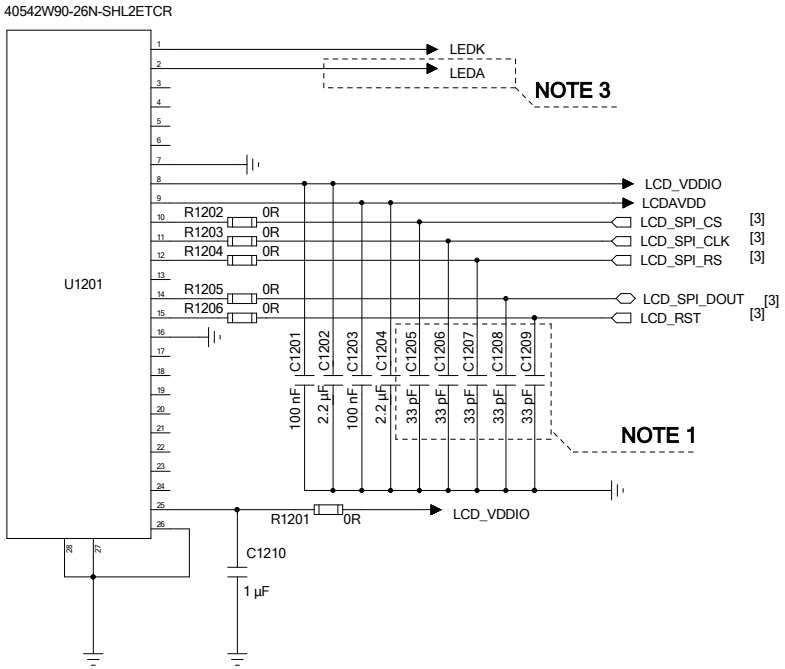
LCM Interface Design



NOTE:

1. The 33 pF capacitors of the signal pins are reserved, and can be used as per the actual debugging situation.
2. In order to avoid abnormal LCD display caused by power fluctuation, the filter capacitors of the LCD power supply pins, LCDAVDD and LCD_VDDIO, must be mounted.
3. The power supply pin LEDA of the backlight is provided by external power supply circuit, and you can design the circuit by yourself.

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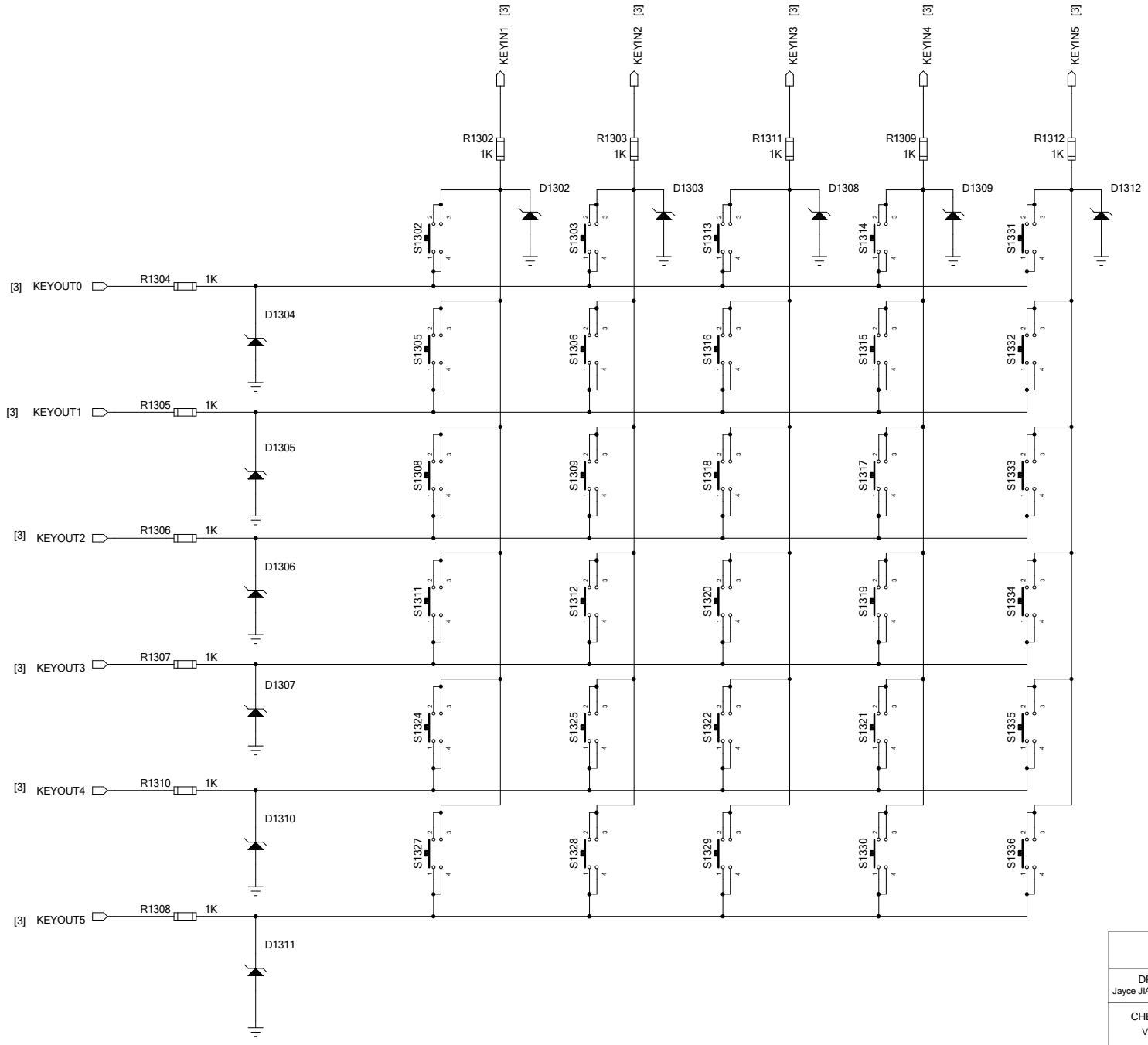
Matrix Keypad Interface Design



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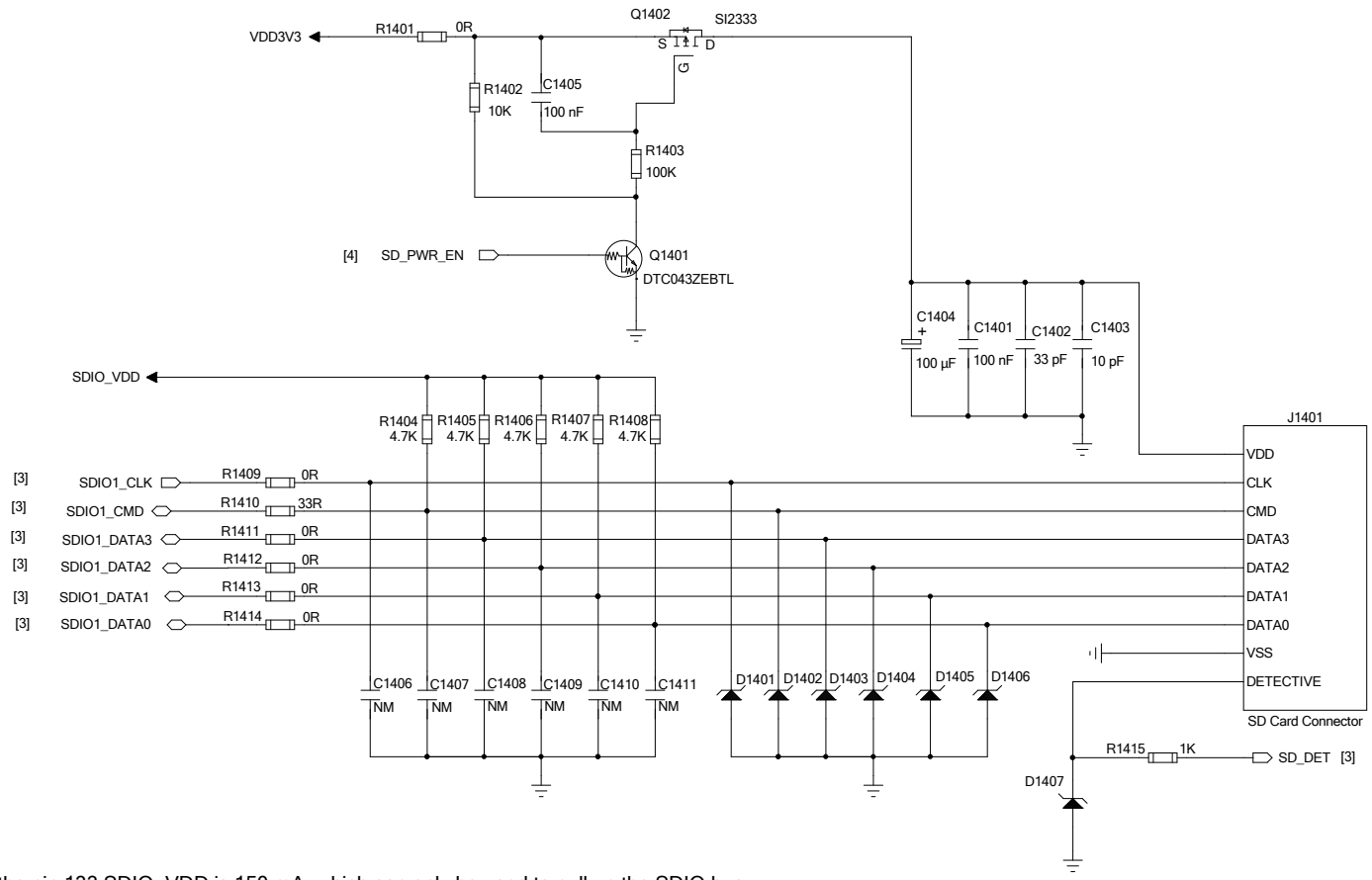
SD Card Interface Design



NOTE:

1. The maximum output current of the pin 133 SDIO_VDD is 150 mA, which can only be used to pull up the SDIO bus.
2. The voltage range of VDD, power supply for the SD card, is 2.7-3.6 V and it should provide at least 800 mA current.
3. To avoid the jitter of bus, pull-up resistors R1404-R1408 are recommended to be added to SDIO bus. Value range of these resistors should be 10-100 kΩ and the recommended value is 4.7 kΩ. SDIO_VDD should be used as the pull-up power.
4. To improve signal quality, it is recommended to add resistors R1409-R1414 in series between the module and the SD card connector. The bypass capacitors C1406-C1411 are reserved and not mounted by default.
5. For good ESD protection, add a TVS diode on each SD card pin, and place them as close to the SD card connector as possible. The parasitic capacitance of TVS diodes should be less than 15 pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noise signals such as clock and DC-DC signals.
7. Route SDIO signals with 50 Ω ±10 % impedance. It is important to route SDIO signals with ground surrounded, and the total routing length should be less than 50 mm. It is recommended to keep the trace length difference among SDIO1_CLK, SDIO1_DATA[0:3] and SDIO1_CMD less than 1 mm.
8. Keep the space between SDIO signal traces and other signal traces greater than twice the trace width and ensure that the bus capacitance is less than 15 pF.

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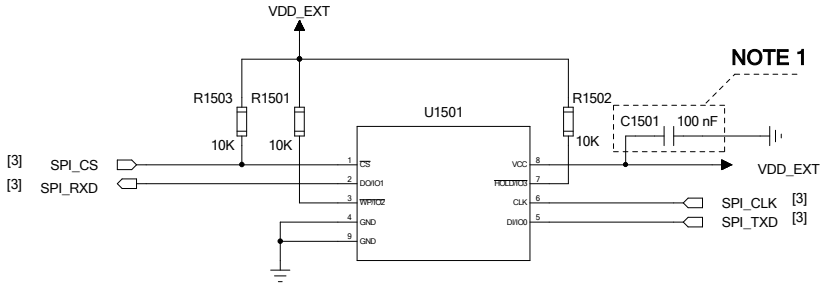
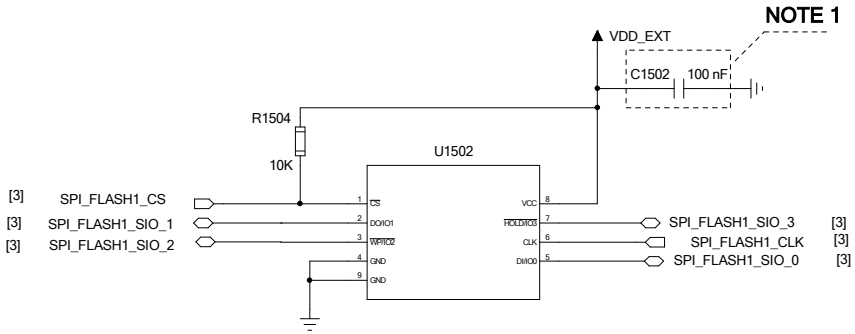
External Flash Interface Design

Four-wire NOR Flash Circuit Design



Six-wire NOR Flash Circuit Design



NOTE:

1. The power filter capacitors C1501 and C1502 need to be placed close to the power pins of the flash chip to achieve the expected filtering effect.
2. For the four-wire NOR flash circuit, it is recommended that the WP and HOLD pins be connected with pull-up resistors, to avoid abnormal levels causing the flash chip to malfunction, resulting in abnormal transmission or data loss.
3. The SPI of the module only supports master mode, that is, the module can only be a host when communicating with the peripherals through SPI.

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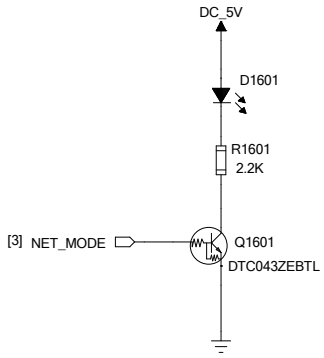
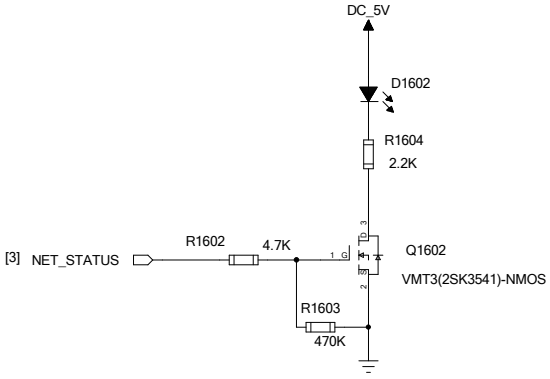
Indicators





NOTE:

1. For more details about NET_MODE and NET_STATUS, refer to the hardware design document of the module.
2. If the low power consumption is required when your device is in sleep, replace the power supply DC_5V of the NET_MODE and NET_STATUS indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

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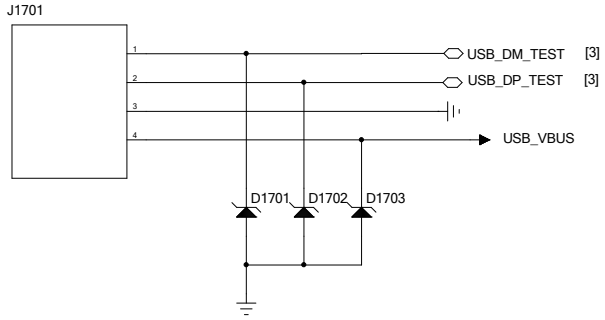
Reserved Test Points

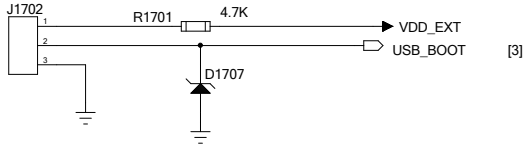
USB Interface Test Points



NOTE:

1. Test points must be reserved for USB interface.
2. The module can upgrade firmware and debug the software over USB interface. The parasitic capacitance of the ESD protection components on USB data lines should be less than 2 pF.

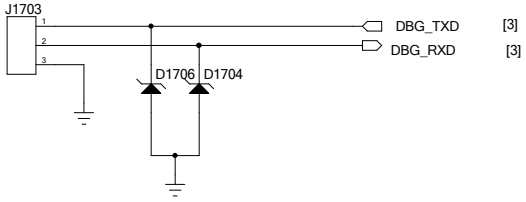
USB_BOOT Interface Test Points



NOTE:

1. It is recommended to reserve a test point for USB_BOOT interface.
2. Pull down the USB_BOOT to GND before the module starts up, and the module will enter the emergency download mode when it is turned on. In this mode, the module supports firmware upgrading over USB interface.

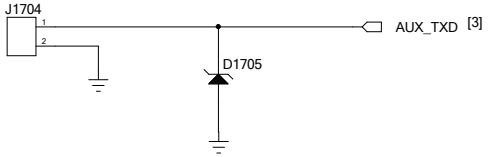
Debug UART Test Points



NOTE:

1. Test points must be reserved for DBG_TXD and DBG_RXD to capture AP logs.
2. The debug UART interface supports 1.8 V power domain, and a level-shifting circuit should be used if the power domain of your application is 3.3 V. For details, refer to the "UART Interface Design".
3. The debug UART only supports the baud rate of 2000000 bps.

Auxiliary UART Test Points



NOTE:

1. A test point must be reserved for AUX_TXD to capture CP logs.
2. The auxiliary UART interface supports 1.8 V power domain, and a level-shifting circuit should be used if the power domain of your application is 3.3 V. For details, refer to the "UART Interface Design".
3. When capturing the CP log, set the baud rate to 8000000 bps.

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