EC200A Series QuecOpen Reference Design

LTE Standard Module Series

Version: 1.2

Date: 2023-08-02

Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2022-06-09	Shiye ZHU	Creation of the document
1.0	2022-07-26	Shiye ZHU	First official release
1.1	2023-06-01	Coco CHEN	1. Changed the required current of the module from 3.0 A to 2.8 A (Sheets 1 & 2 & 5). 1. Added the Notes 5 & 6 (Sheet 3). 2. Added reference design of WLAN interface (Sheets 3, 20, 21 and 22). 3. Changed the wakeup pin of WAKE_UP_MCU from WAKEUP_IN to MAIN_DTR (Sheet 4). 4. Updated the power supply design for SD card, SLIC, WLAN and Ethernet PHYs (Sheet 5). 5. Added two resistors R0807 and R0808 in UART Level-shifting Circuit – IC solution (Sheet 8). 6. Deleted the triode in the STATUS indicator design (Sheet 23).
1.2	2023-08-02	Julian TANG	2. Deleted resistor R1401 on VDD_3V3 trace (Sheet 14). 3. Updated the resistance of R1910 in SLIC design to 3.9 K and added related note (Sheet 19).

Contents

1 Reference Design

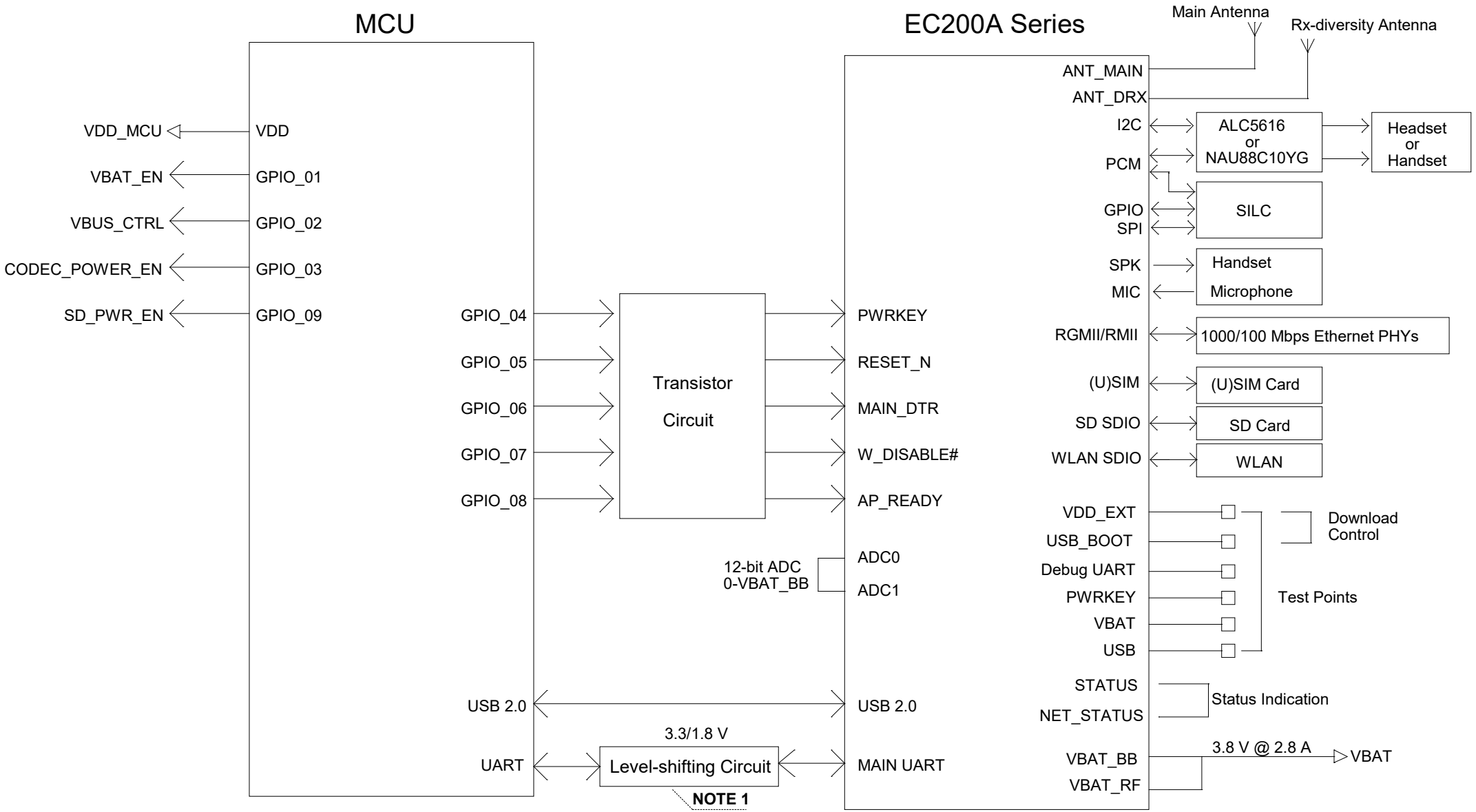
1.1. Introduction

This document provides the reference design for Quectel EC200A series QuecOpen® module, including block diagrams of power supply and module design, analog audio, UART, (U)SIM, RGMII/RMII, SD card interfaces, etc.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



NOTE:

1. A level-shifting circuit or a voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.
2. The power supply should be able to provide sufficient current of at least 2.8 A for the module.

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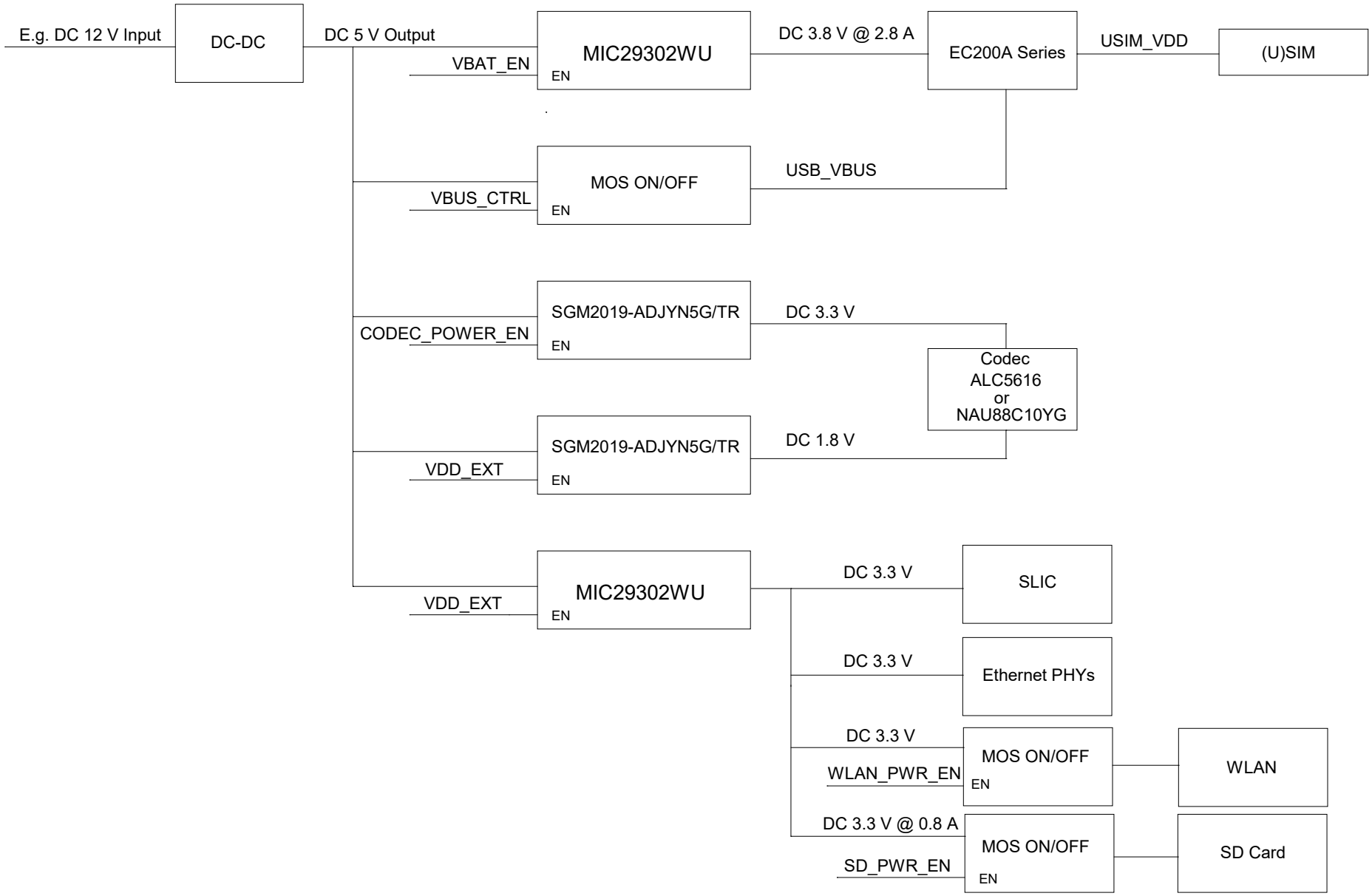
Power System Block Diagram



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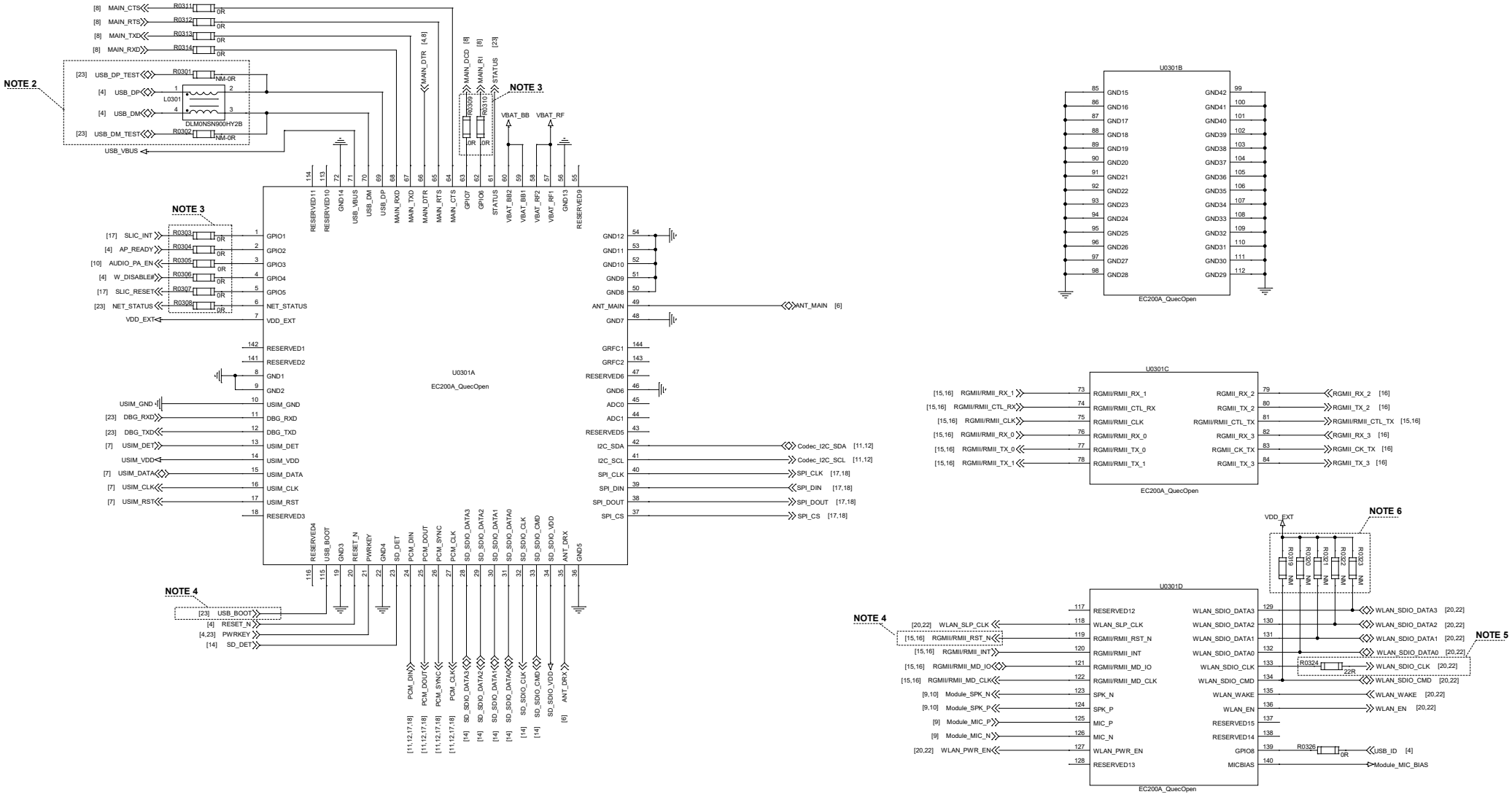
Module Interface



NOTE:

1. All GND pins should be connected to the ground, and keep unused and RESERVED pins unconnected. Ensure there is a complete reference ground plane below the module,and the ground plane is as close as possible to the layer where the module is located.
2. A common mode choke L0301 is recommended to be added in series between the module and your MCU in order to suppress EMI spurious transmission, and it should be placed close to the module. Meanwhile, it is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the extra stubs of the trace. The R0301 and R0302 resistors should be placed close to the module to ensure the integrity of USB signal.
3. Pins are multiplexed with alternate function, and 0 Ω resistors are connected in series for the selection of functions in compatible design.
4. USB_BOOT and RGMII/RMII_RST_N cannot be pulled up to high level before the module is turned on.
5. In order to improve the signal quality, the WLAN_SDIO_CLK signal trace needs to be connected with 15–24 Ω resistor in series near the module, and the distance from the WLAN_SDIO_CLK pin to the resistor needs to be less than 5 mm.
6. To avoid the jitter of bus, pull-up resistors R0319–R0323 are needed to be added to SDIO bus. VDD_EXT should be used as the pull-up power. The resistance of these resistors are among 10–100 kΩ and not mounted by default.

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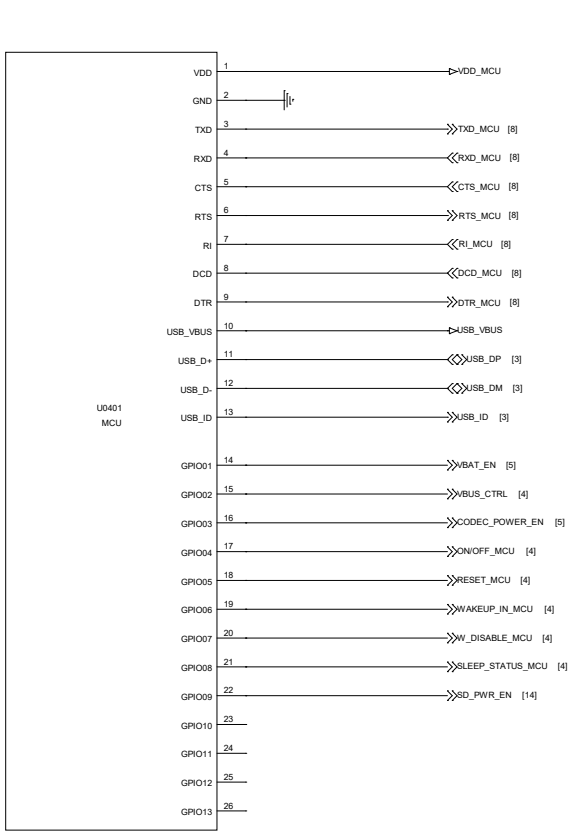
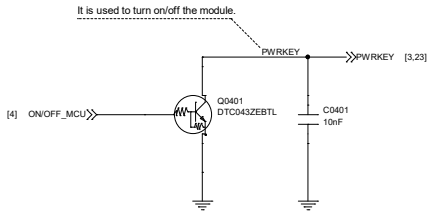
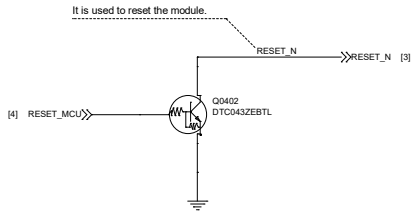
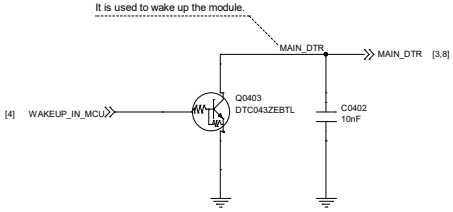
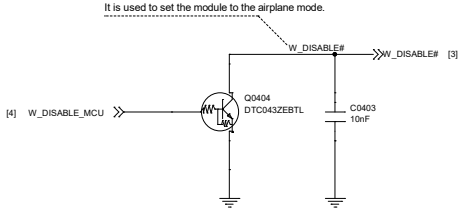
MCU Interface

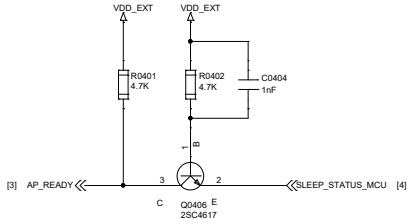


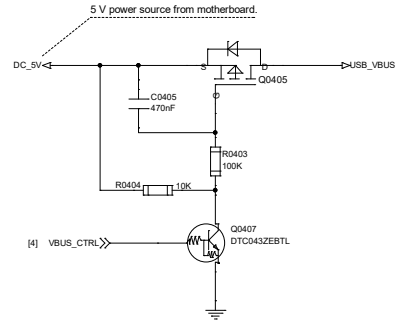












NOTE:

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V. If the GPIO interfaces of U0401 is also 1.8 V, then the related level-shifting circuit is not needed.
2. The USB interface of the module serves as a host device or slave device and supports full-speed and high-speed modes of USB 2.0. If you need to use OTG function, it is necessary to distinguish whether the USB is in master mode or slave mode by the level change of the USB_ID pin. The USB_VBUS pin of the module should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select GPIO pins which are at low level by default as the control pins for PWRKEY and RESET_N of the module. Ensure that the load capacitance on PWRKEY and RESET_N pins does not exceed 10 nF.

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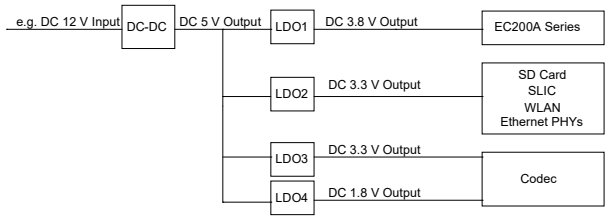
Power Supply Design

DC-DC Application

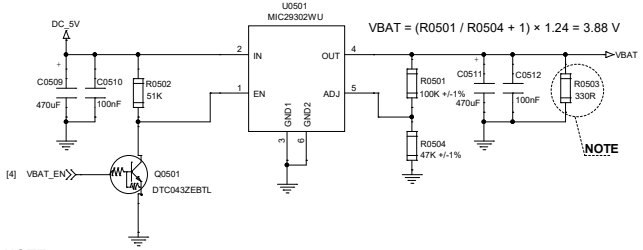
When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to 5.0 V, and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V to power the module, audio PA, Ethernet PHYs, SLIC, WLAN, SD card and Codec.

The supply current of the module must be of at least 2.8 A.



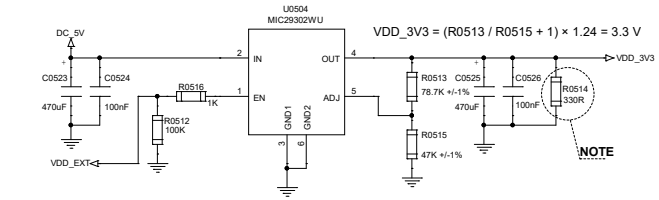
LDO Application

When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



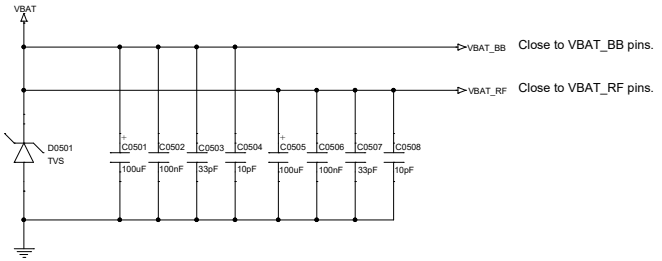
NOTE:
The recommended load current is greater than 10 mA.

Power Supply for SD Card, SLIC, WLAN and Ethernet PHYs



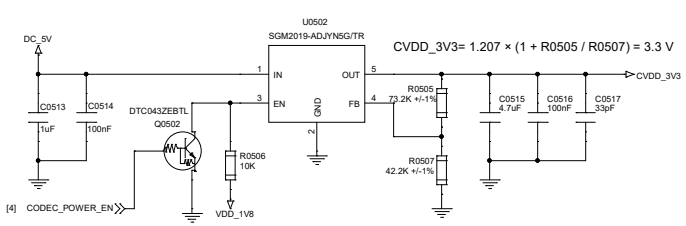
NOTE:
The recommended load current is greater than 10 mA.

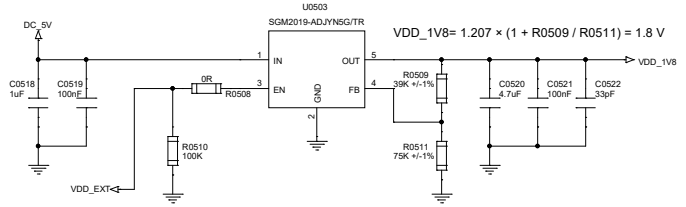
VBAT Design



NOTE:
1. The power supply should be able to provide sufficient current of at least 2.8 A for the module.
2. VBAT should be routed in star configuration to VBAT_BB and VBAT_RF pins.
3. The width of VBAT_BB trace should not be less than 1 mm; and the width of VBAT_RF trace should not be less than 2 mm.
4. The recommended operating voltage of VBAT is 3.4–4.5 V.

Power Supply for Codec





NOTE:
1.VDD_EXT and CODEC_POWER_EN are used to turn on/off VDD_1V8 and CVDD_3V3 respectively.
2.The following power-up/down sequences should be followed to ensure the audio codec works normally.
Power-up sequence: power up VDD_1V8 first, and then CVDD_3V3.
Power-down sequence: power down CVDD_3V3 first, and then VDD_1V8.

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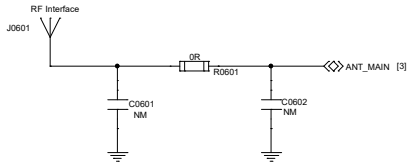
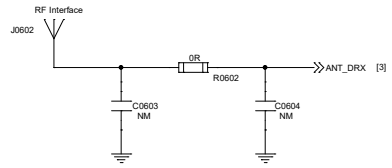
Antenna Interface Design

Main Antenna



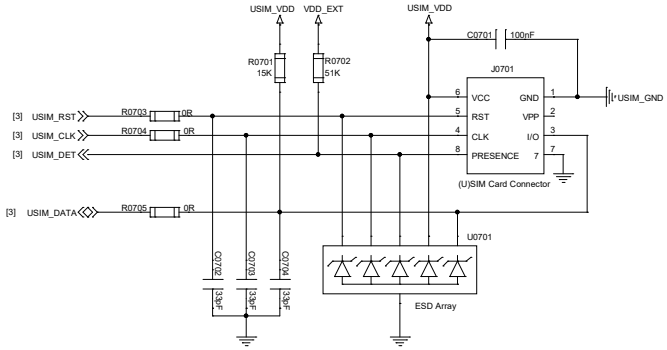
Rx-diversity Antenna



NOTE:

It is highly recommended to reserve a Π type circuit for main and Rx-diversity antennas for future debugging. The impedance of the RF signal traces must be controlled as 50 Ω when routing.

(U)SIM Interface Design

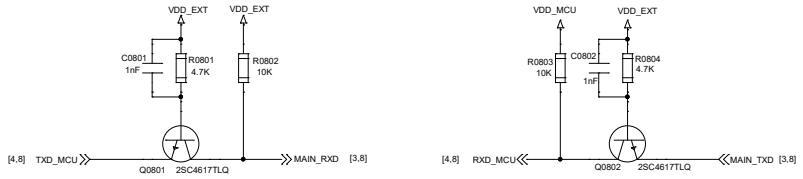


NOTE:

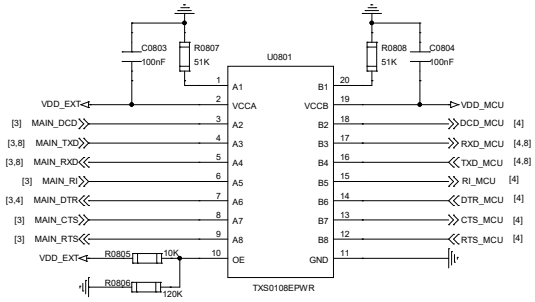
1. U0701 is recommended to be used to offer good ESD protection, and the parasitic capacitance should not be more than 15 pF.
2. The pull-up resistor R0701 can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.
3. Connect 0 Ω resistors R0703-R0705 in series between the module and (U)SIM card for debugging, and capacitors C0702-C0704 can be used to filter out RF interference.
4. C0701's capacitance should be less than 1 μF and it should be placed close to the (U)SIM card connector.
5. The GND of the (U)SIM card connector is recommended to be connected to the module's USIM_GND. In addition, USIM_GND can also be connected to the GND of your PCB directly if the PCB's GND is complete.
6. For more information about the layout of (U)SIM interface, please refer to *Quectel_EC200A_Series_QuecOpen_Hardware_Design*.

UART Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



NOTE:

1. There are two level shifting solutions: transistor solution and IC solution, and the latter one is recommended.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, please refer to the datasheet of TXS0108EPWR.
3. The transistor solution is not applicable for applications with baud rates exceeding 460 kbps. The capacitors C0801 and C0802 of 1 nF can improve the signal quality.
4. MAIN_RTS and MAIN_DTR transistor circuits are similar to that of the MAIN_RXD interface.
   MAIN_CTS, MAIN_RI and MAIN_DCD transistor circuits are similar to that of the MAIN_TXD interface.

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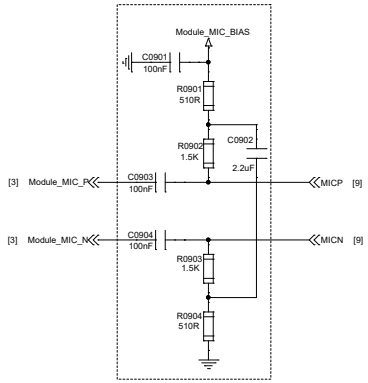
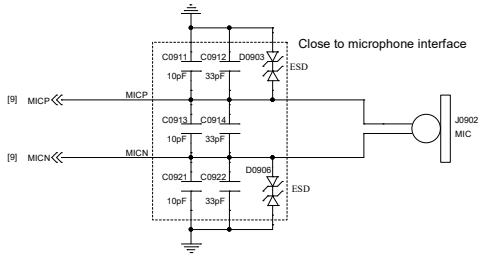
Analog Audio Design

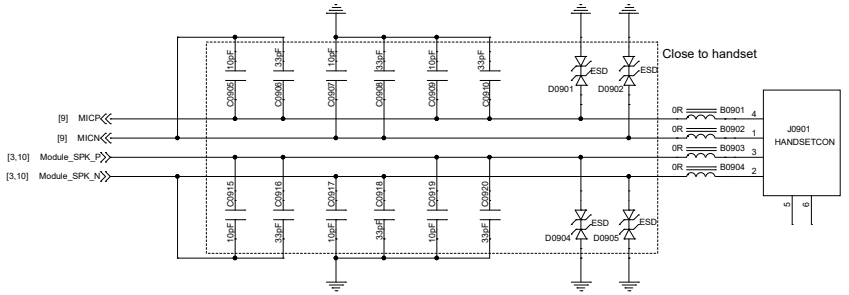
Microphone Bias Circuit



Microphone Application



Handset Application



NOTE:

1. Both the MIC and SPK signal traces need to be routed as differential pairs.
2. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from interferences.
3. In the audio design, your can choose either the analog audio or the codec.
4. 10 pF and 33 pF capacitors are used to filter TDD noises.
5. The analog output only drives handset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.

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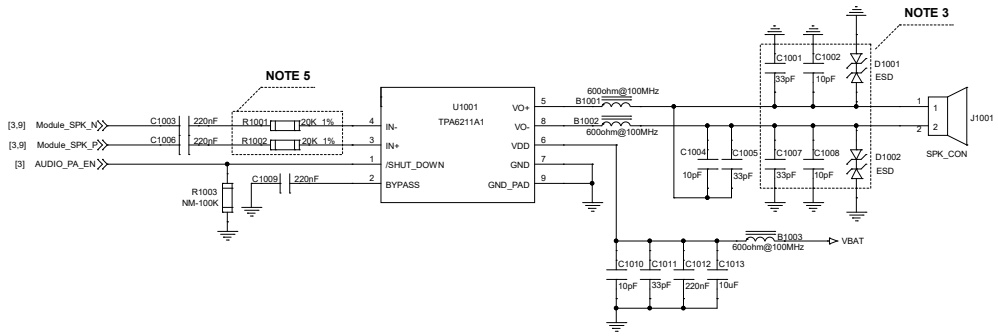
Analog Audio Design (Audio Power Amplifier)



NOTE:

1. SPK_P and SPK_N are differential output channels that can be used for external audio power amplifier.
   It is recommended to select one pin of the module to control the enable pin of the audio power amplifier to eliminate Pop noise. For more information about AUDIO_PA_EN, please contact Quectel Technical Support.
2. The amplifier model in this design is for reference only. Select the audio power amplifier with appropriate power according to actual needs.
3. Place filter capacitors and ESD protection components close to the loudspeaker.
4. The selection of ESD device is related to the selection of audio power amplifier. Ensure that the output audio voltage of audio power amplifier is within the maximum reverse working voltage range of ESD device under normal working condition to avoid damage to ESD device.
5. R1001 and R1002 can adjust the gain of the power amplifier, please refer to the datasheet of TPA6211A1 for details.

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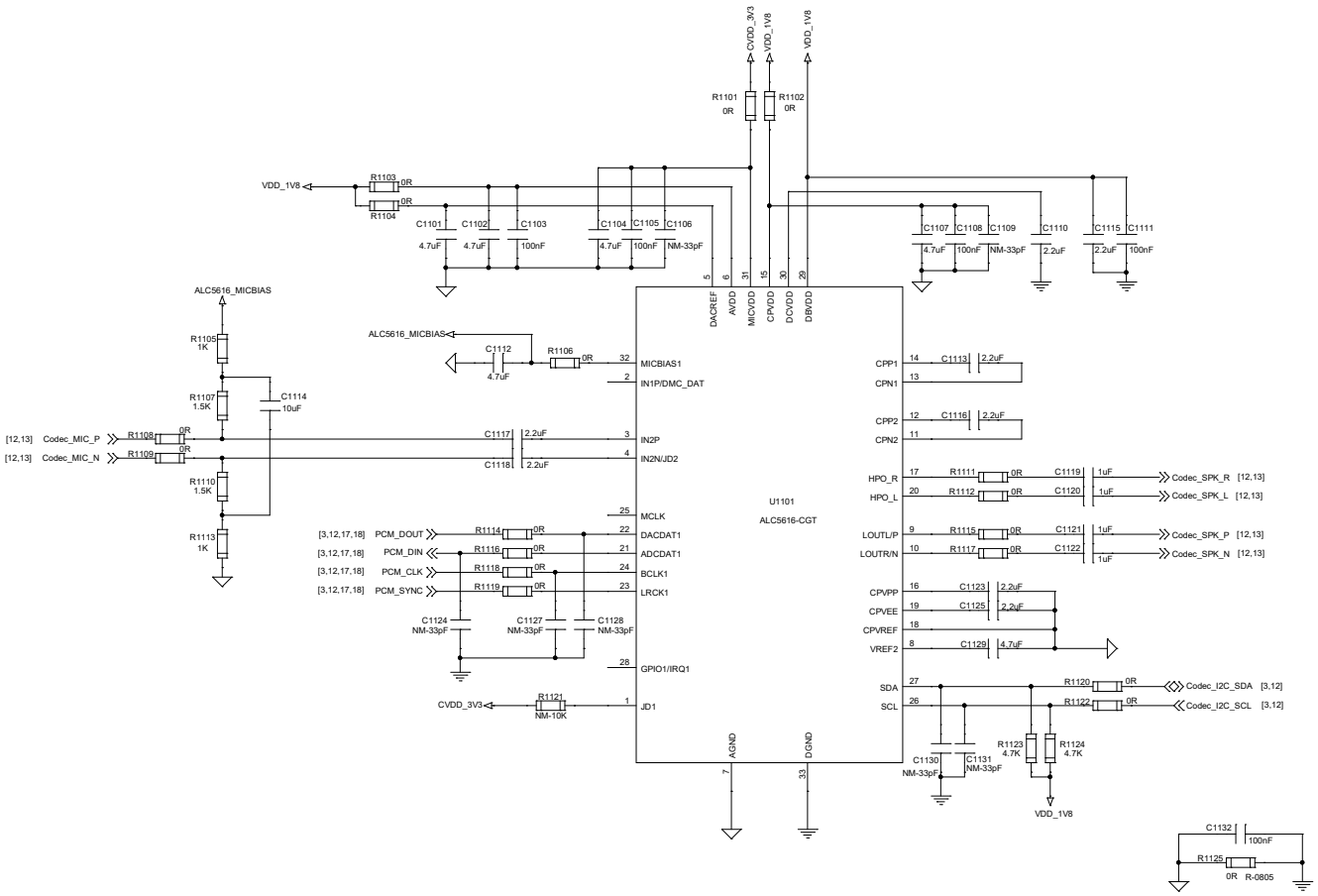
Audio Codec Design (ALC5616)



NOTE:

1. ALC5616 power-up sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD → MICVDD → software initialization.
2. ALC5616 power-down sequence: disable codec function by software → MICVDD → DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.
3. The module will automatically initialize the codec via I2C interface after it is turned on successfully, so all power supplies for the codec need to be powered on before that.
4. Pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805. For more details, please refer to Sheet "Audio Codec Interface Design".
5. For more details, please refer to the datasheet of ALC5616.

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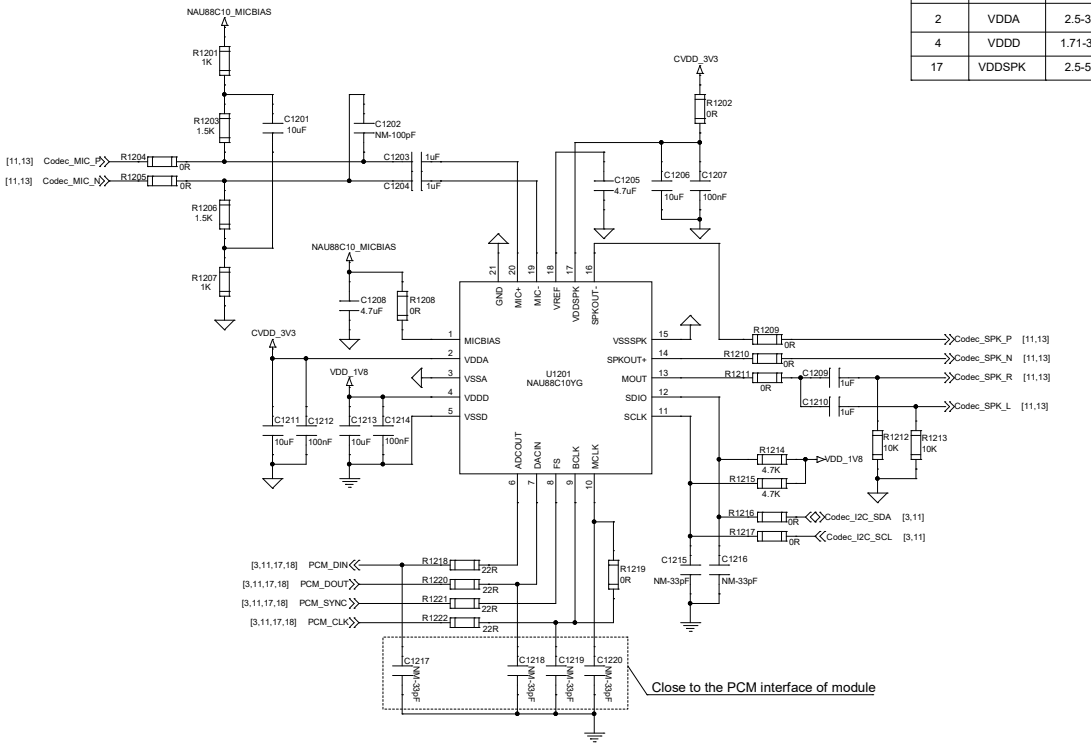
Audio Codec Design (NAU88C10YG)

Pin No.	Pin Name	Voltage	Description
2	VDDA	2.5-3.6 V	Analog VDD
4	VDDD	1.71-3.6 V	Digital VDD
17	VDDSPK	2.5-5.5 V	SPK power supply



NOTE:

1. The codec should be away from interference sources such as RF and power supplies, and the codec audio signal should be surrounded with ground as much as possible.
2. The voltage of VDDA pin must always be greater than that of VDDD.
3. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805. For more details, please refer to sheet “Audio Codec Interface Design”.
4. For more details, please refer to the datasheet of NAU88C10YG.

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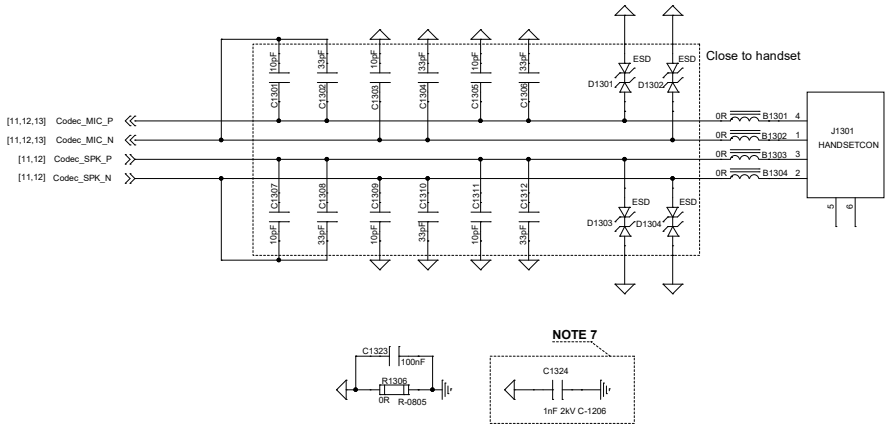
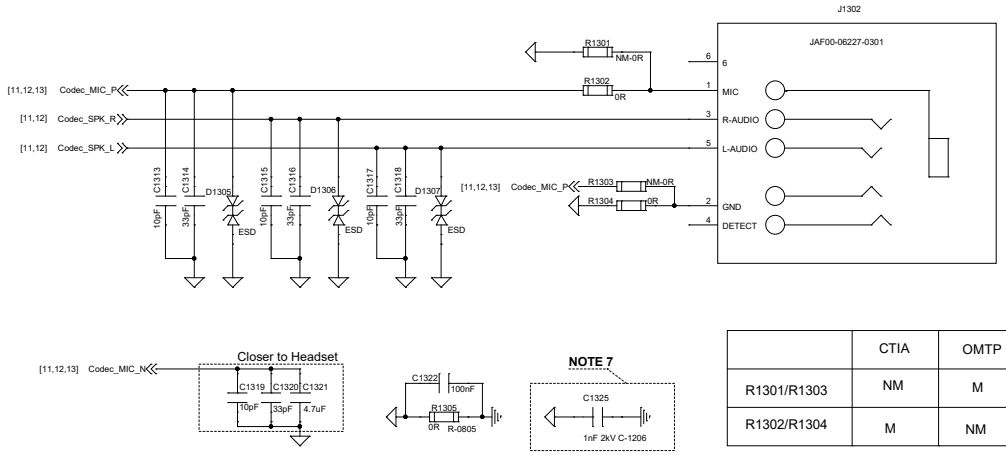
Audio Codec Interface Design

Handset Application



Headset Application

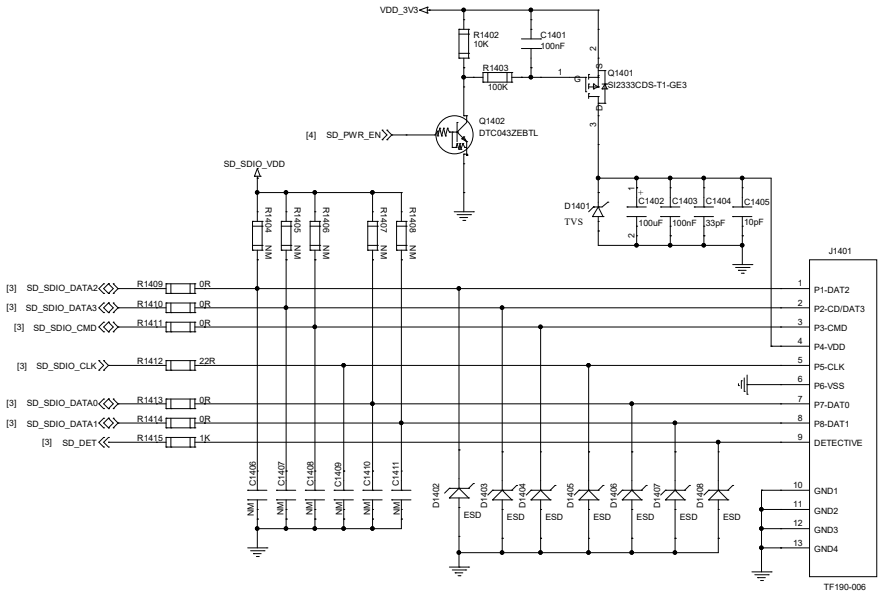


	CTIA	OMTP
R1301/R1303	NM	M
R1302/R1304	M	NM

NOTE:

1. The codec analog output can drive handset and headset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.
2. In handset applications, both the MIC and SPK signal traces need to be routed as differential pairs.
3. In headset applications, route the MIC signal traces as a differential pair.
4. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noises such as clock and DC-DC signals.
5. Pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805 (a via directly to main GND).
6. You can choose either ALC5616 or NAG88C10YG in audio codec design.
7. C1324 and C1325 capacitors are used for electrostatic protection, and they need to be placed close to D1301, D1302, D1303, D1304 and D1305, D1306, D1307 respectively, and connected to the main ground nearby.

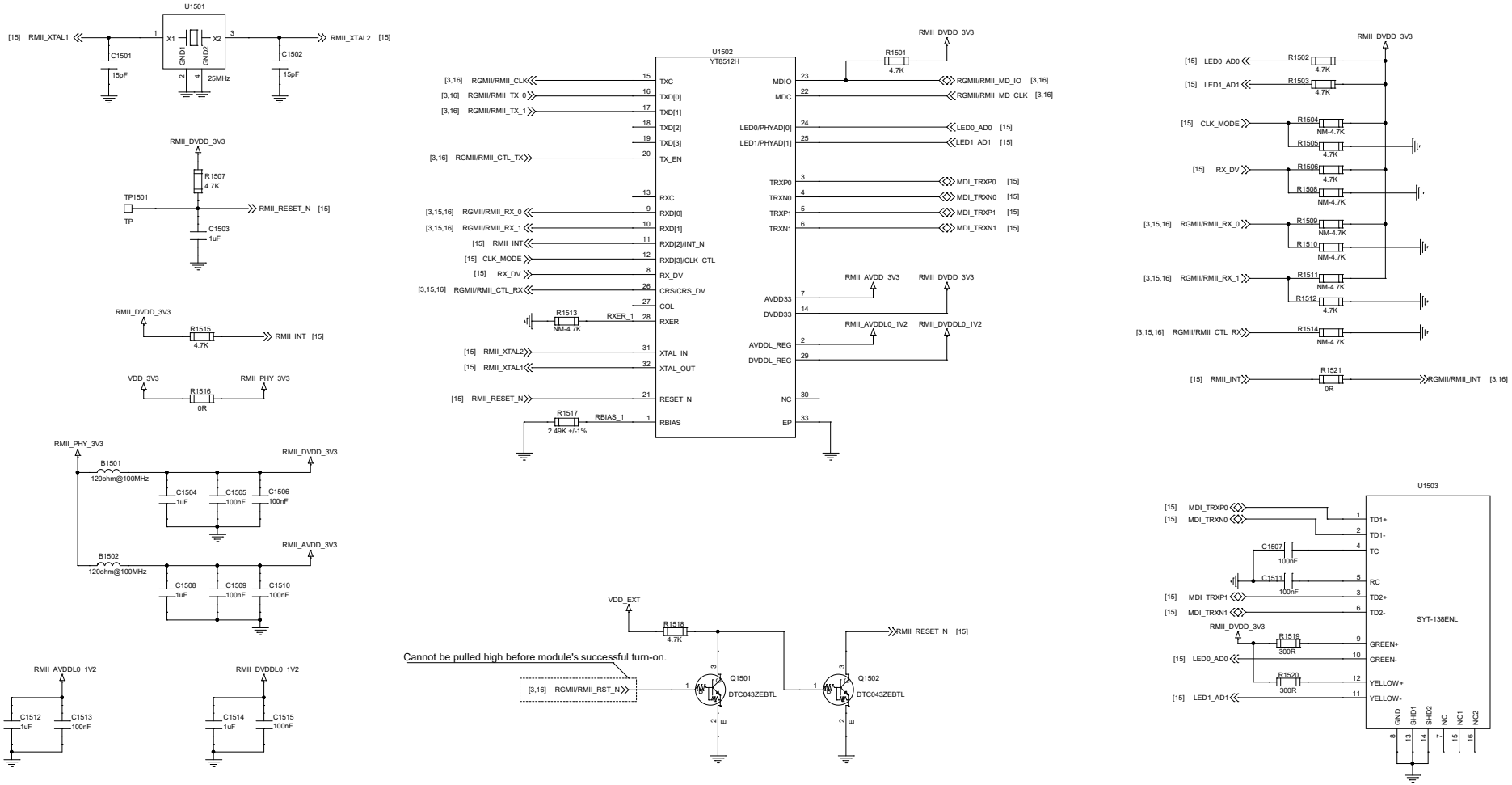
SD Card Interface Design



NOTE:

1. The SD_SDIO_VDD can only be used for the pull-up resistor of SDIO bus and its maximum output current is 50 mA.
2. The voltage range of SD card power supply VDD is 2.7–3.6 V and a sufficient current of at least 0.8 A should be provided.
3. To avoid the jitter of bus, pull-up resistors R1404–R1408 are needed to be added to SDIO bus. SD_SDIO_VDD should be used as the pull-up power. The resistance of these resistors are among 10–100 kΩ and the recommended value is 100 kΩ.
4. To adjust the signal quality, it is recommended to add resistors R1409–R1414 in series between the module and the SD card connector. The recommended resistance of R1412 is 22 Ω and the others is 0 Ω. The bypass capacitors C1406–C1411 are reserved and not mounted by default.
5. To offer good ESD protection, it is recommended to add ESD protective device on SD card pins near the SD card connector with junction capacitance less than 8 pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, as well as noisy signals such as clock and DC-DC signals.
7. It is important to route the SDIO signal traces with ground surrounded. The impedance of SDIO data trace is 50 Ω (±10 %).
8. It is recommended to keep the traces of SD_SDIO_CLK, SD_SDIO_DATA[0:3] and SD_SDIO_CMD with equal length (the difference among them is less than 1 mm) and the total routing length needs to be less than 50 mm.
9. Make sure the adjacent trace spacing is twice the trace width and the bus capacitance is less than 15 pF.

RMII Design (100 Mbps Ethernet)



NOTE:

1. Keep data signal traces and control signal traces of RMII interfaces far away from sensitive circuits and signals such as RF signals, analog signals, and noise signals generated by clock, DC-DC.
2. The single-ended impedance of RMII data trace is 50 Ω ±10 %.
3. The length difference of RGMII/RMII_TX_[0:1] and RGMII/RMII_CTL_TX should be less than 2 mm, and the spacing between the signal traces should be larger than twice the trace width. Similarly, the length difference of RGMII/RMII_RX_[0:1], RGMII/RMII_CTL_RX and RGMII/RMII_CLK should be less than 2 mm, and the spacing between the signal traces should be larger than twice the trace width.
4. Spacing between Tx bus and Rx bus is larger than 2.5 times of the trace width.
5. Spacing between Tx/Rx bus and other signals is larger than 3 times of the trace width.
6. It is recommended to use a level-shifting chip without pull-up for the level-shifting circuit.
7. For more details, please refer to the datasheet of YT8512H.

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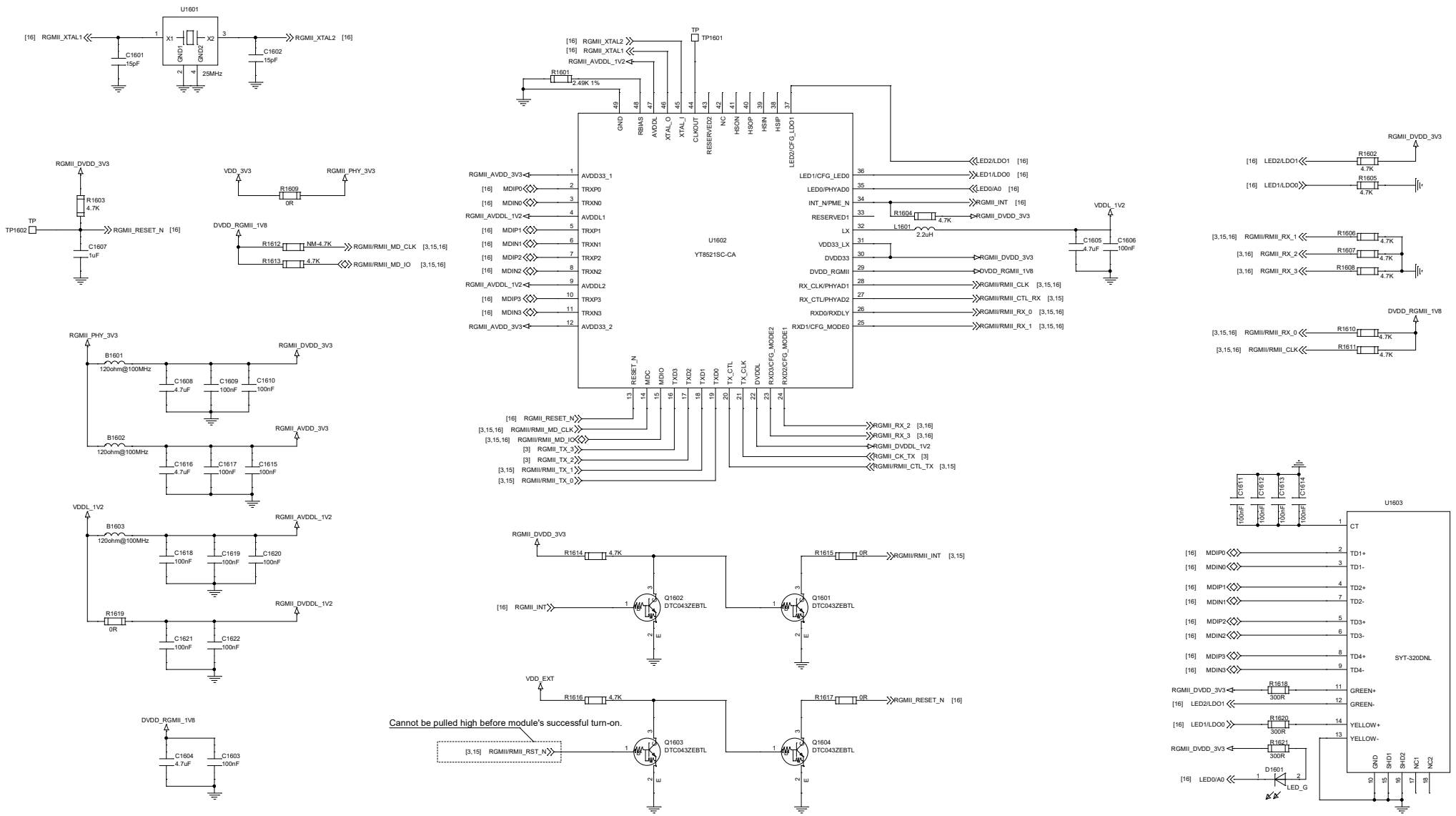
RGMII Design (1000 Mbps Ethernet)



NOTE:

1. Keep data signal traces and control signal traces of RGMII interfaces far away from sensitive circuits and signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
2. The single-ended impedance of RGMII data trace is 50 Ω ±10 %.
3. The length difference of RGMII/RMII_TX_[0:1], RGMII_TX_[2:3], RGMII/RMII_CTL_TX and RGMII_CK_TX should be less than 0.25 mm, and the spacing between the signal traces should be larger than twice the trace width. Similarly, the length difference of RGMII/RMII_RX_[0:1], RGMII_RX_[2:3], RGMII/RMII_CTL_RX and RGMII/RMII_CLK should be less than 0.25 mm, and the spacing between the signal traces should be larger than twice the trace width.
4. Spacing between Tx bus and Rx bus is larger than 2.5 times of the trace width.
5. Spacing between Tx/Rx bus and other signals is larger than 3 times of the trace width.
6. It is recommended to use a level shifting chip without pull-up for the level-shifting circuit.
7. For more details, please refer to the datasheet of YT8521SC.

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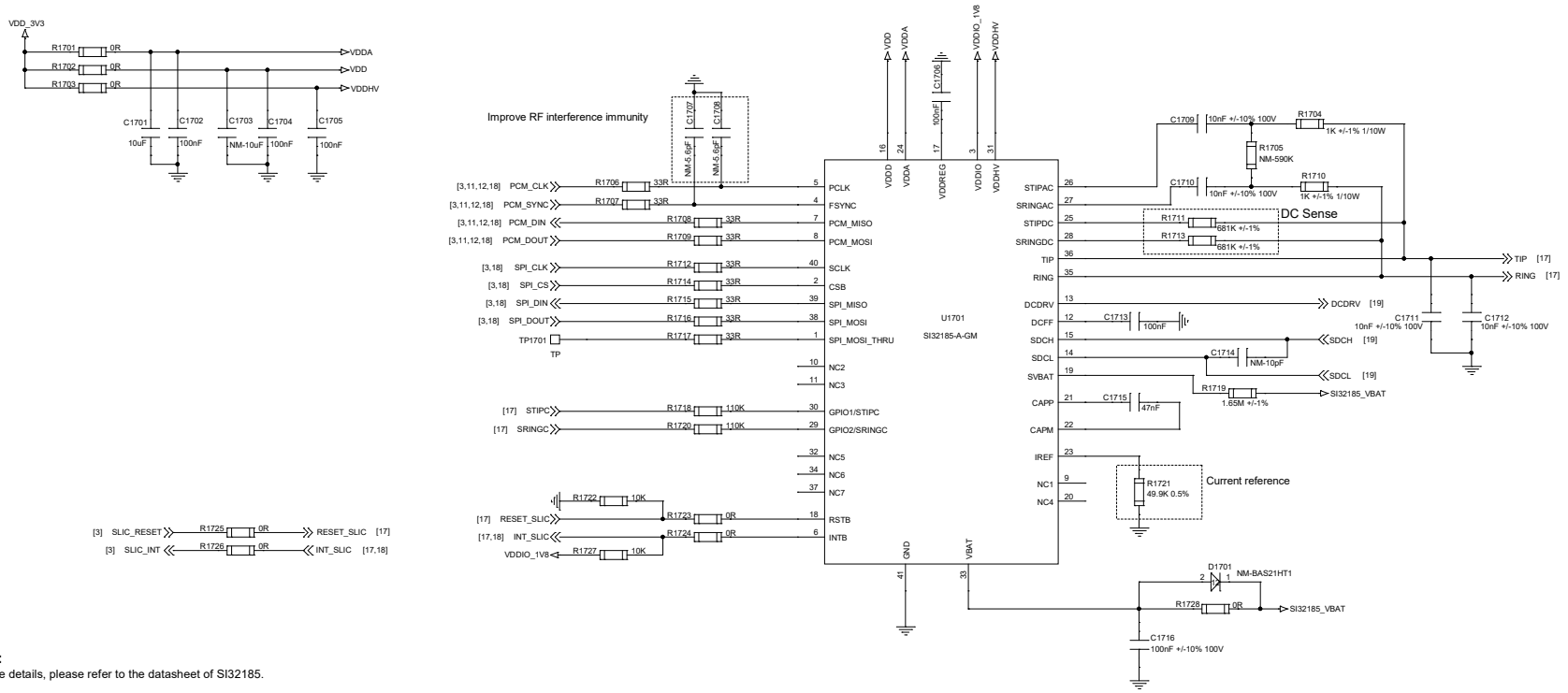
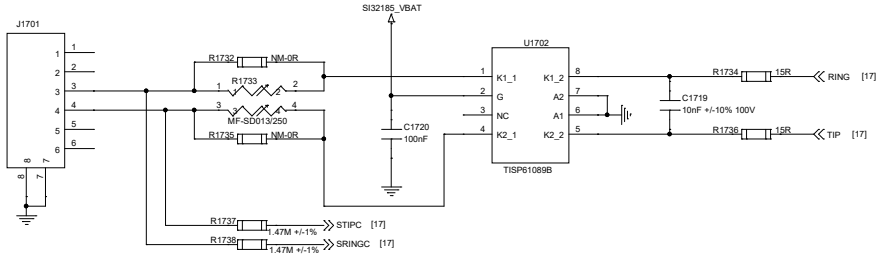
SLIC Design (SI32185)

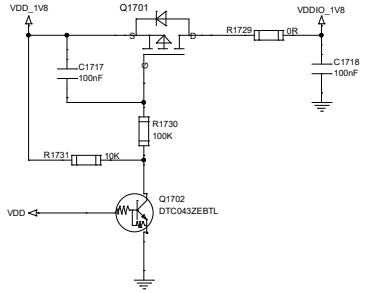


NOTE:
For more details, please refer to the datasheet of SI32185.

High Voltage Ringing SLIC Protector



Power Supply Timing Control



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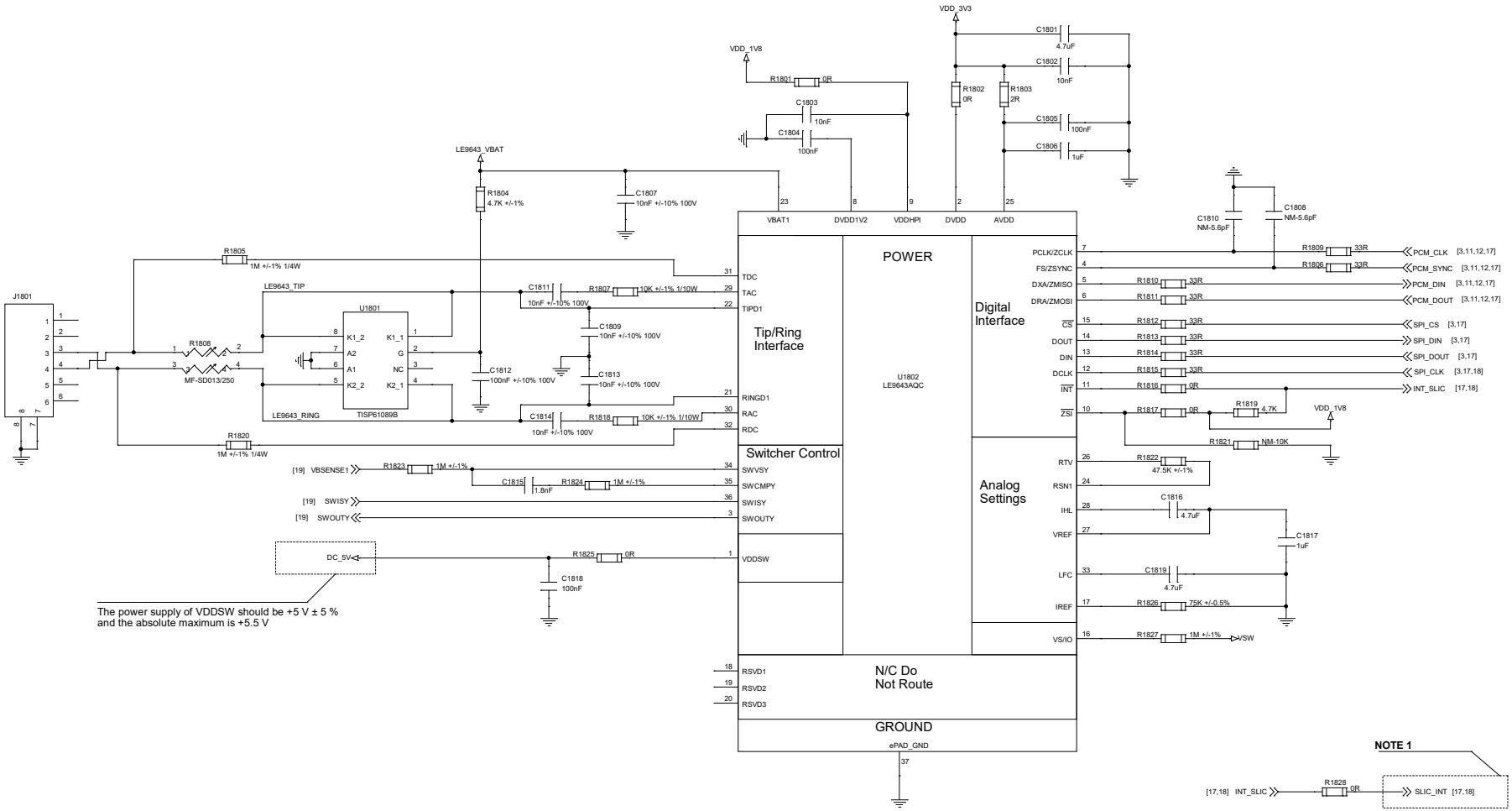
SLIC Design (LE9643)



NOTE:

1. If you need SLIC interrupt function, you need to connect INT_SLIC to pin 1 of the module, and modify the GPIO configuration of pin 1 of the module through software.
2. For more details, please refer to the datasheet of LE9643.

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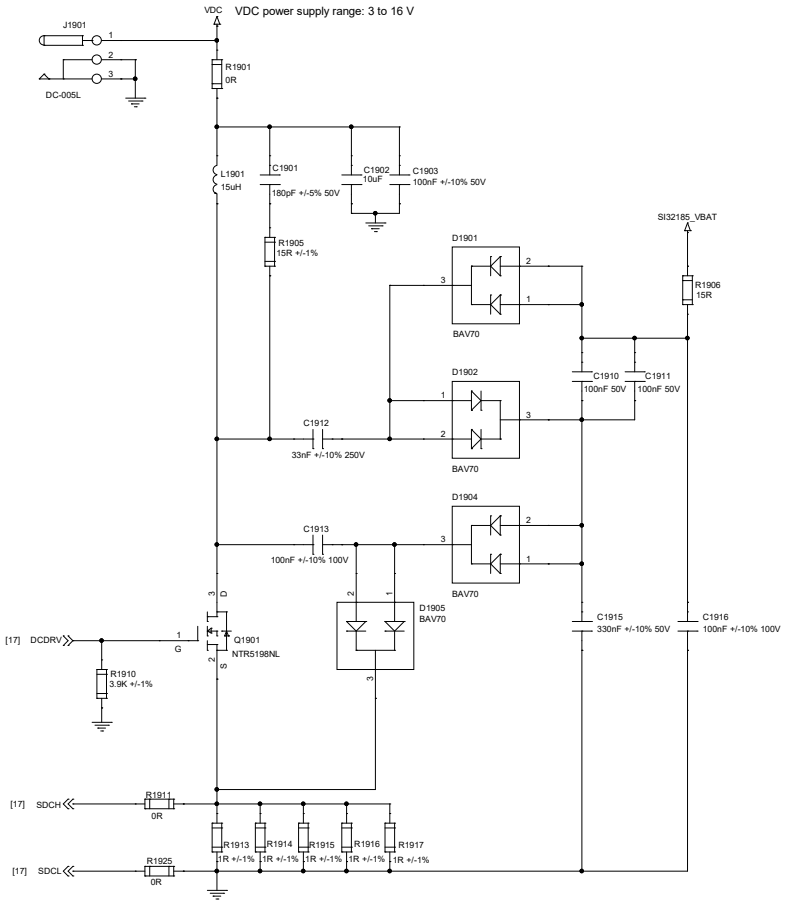
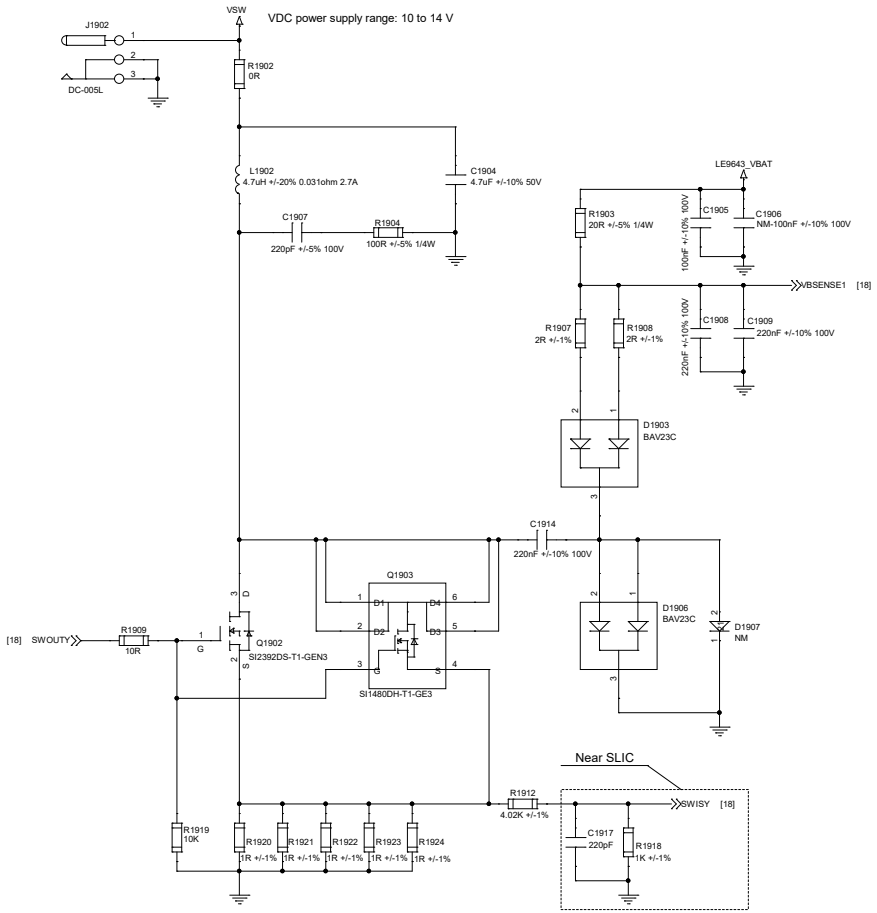
SLIC Power Supply Design

SI32185 Power Supply Design



LE9643 Power Supply Design



NOTE:

R1910 must be reserrved to protect Q1901 from damage.

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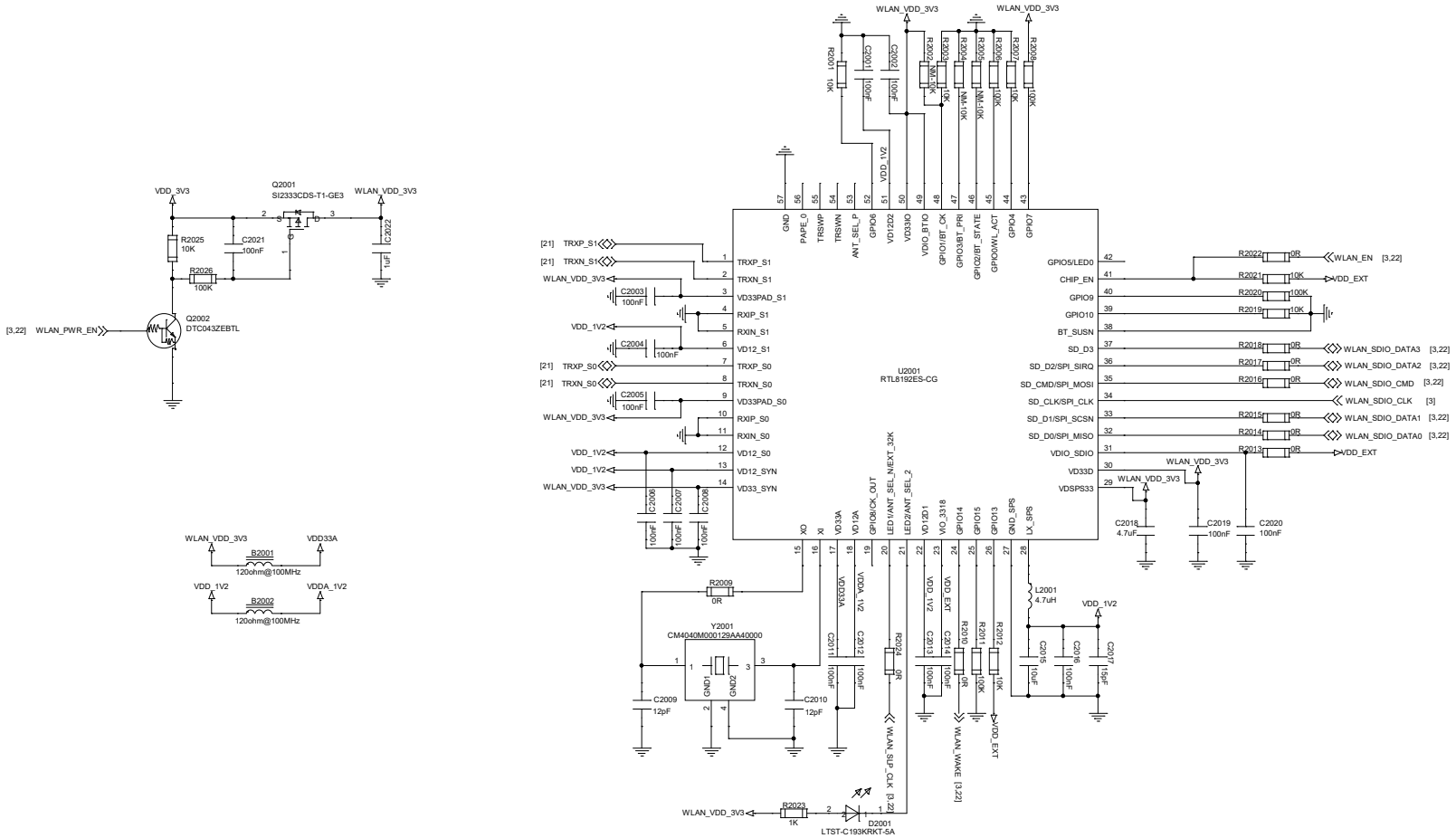
WLAN Design (RTL8192)



NOTE:

1. In order to adjust the signal quality, it is recommended to add 0 Ω resistors R2014–R2018 in series between the module and the RTL8192.
2. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, as well as noisy signals such as clock and DC-DC signals.
3. It is important to route the SDIO signal traces with ground surrounded. The impedance of SDIO data trace is 50 Ω (±10 %).
4. It is recommended to keep the traces of WLAN_SDIO_CLK, WLAN_SDIO_DATA[0:3] and WLAN_SDIO_CMD with equal length (the difference among them is less than 1 mm) and the total routing length needs to be less than 50 mm.
5. Make sure the adjacent trace spacing is twice the trace width and the bus capacitance is less than 15 pF.

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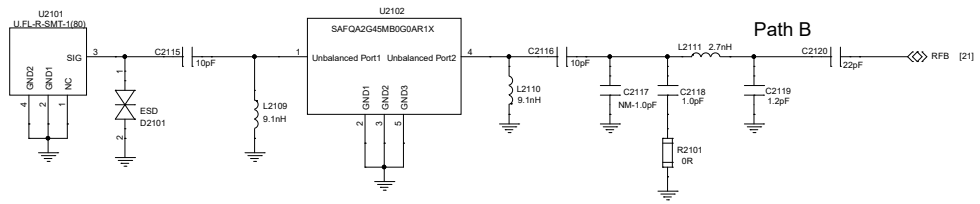
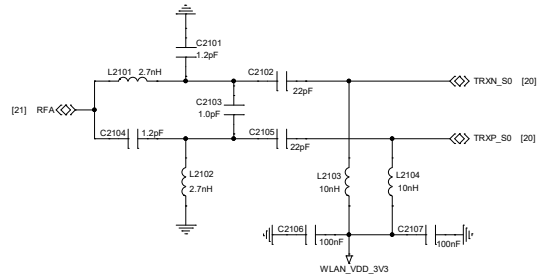
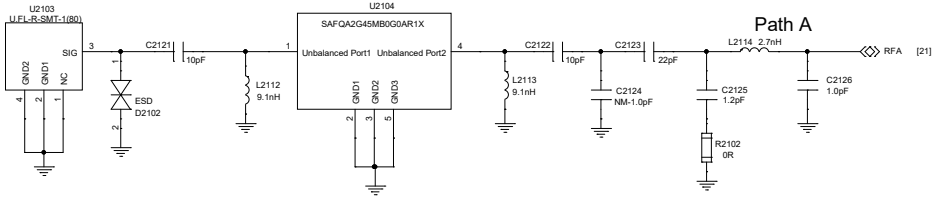
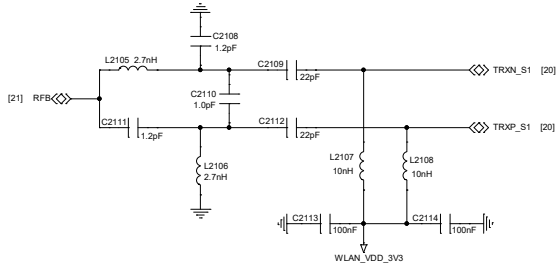
RTL8192 RF Design









NOTE:

The impedance of the RF signal traces must be controlled as 50 Ω when routing.

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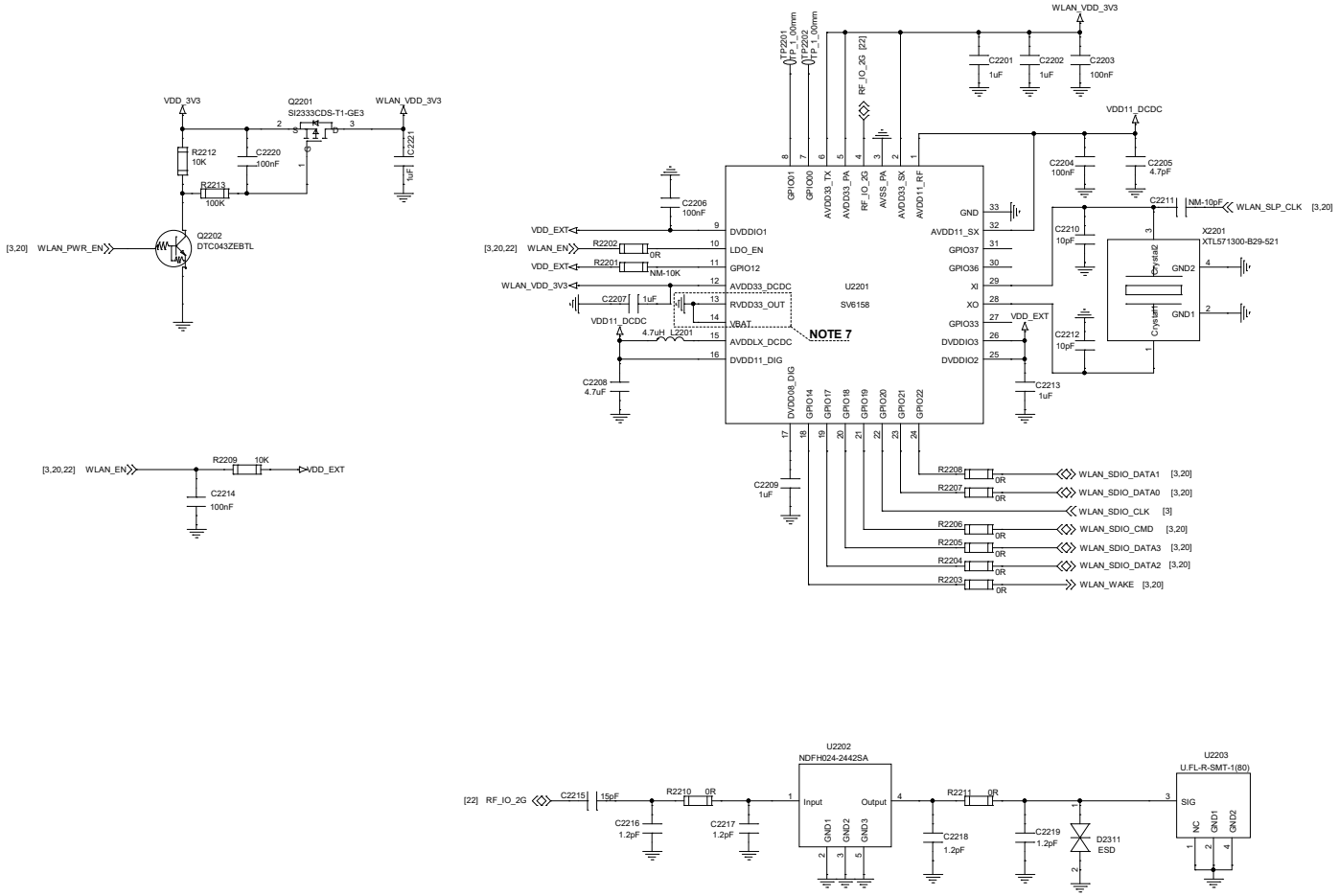
WLAN Design (SV6158)



NOTE:

1. In order to adjust the signal quality, it is recommended to add 0 Ω resistors R2203–R2208 in series between the module and the SV6158.
2. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, as well as noisy signals such as clock and DC-DC signals.
3. It is important to route the SDIO signal traces with ground surrounded. The impedance of SDIO data trace is 50 Ω (±10 %).
4. It is recommended to keep the traces of WLAN_SDIO_CLK, WLAN_SDIO_DATA[0:3] and WLAN_SDIO_CMD with equal length (the difference among them is less than 1 mm) and the total routing length needs to be less than 50 mm.
5. Make sure the adjacent trace spacing is twice the trace width and the bus capacitance is less than 15 pF.
6. The impedance of the RF signal traces must be controlled as 50 Ω when routing.
7. In 5 V application, VBAT connects to 5 V, and RVDD33 can provide 3.3 V. In 3.3 V application, VBAT connects to 0 V, and RVDD33 is connected to 0 V as well.

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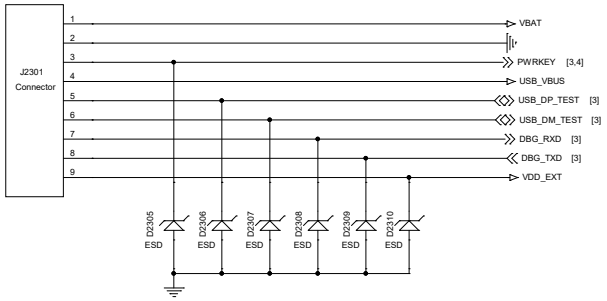
Other Designs

Indicators

NOTE:

1. The STATUS is an open drain output pin.
2. For more details about STATUS and NET_STATUS, please refer to *Quectel_EC200A_Series_QuecOpen_Hardware_Design*.
3. If the low current consumption is required when your device is in sleep mode, replace the power supply VBAT of the STATUS and NET_STATUS indicators with external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

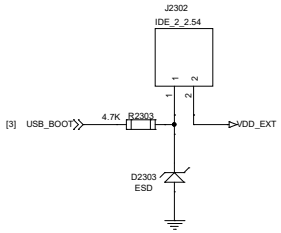
Reserved Test Points



NOTE:

1. Test points for both USB and debug UART interfaces are reserved for capturing logs.
2. Test points for USB interface can also be reserved for firmware upgrade.
3. The junction capacitance of the ESD protection components on USB data traces should be less than 2 pF.
4. The debug UART interface supports 1.8 V power domain, and a voltage-level translator should be used if the power domain of your application is 3.3 V.

USB_BOOT Interface



NOTE:

1. It is recommended to reserve the USB_BOOT interface design.
2. USB_BOOT is kept open by default.
   Pull up USB_BOOT to VDD_EXT to make the module enter emergency download mode before it is turned on.
   In this mode, the module supports firmware upgrade over USB interface.

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