UC200A-GL

Reference Design

UMTS/HSPA+ Module Series

Version: 1.0

Date: 2023-03-03

Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2022-10-19	Coco CHEN	Creation of the document
1.0	2023-03-03	Coco CHEN	First official release

Contents

1 Reference Design

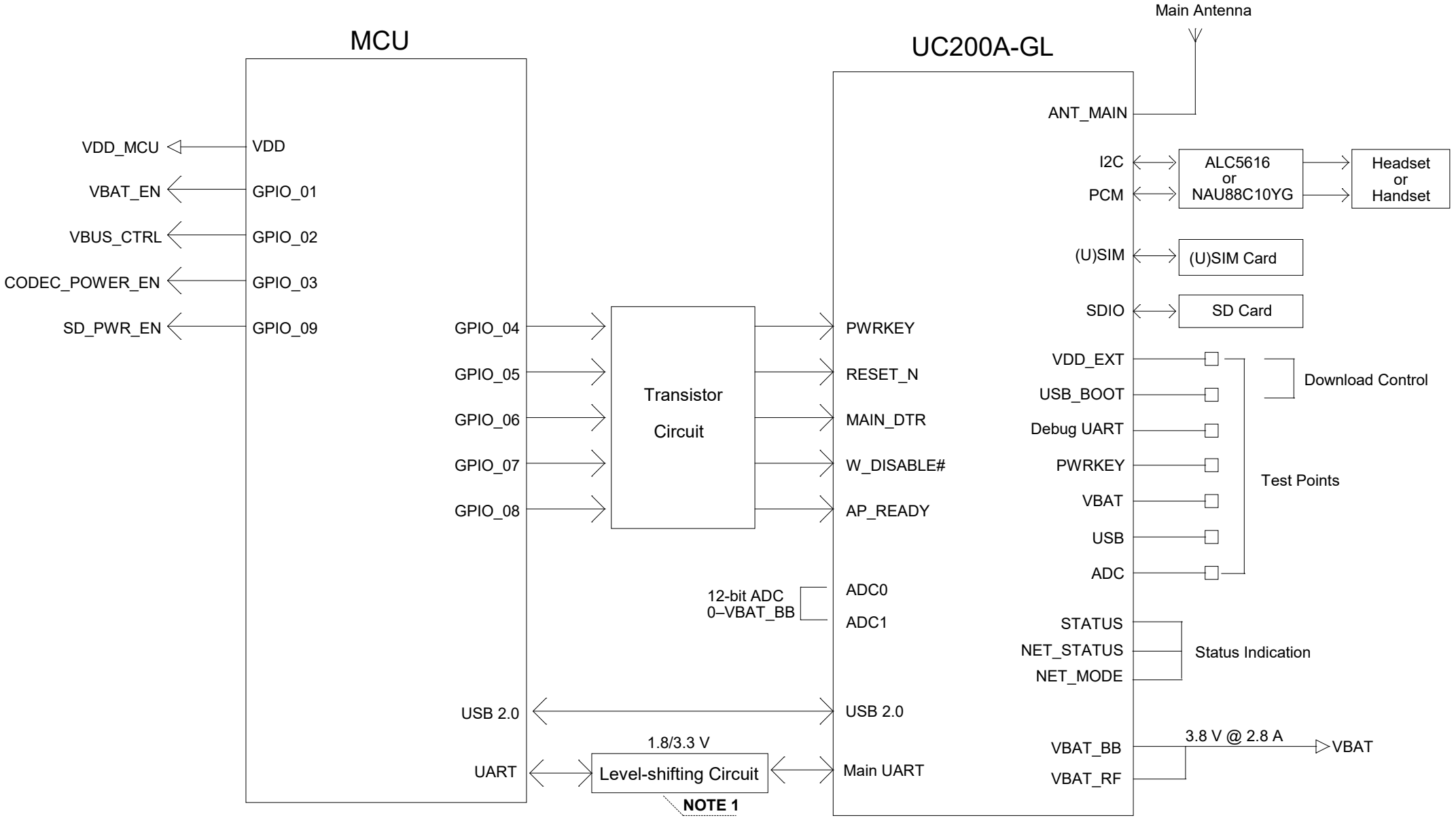
1.1. Introduction

This document provides the reference design for Quectel UC200A-GL module, including the design of power supply, module interfaces, (U)SIM interface, SD card interfaces and audio interfaces, etc.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



NOTE:

1. A level-shifting circuit or a voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.
2. The power supply should be able to provide sufficient current up to 2.8 A for the module.

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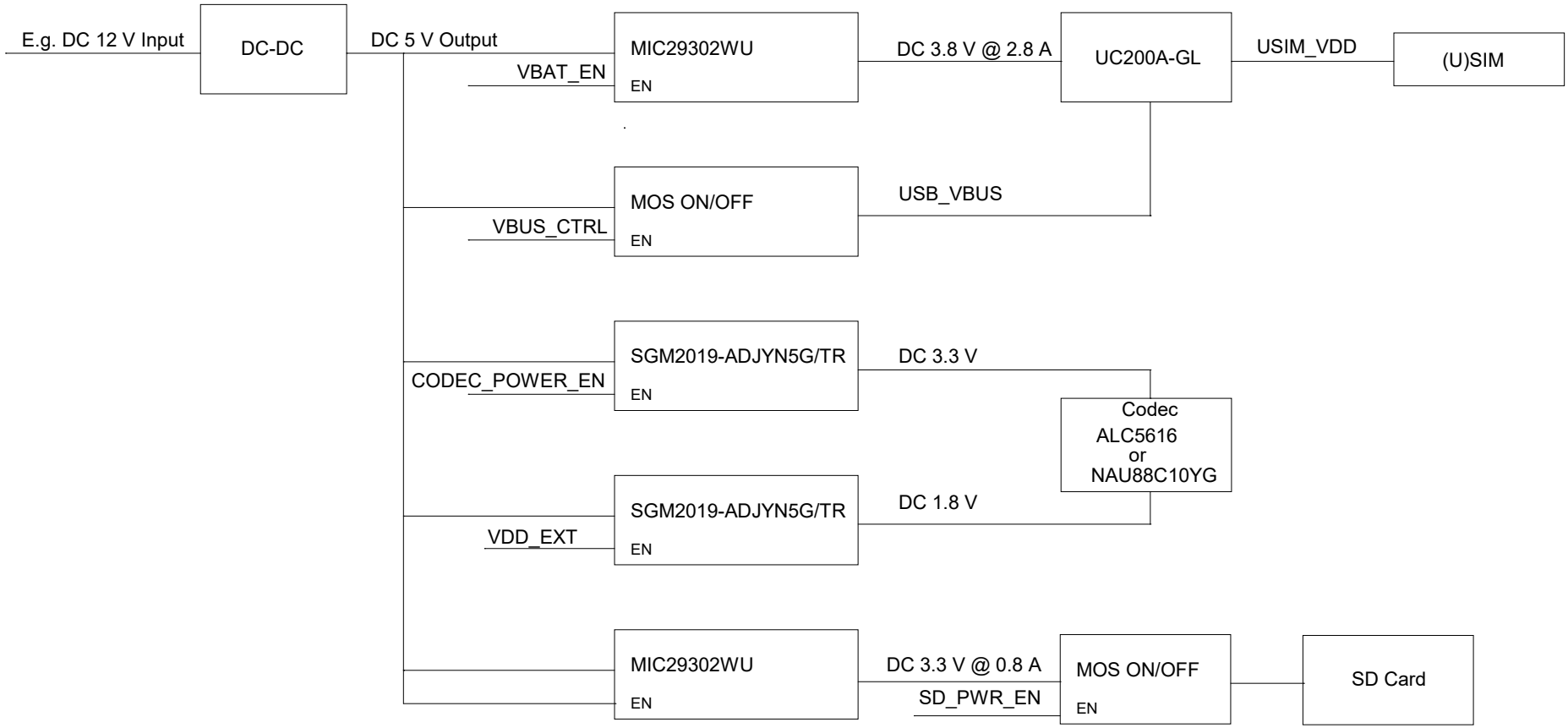
Power System Block Diagram



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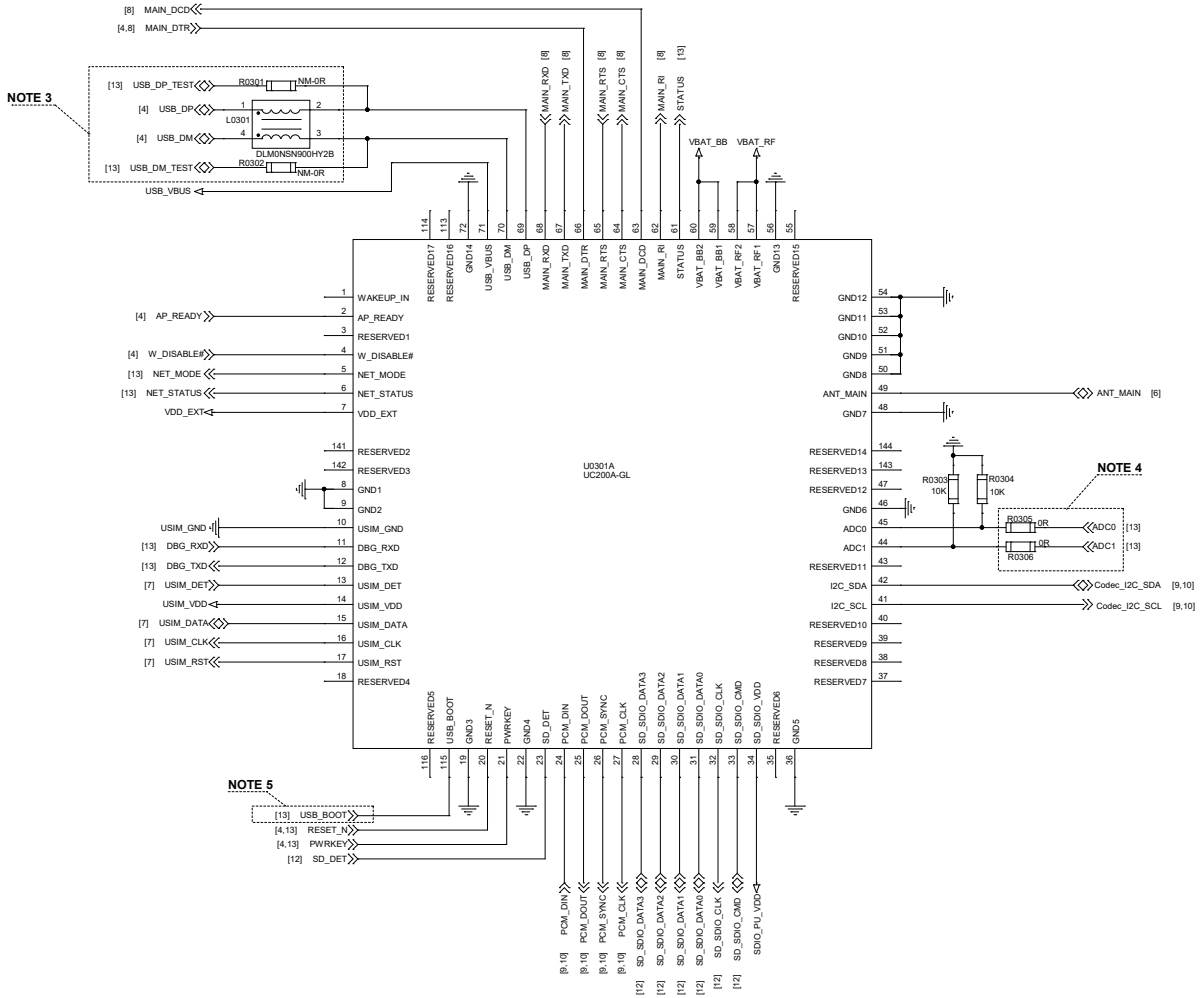
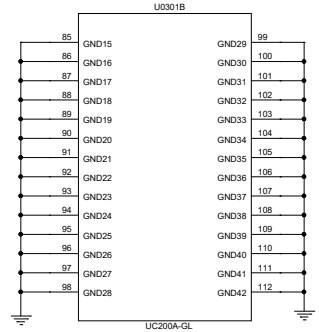
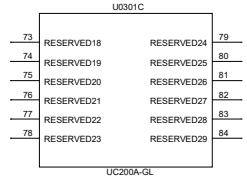
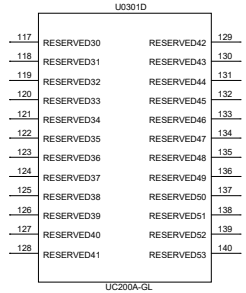
Module Interfaces









NOTE:

1. All GND pins should be connected to the ground, and keep unused and RESERVED pins unconnected.
2. Ensure there is a complete reference ground plane below the module, and the ground plane should be placed as close to the module layer as possible.
   Other traces cannot be routed on the first layer below the module.
3. A common mode choke L0301 is recommended to be added in series between the module and your MCU in order to suppress EMI spurious transmission.
   Meanwhile, it is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the extra stubs of the trace.
   L0301 and the two resistors R0301 and R0302 should be placed closed to the module for the integrity of USB signal.
4. It is recommended to use the resistor divider circuit for ADC application. A voltage divider with resistance of less than 100 kΩ should be used for ADC interface application.
5. USB_BOOT cannot be pulled up before the module starts up successfully.

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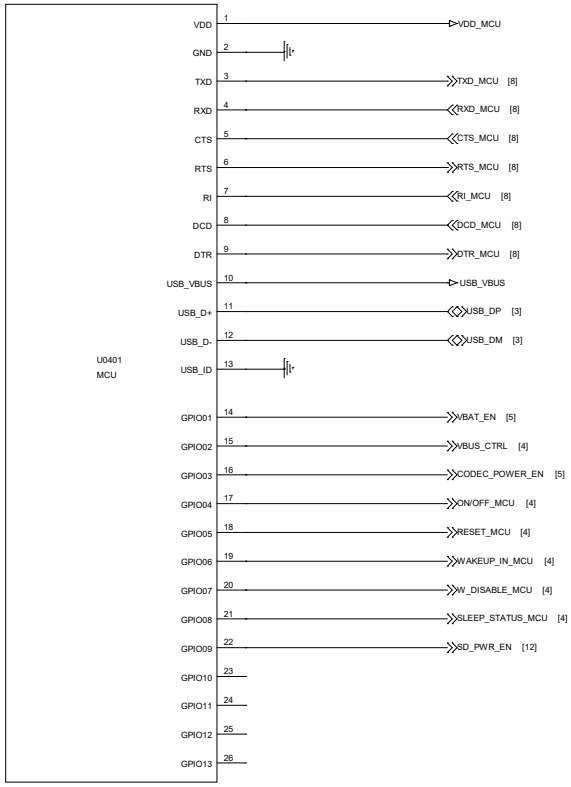
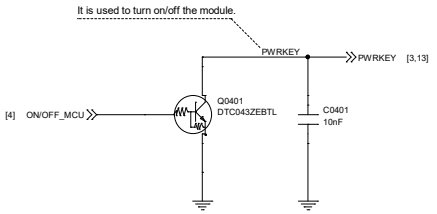
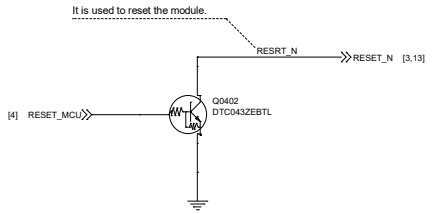
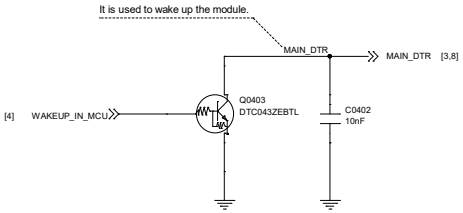
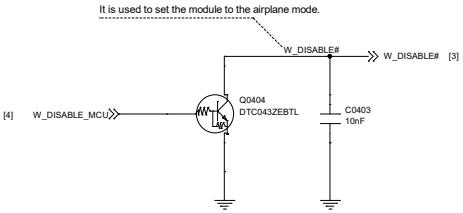
MCU Interfaces

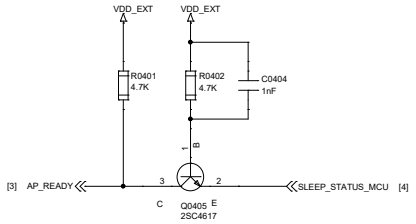


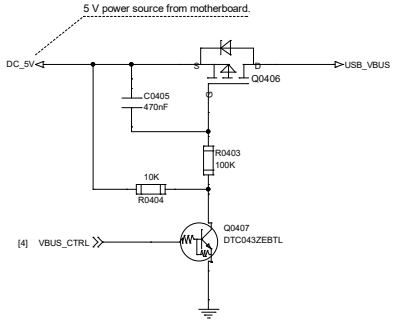












NOTE:

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V. If the GPIO interfaces of U0401 is also 1.8 V, then the related level-shifting circuit is not needed.
2. The USB interface of the module only serves as a slave device and supports full-speed and high-speed modes of USB 2.0. To communicate with the USB interface, MCU needs to support USB host mode or OTG function.

   The USB_VBUS pin of the module should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select GPIO pins which are at low level by default as the control pins for PWRKEY and RESET_N of the module.

   Ensure that the maximum load capacitance does not exceed 10 nF on PWRKEY and RESET_N pins.

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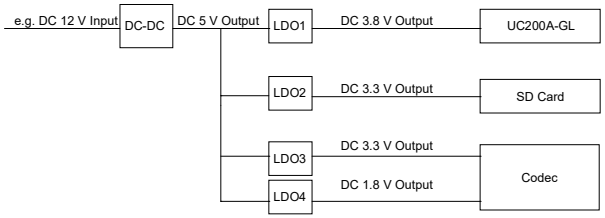
Power Supply Design

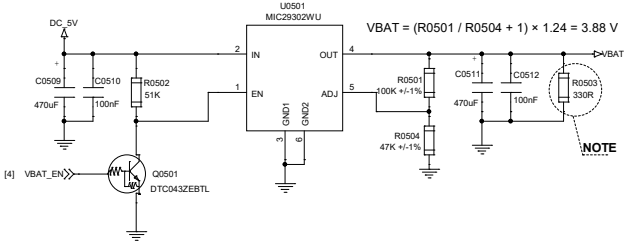
DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert a high input voltage into a 5.0 V output, and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V voltages to power the module, SD card and codec.



LDO Application

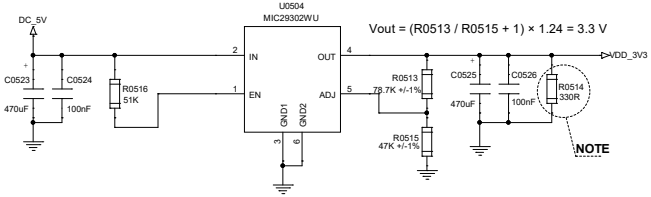
When the input voltage is below 7.0 V, use a LDO to convert it to 3.8 V.



NOTE:

The recommended load current is greater than 10 mA.

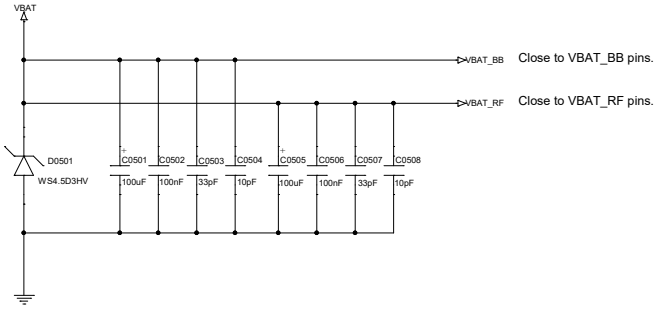
Power Supply for SD Card



NOTE:

The recommended load current is greater than 10 mA.

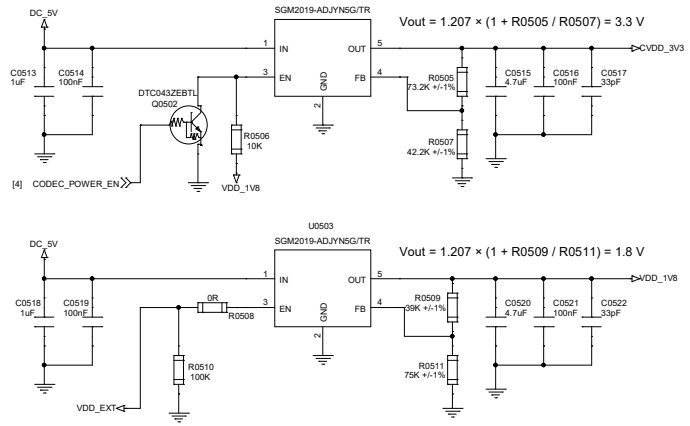
VBAT Design



NOTE:

1. The power supply should be able to provide sufficient current up to 2.8 A for the module.
2. VBAT should be routed in star configuration to VBAT_BB and VBAT_RF pins.
3. The width of VBAT_BB trace should be not less than 1 mm and the width of VBAT_RF trace should be not less than 2 mm.
4. The recommended operating voltage of VBAT is 3.4–4.5 V and the typical value is 3.8 V.

Power Supply for Codec



NOTE:

1. VDD_EXT and CODEC_POWER_EN are used to turn on/off VDD_1V8 and VDD_3V3 respectively.
2. The following power-up/down sequences should be followed to ensure the audio codec works normally.

   Power-up sequence: power up VDD_1V8 first, and then VDD_3V3.

   Power-down sequence: power down VDD_3V3 first, and then VDD_1V8.

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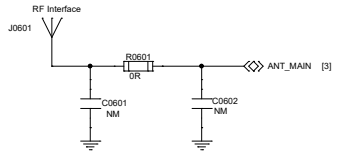
Antenna Interface Design

Main Antenna



NOTE:

1. It is recommended to reserve a Π-type circuit for main antenna for future debugging.
2. The impedance of the RF signal traces must be controlled as 50 Ω when routing.

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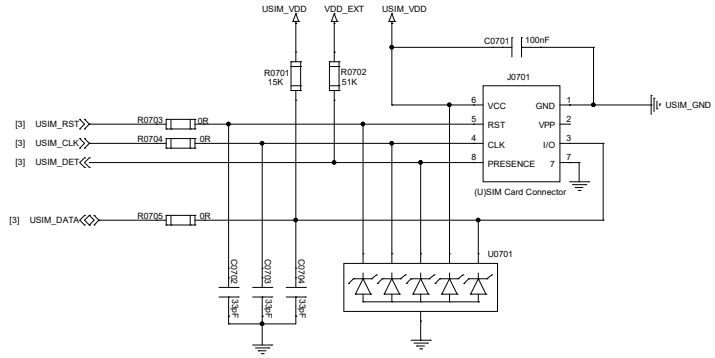
(U)SIM Interface Design

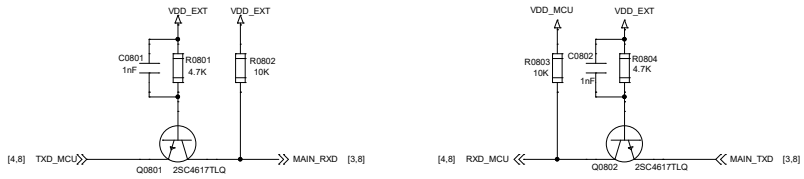


NOTE:

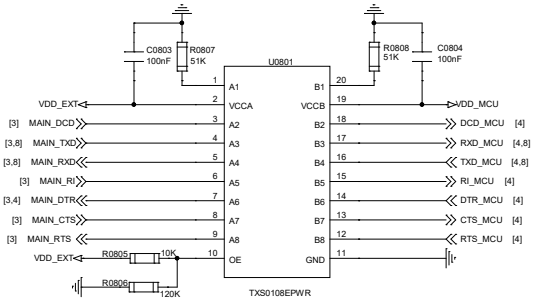
1. U0701 is recommended to be used to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.
2. The pull-up resistor R0701 can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.
3. R0703–R0705 in series between the module and (U)SIM card are used for debugging, and capacitors C0702–C0704 are used to filter out RF interference.
4. C0701 whose capacitance should be less than 1 μF must be placed close to the (U)SIM card connector.
5. The GND of the (U)SIM card connector is recommended to be connected to the GND layer directly.
6. For more information about the layout of (U)SIM interface, see the hardware design document of the module.

UART Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, see the datasheet of TXS0108EPWR.
3. The level-shifting circuit solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C0801 and C0802 of 1 nF can improve the signal quality.
4. MAIN_RTS and MAIN_DTR level-shifting circuits are similar to that of MAIN_RXD.

   MAIN_CTS, MAIN_RI and MAIN_DCD level-shifting circuits are similar to that of MAIN_TXD.

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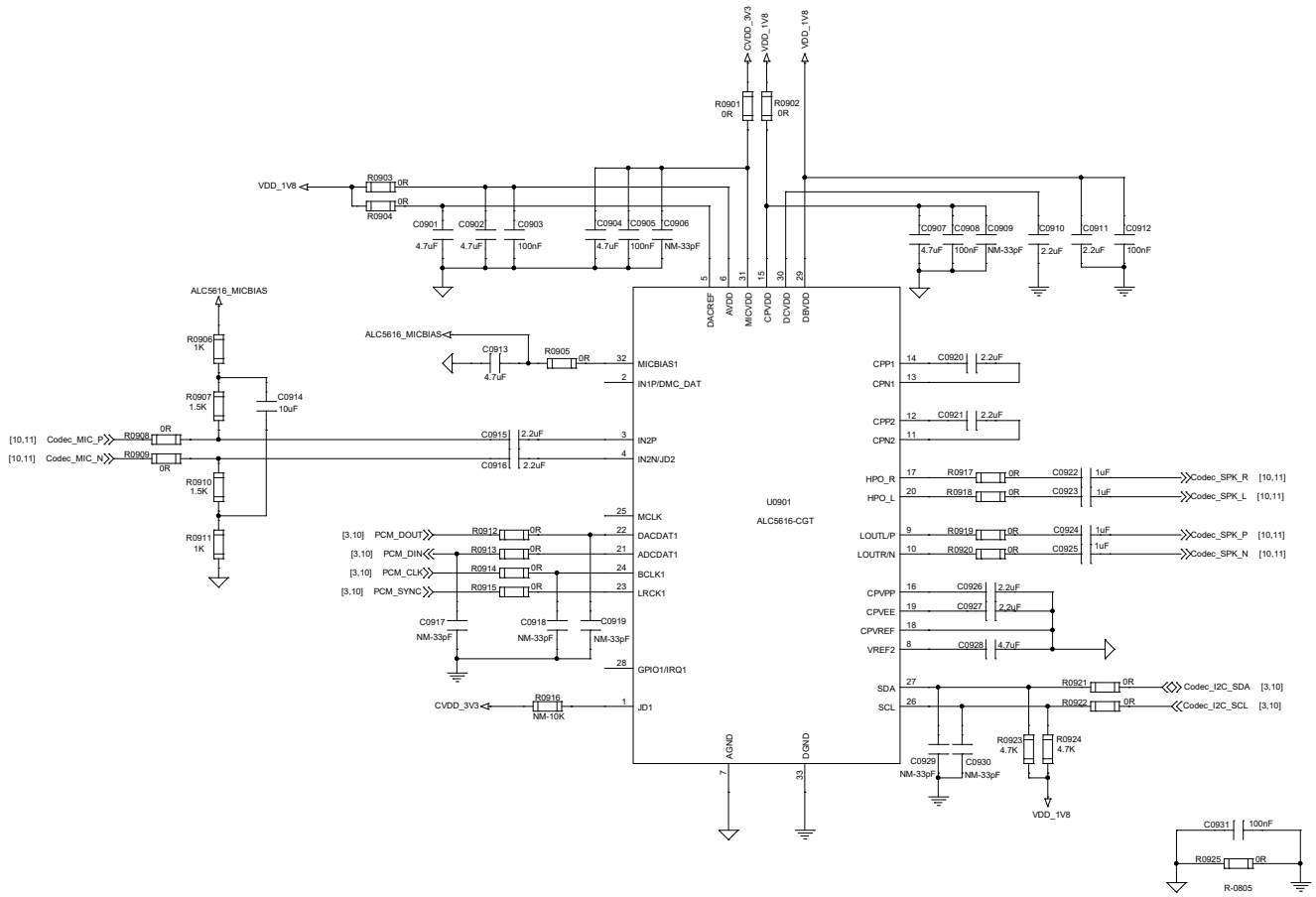
Audio Codec Design (ALC5616)



NOTE:

1. ALC5616 power-up sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD → MICVDD → software initialization.
2. ALC5616 power-down sequence: disable codec function by software → MICVDD → DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.
3. The module will automatically initialize the codec via I2C interface after it is turned on successfully, so all power supplies for the codec need to be powered up before that.
4. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805. For more details, see the sheet of "Audio Codec Interface Design".
5. For more details, see the datasheet of ALC5616.

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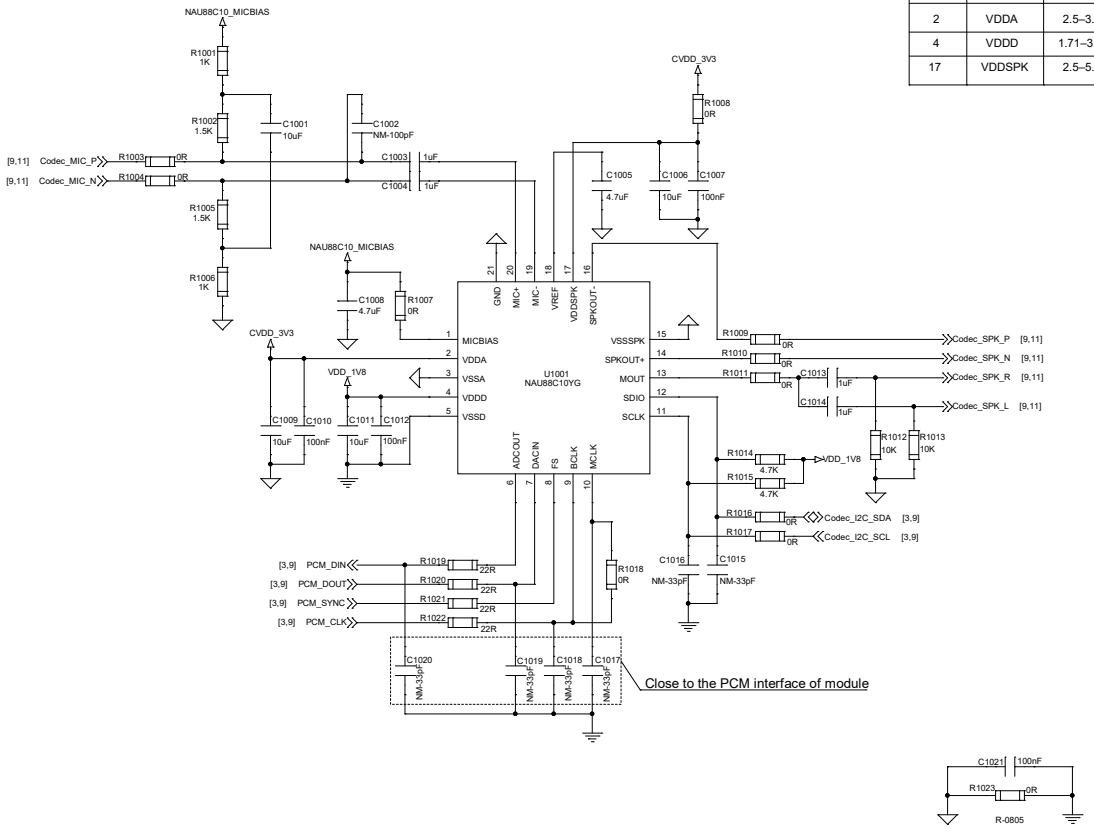
Audio Codec Design (NAU88C10YG)

Pin No.	Pin Name	Voltage	Description
2	VDDA	2.5–3.6 V	Analog VDD
4	VDDD	1.71–3.6 V	Digital VDD
17	VDDSPK	2.5–5.5 V	Loudspeaker power supply



NOTE:

1. The codec should be away from interference sources such as RF and power supplies, and the codec audio signal should be surrounded with ground as much as possible.
2. The voltage of VDDA pin must always be larger than that of VDDD.
3. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805. For more details, see the sheet of “Audio Codec Interface Design.
4. For more details, see the datasheet of NAU88C10YG.

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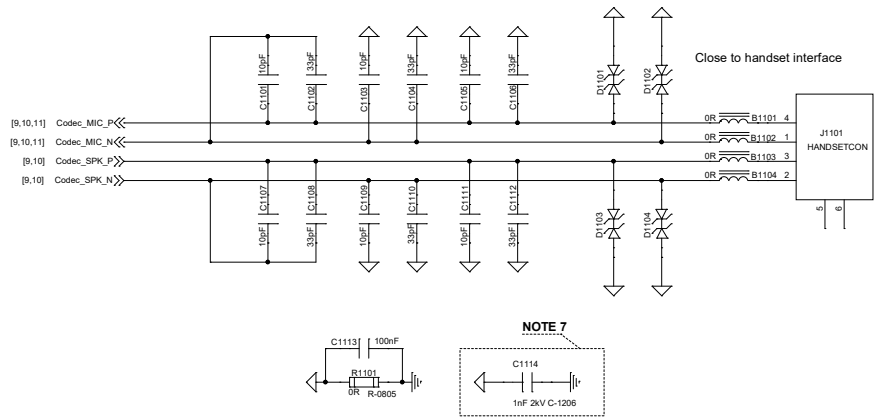
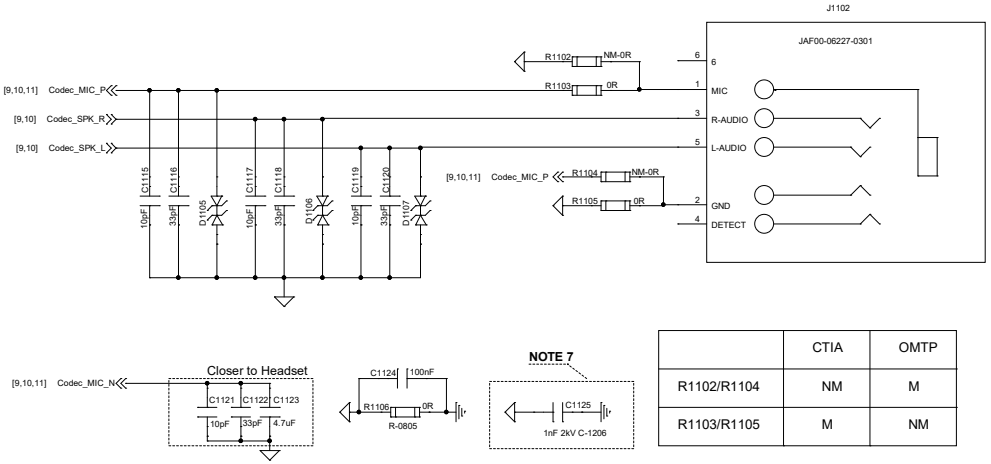
Audio Codec Interface Design

Handset Application



Headset Application

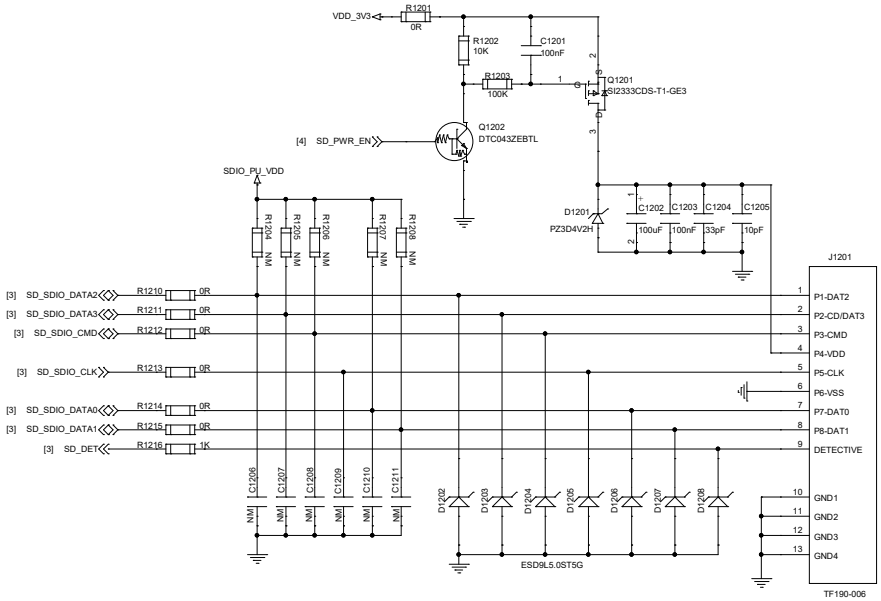


	CTIA	OMTP
R1102/R1104	NM	M
R1103/R1105	M	NM

NOTE:

1. The codec analog output can drive handset and headset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.
2. In handset application, both the MIC and SPK signal traces need to be routed as differential pairs.
3. In headset application, the MIC signal traces need to be routed as a differential pair.
4. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noises such as clock and DC-DC signals, etc.
5. Pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805 (a via directly to main GND).
6. You can choose either ALC5616 or NAG88C10YG in audio codec design.
7. C1114 and C1125 capacitors are used for ESD protection, they need to be placed close to D1101, D1102, D1103, D1104, D1105, D1106 and D1107 respectively, and connected to the main ground nearby.

SD Card Interface Design



NOTE:

1. The SDIO_PU_VDD can only be used for the pull-up resistor of SDIO bus and its maximum output current is 50 mA.
2. The supply voltage range of VDD for SD card is 2.7–3.6 V and a sufficient current up to 0.8 A should be provided.
3. To avoid the jitter of bus, pull-up resistors R1204–R1208 are recommended to be added to SDIO bus. SDIO_PU_VDD should be used as the pull-up power.
   The value of these resistors are among 10–100 kΩ and the recommended value is 100 kΩ.
4. In order to improve the signal quality, it is recommended to add 0 Ω resistors R1210–R1215 in series between the module and the SD card connector.
   The bypass capacitors C1206–C1211 are reserved and not mounted by default.
5. In order to offer good ESD protection, it is recommended to add electrostatic protective devices on SD card pins near the SD card connector with junction capacitance less than 15 pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc, as well as noisy signals such as clock and DC-DC signals, etc.
7. It is important to route the SDIO signal traces with ground surrounded. The impedance of SDIO data trace is 50 Ω (±10 %).
8. It is recommended to keep the traces of SD_SDIO_CLK, SD_SDIO_DATA[0:3] and SD_SDIO_CMD with equal length (the difference among them is less than 1 mm)
   and the total routing length needs to be less than 50 mm.
9. Make sure the adjacent trace spacing is twice the trace width and the bus capacitance is less than 15 pF.

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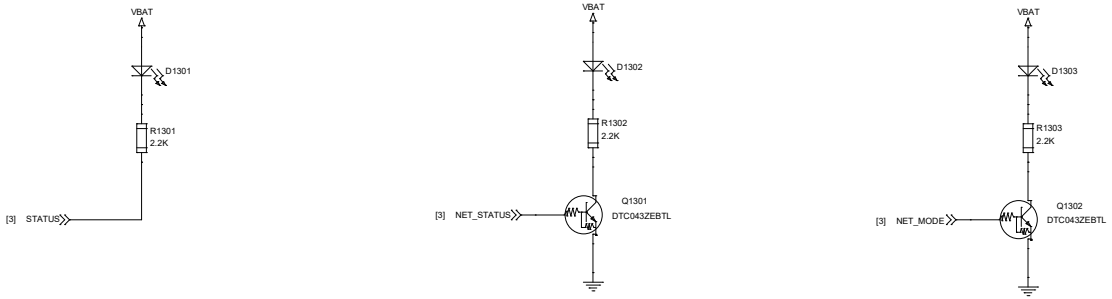
Other Designs

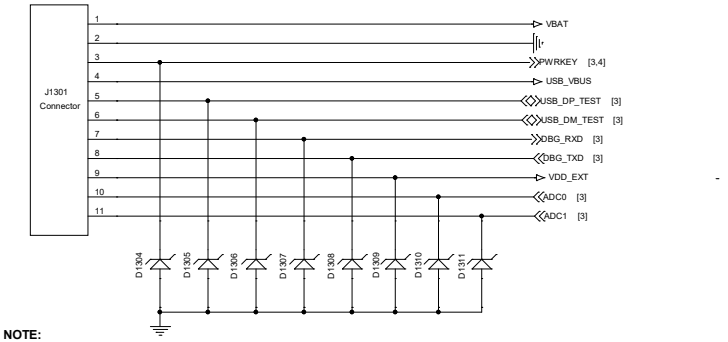
Indicators



NOTE:

1. The STATUS is an open drain output pin.
2. For more details about STATUS, NET_STATUS and NET_MODE, see the hardware design document of the module.
3. If the low current consumption is required when your device is in sleep status, replace the power supply VBAT of the STATUS, NET_STATUS and NET_MODE indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

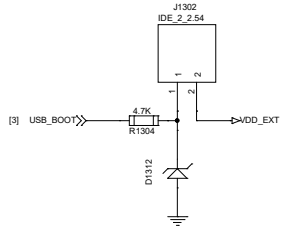
Reserved Test Points



NOTE:

1. Test points for both USB and debug UART interfaces are reserved for capturing logs.
2. Test points for USB interface can also be reserved for firmware upgrading.
3. The junction capacitance of the ESD protection components on USB data lines should be less than 2 pF.
4. The debug UART interface supports 1.8 V power domain, and a level-shifting circuit should be used if the power domain of your application is 3.3 V.

USB_BOOT Interface



NOTE:

1. It is recommended to reserve the USB_BOOT interface design.
2. USB_BOOT is kept open by default. Pull USB_BOOT up to VDD_EXT before the module starts up, thus the module will enter emergency download mode when powered up. In this mode, the module supports firmware upgrading over USB interface.

Quectel Wireless Solutions		
PROJECT: UC200A-GL		VER: 1.0
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DATE: Friday, March 03, 2023	SHEET: 13 OF 13	