UC200A-GL

Hardware Design

UMTS/HSPA+ Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-10-29	Anthony LIU/Ethan FANG	Creation of the document
1.0	2022-06-30	Bowen LIAO/Ethan FANG	First official release

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1 Introduction

This document defines UC200A-GL module and describes its air interface and hardware interface which are connected with your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SD_SDIO_DATA[0:3] refers to all four SD_SDIO_DATA pins, SD_SDIO_DATA0, SD_SDIO_DATA1, SD_SDIO_DATA2, and SD_SDIO_DATA3.

2 Product Overview

UC200A-GL is a WCDMA/GSM wireless communication module. Its general features are listed below：

- Supports HSDPA, HSUPA, HSPA+, WCDMA, EDGE and GPRS coverage.
- Provides audio support for your specific applications.
- SMT module; supports most M2M applications，like OTT, CPE, Router, data card, PAD, security and industrial-grade PDA.

Table 2: Brief Introduction of the Module

Categories	
Package and pins number	80 LCC pins; 64 LGA pins
Dimensions	(29.0 ±0.15) mm × (32.0 ±0.15) mm × (2.4 ±0.2) mm
Weight	approx. 4.4 g
Wireless network functions	WCDMA/GSM

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Type	UC200A-GL
WCDMA	B1/B2/B5/B8
GSM	GSM850/EGSM900/DCS1800/PCS1900

2.2. Key Features

Table 4: Key Features

Features	Details
Power Supply	● Supply voltage: 3.4–4.5 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interface	Supports (U)SIM card: 1.8/3.0 V
Audio Features	● Supports one digital audio interface: PCM interface ● GSM: HR/FR/EFR/AMR/AMR-WB ● WCDMA: AMR/AMR-WB ● Supports echo cancellation and noise suppression
PCM Interface	● Used for audio function with external Codec ● Supports 16-bit linear data format ● Supports short frame synchronization ● Supports master and slave* modes
I2C Interface	● Supports one digital I2C interface ● Complies with I2C bus protocol specifications (100 kHz/400 kHz) ● Multi-master mode is not supported
USB Interface	● Compliant with USB 2.0 specification (slave only), with transmission rates up to 480 Mbps ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial driver for Windows 7/8/8.1/10/11, Linux 2.6–5.15 and Android 4.x–12.x systems
SDIO Interface	Supports SD 3.0 protocol
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default, Max. 921600 bps ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for log output ● Baud rate: 115200 bps
Network Indication	● NET_MODE indicates network registration status ● NET_STATUS indicates network operation status
AT Commands	Compliant with *3GPP TS 27.007*, *3GPP TS 27.005* and Quectel

	enhanced AT commands
Antenna Interface	● Main antenna interface (ANT_MAIN) ● 50 Ω impedance
Transmitting Power	● GSM850: Class 4 (33 dBm ±2 dB) ● EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800: Class 1 (30 dBm ±2 dB) ● PCS1900: Class 1 (30 dBm ±2 dB) ● GSM850 8-PSK: Class E2 (27 dBm ±3 dB) ● EGSM900 8-PSK: Class E2 (27 dBm ±3 dB) ● DCS1800 8-PSK: Class E2 (26 dBm ±3 dB) ● PCS1900 8-PSK: Class E2 (26 dBm ±3 dB) ● WCDMA: Class 3 (24 dBm +1/-3 dB)
UMTS Features	● Supports 3GPP Rel-7 HSPA+, HSDPA, HSUPA and WCDMA ● Supports QPSK, 16QAM and 64QAM modulation ● HSPA+: Max. 21 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL)/384 kbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1–4 ● Max. 85.6 kbps (DL)/85.6 kbps (UL) **EDGE:** ● Supports EDGE multi-slot class 12 ● Supports GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 236.8 kbps (DL)/236.8 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS /FTPS/SSL/FILE/MQTT/MMS/SMTP/SMTPS protocols ● Supports PAP and CHAP for PPP connections
Temperature Range	● Operating temperature range [1]: -35 °C to +75 °C ● Extended temperature range [2]: -40 °C to +85 °C ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	Use USB interface or DFOTA to upgrade
RoHS	All hardware components are fully compliant with EU RoHS directive

[1] Within the operating temperature range, the module meets 3GPP specifications.
[2] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- DDR + NAND flash
- Radio frequency
- Peripheral interface

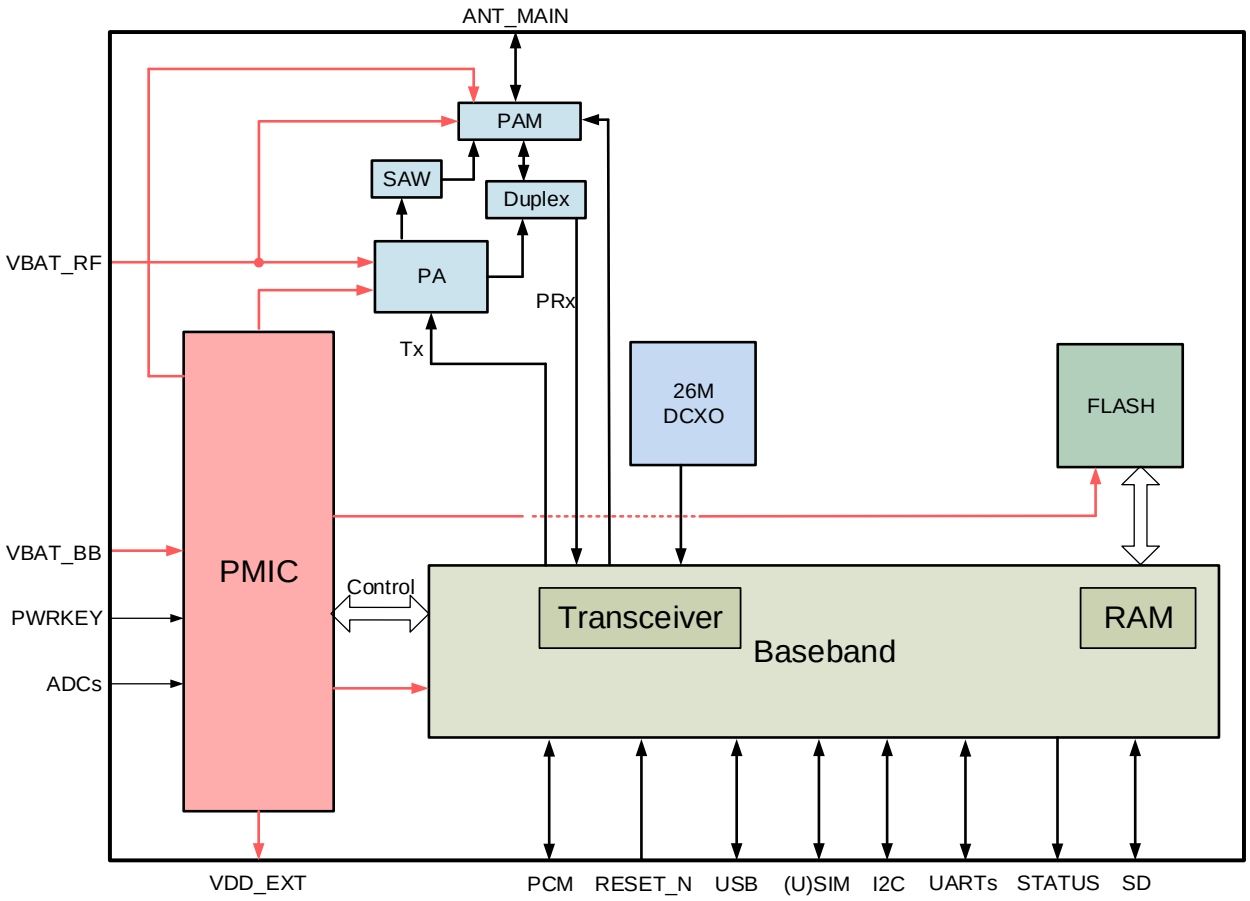


Figure 1: Functional Diagram

2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

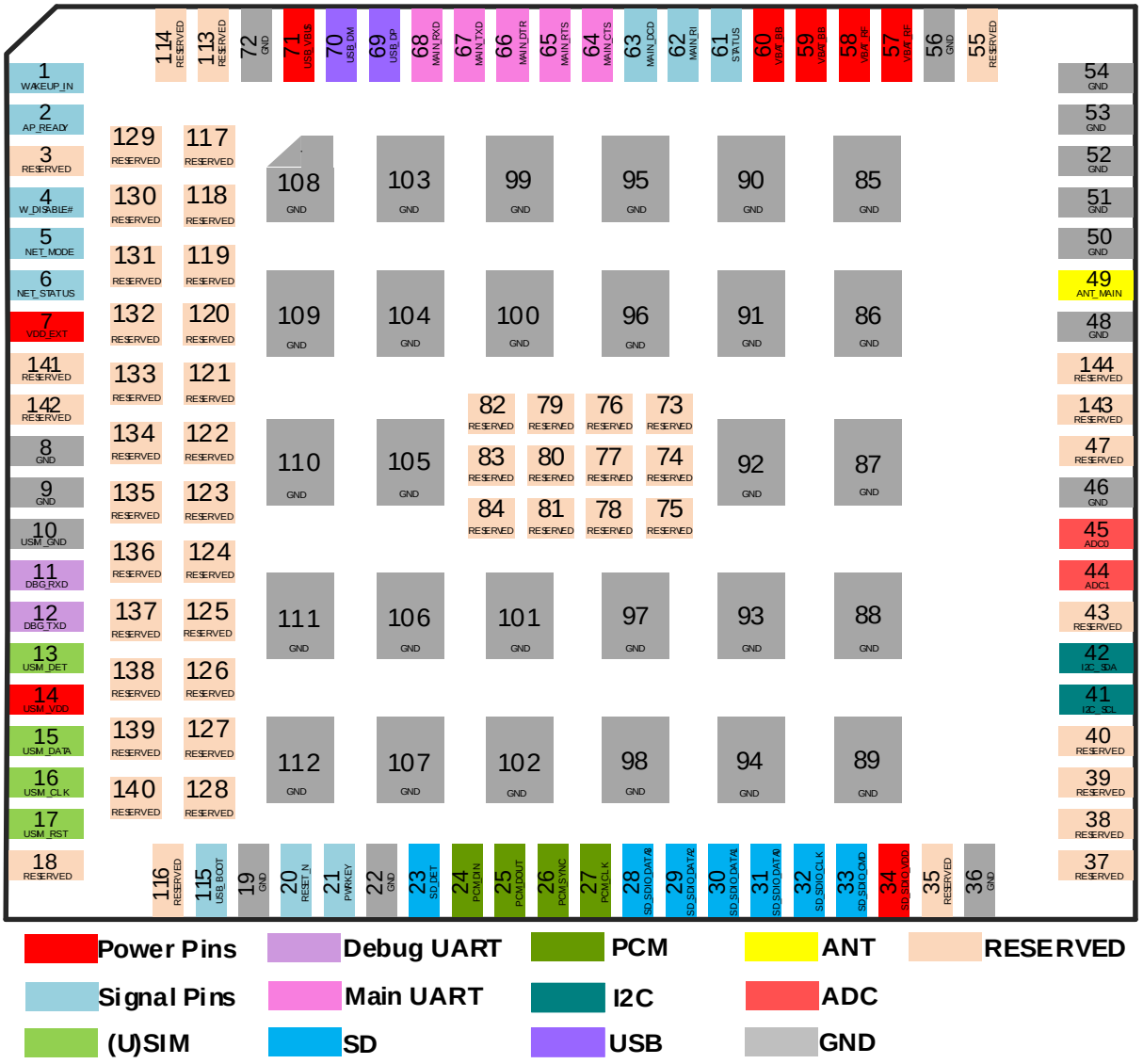


Figure 2: Pin Assignment (Top View)

NOTE

1. USB_BOOT cannot be pulled up before startup.
2. Other unused and RESERVED pins are kept open, and all GND pins are connected to the ground network.

2.5. Pin Description

The following table shows the DC characteristics and pin descriptions.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for the module's baseband part	Vmax = 4.5 V Vmin = 3.4 V Vnom = 3.8 V	It should at least be provided with a sufficient current of 0.8 A.
VBAT_RF	57, 58	PI	Power supply for the module's RF part		It should at least be provided with a sufficient current of 2.0 A.
VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	It can provide a pull-up power supply to the external GPIO. If unused, keep it open.

Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module	V_{IL}max = 0.5 V	VBAT power domain. Active low.
RESET_N	20	DI	Reset the module		1.8 V power domain. Active low after module startup.
Indication Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_MODE	5	DO	Indicate the module's network registration mode	1.8 V	If unused, keep them open.
NET_STATUS	6	DO	Indicate the module's network activity status		
STATUS	61	OD	Indicate the module's operation status		External pull-up is required. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	Typical value is 5.0 V. If unused, keep it open.
USB_DP	69	AIO	USB differential data (+)		90 Ω differential impedance. USB 2.0 compliant. If unused, keep them open.
USB_DM	70	AIO	USB differential data (-)		
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		Specified ground for (U)SIM card		It is connected to (U)SIM card connector.

USIM_VDD	14	PO	(U)SIM card power supply	1.8/3.0 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM_DATA	15	DIO	(U)SIM card data		
USIM_CLK	16	DO	(U)SIM card clock		
USIM_RST	17	DO	(U)SIM card reset		
USIM_DET	13	DI	(U)SIM card hot-plug detect	1.8 V	If unused, keep it open.
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_SDIO_CLK	32	DO	SD card SDIO clock	1.8/2.8 V	If unused, keep them open.
SD_SDIO_CMD	33	DIO	SD card SDIO command		
SD_SDIO_DATA0	31	DIO	SD card SDIO data bit 0		
SD_SDIO_DATA1	30	DIO	SD card SDIO data bit 1		
SD_SDIO_DATA2	29	DIO	SD card SDIO data bit 2		
SD_SDIO_DATA3	28	DIO	SD card SDIO data bit 3		
SD_SDIO_VDD	34	PO	SD card SDIO power supply		
SD_DET*	23	DI	SD card detect	1.8 V	If unused, keep it open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RI	62	DO	Main UART ring indication	1.8 V	If unused, keep them open.
MAIN_DCD	63	DO	Main UART data carrier detect		
MAIN_CTS	64	DO	DTE clear to send signal from DCE		Connect to DTE's CTS. If unused, keep it open.
MAIN_RTS	65	DI	DTE request to send signal to DCE		Connect to DTE's RTS.

					If unused, keep it open.
MAIN_DTR	66	DI	Main UART data terminal ready		If unused, keep them open.
MAIN_RXD	68	DI	Main UART receive		
MAIN_TXD	67	DO	Main UART transmit		
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	11	DI	Debug UART receive	1.8 V	If unused, keep them open.
DBG_TXD	12	DO	Debug UART transmit		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock		Used for external Codec. An external 1.8 V pull-up resistor is needed. If unused, keep them open.
I2C_SDA	42	OD	I2C serial data		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	26	DIO	PCM data frame sync	1.8 V	In master mode, it is in output state. In slave mode*, it is in input state. If unused, keep them open.
PCM_CLK	27	DIO	PCM clock		
PCM_DIN	24	DI	PCM data input		If unused, keep them open.
PCM_DOUT	25	DO	PCM data output		
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	49	AIO	Main antenna interface		50 Ω impedance.

ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	45	AI	General-purpose ADC interface	Voltage Range: 0 V–VBAT_BB	If unused, keep them open.
ADC1	44	AI			
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Forces the module to enter emergency download mode	1.8 V	Active High. It is recommended to reserve test points.
WAKEUP_IN*	1	DI	Wake up the module		If unused, keep them open.
AP_READY	2	DI	Application processor ready		
W_DISABLE#	4	DI	Airplane mode control		Pull-up by default. Active low. (Driving it low can make the module enter airplane mode.) If unused, keep it open.
GND					
Pin Name	**Pin No.**				
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112				
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	3, 18, 35, 37–40, 43, 47, 55, 73–84,113, 114, 116–144				Keep them open.

2.6. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (UMTS & LTE EVB) with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

The table below outlines operating modes of the module.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module is registered on the network and ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transmission rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, power consumption of the module will be reduced to the minimal level. The module can still receive paging, SMS, voice call and TCP/UDP data from network.	
Power Down Mode	In this mode, the VBAT power supply is constantly turned on and the software stops working.	

NOTE

More information about the AT command, see ***document [2]***.

3.2. Sleep Mode

In sleep mode, the module can reduce power consumption to a very low level, the following section describes power saving procedures of the module.

3.2.1. UART Application

If the host communicates with module via UART interface, the following preconditions should be met to enable the module to enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR to a high level.
- Ensure USB_VBUS is held at a low level or keep it open.

The following figure shows the connection between the module and the host.

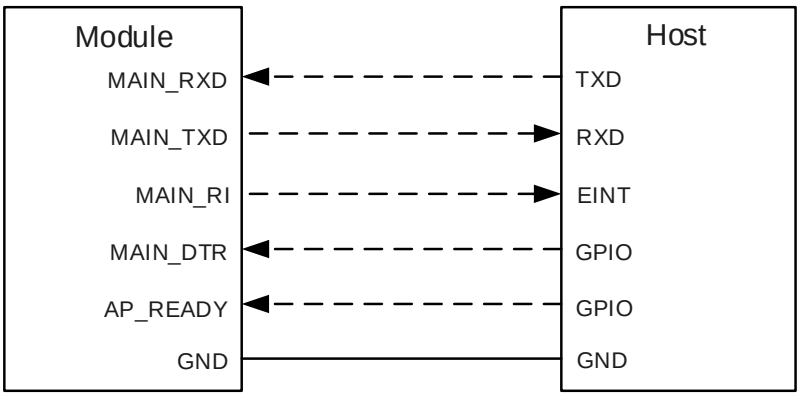


Figure 3: Sleep Mode Application via UART

- Driving MAIN_DTR low by host will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. Please refer to ***Chapter 4.8.3*** for details about MAIN_RI behavior.

3.2.2. USB Application with USB Remote Wakeup Function

If the host supports USB Suspend/Resume and remote wakeup functions, the following three preconditions must be met to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is kept at high level or kept open.

- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

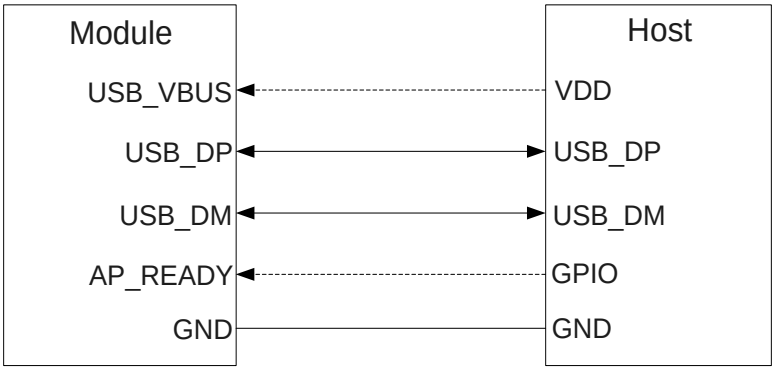


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wakeup signals via USB bus to wake up the host.

3.2.3. USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host. There are three preconditions to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or kept open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

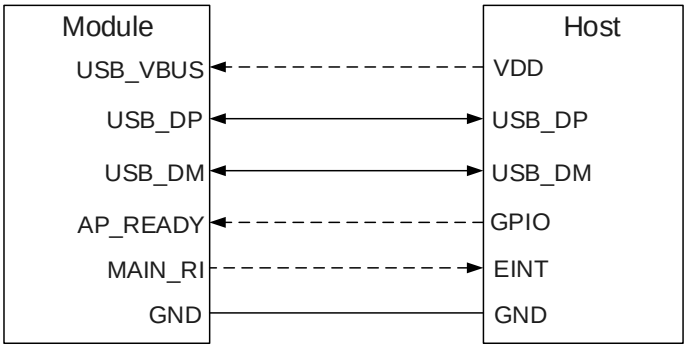


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. Please refer to ***Chapter 4.8.3*** for details about MAIN_RI behavior.

3.2.4. USB Application without USB Suspend Function

If the host does not support USB Suspend function, please disconnect USB_VBUS with additional control circuit to let the module enter into sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or kept open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

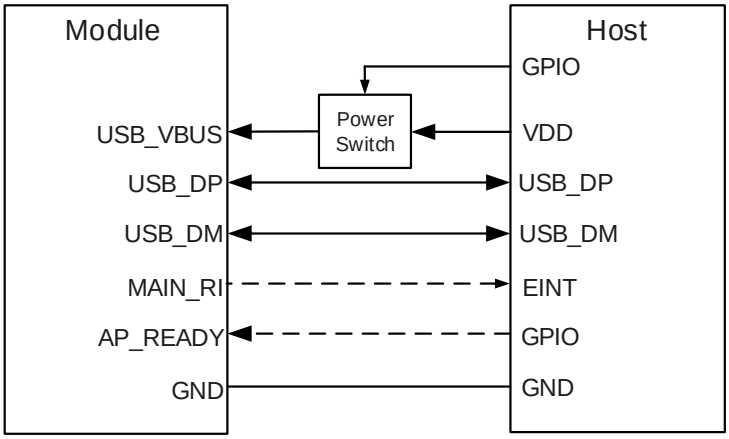


Figure 6: Sleep Mode Application without Suspend Function

Turn on the power switch and supply power to USB_VBUS will wake up the module.

NOTE

1. Please pay attention to the level match shown in dotted line between the module and the host in all figures illustrated in ***Chapter 3.2***.
2. The AP_READY shown in all figures in ***Chapter 3.2***, is set to high level by default and active low.

3.3. Airplane Mode

When the module enters into airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default, and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving the pin low can make the module enter airplane mode.

Software:

AT+CFUN=<fun> provides choices of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode (Both (U)SIM and RF functions are disabled.).
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode (RF function is disabled.).

3.4. Power Supply

3.4.1. Power Supply pins

The module provides four VBAT pins dedicated to the connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows the details of power supply and GND pins.

Table 8: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	59, 60	PI	Power supply for the module's baseband part	It should at least be provided with a sufficient current of 0.8 A.
VBAT_RF	57, 58	PI	Power supply for the module's RF part	It should at least be provided with a sufficient current of 2.0 A.

VDD_EXT	7	PO	Provide 1.8 V for external circuit	It can provide a pull-up power supply to the external GPIO. If unused, keep it open.

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide a sufficient current of 2.8 A at least. If the voltage drops between input and output is not too high, it is suggested that an LDO should be used. If there is a big voltage difference between input and the desired output VBAT, a buck converter is preferred as the power supply.

The following figure shows a reference design for +5 V input power source. The design uses the LDO MIC29302WU from Micrel company. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

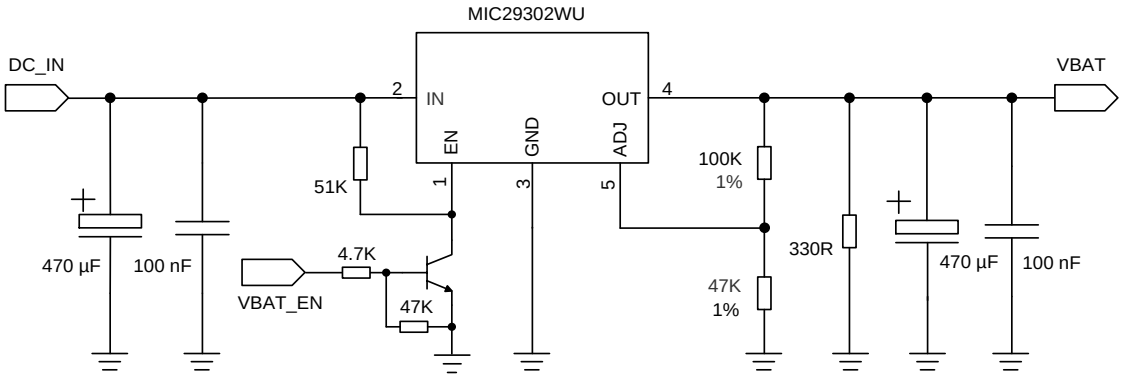


Figure 7: Reference Design of Power Supply

NOTE

It is recommended to design switch control for power supply.

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.4 V to 4.5 V. Please make sure the input voltage will never drop below 3.4 V.

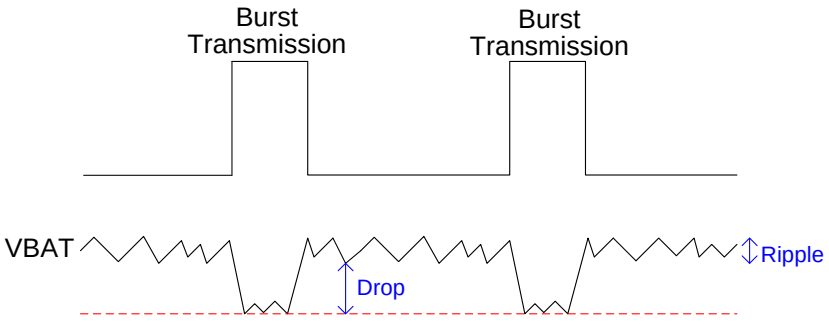


Figure 8: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 µF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star configuration. The width of VBAT_BB trace should be no less than 1 mm; and the width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, to ensure the stability of power source, it is suggested that a TVS diode of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. The following figure shows the star configuration of the power supply.

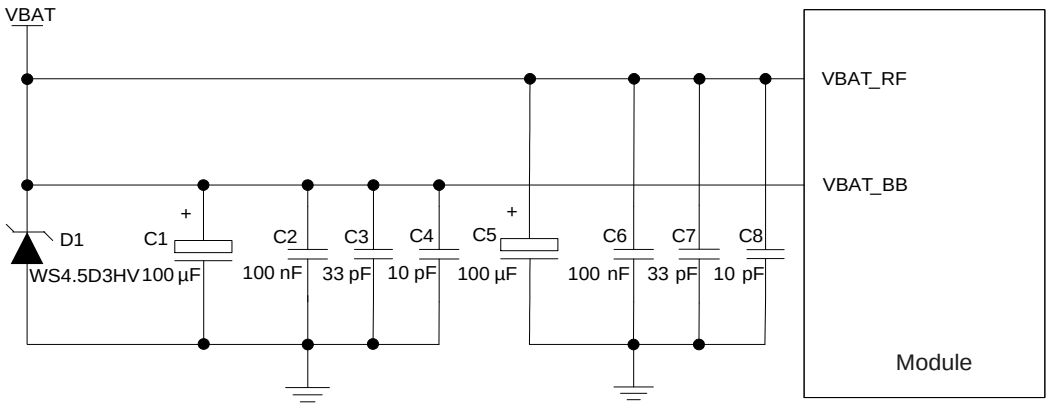


Figure 9: Star Structure of the Power Supply

3.5. Turn On

3.5.1. Turn on the Module with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	VBAT power domain. Active low.

When the module is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

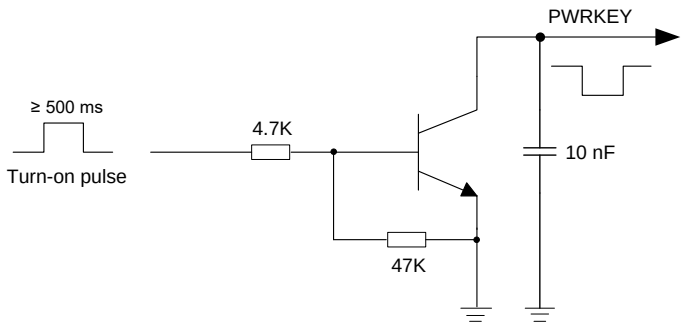


Figure 10: Turning on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

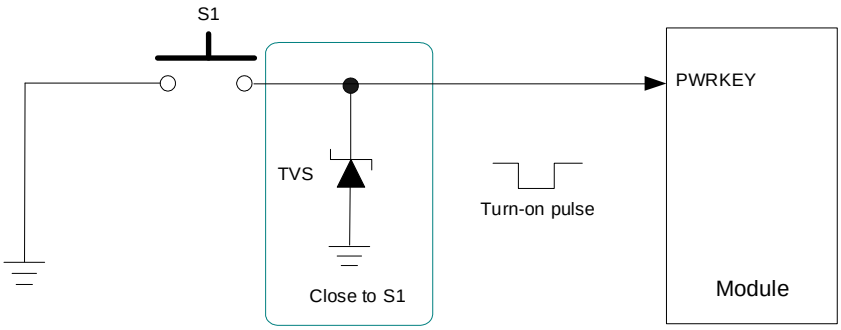


Figure 11: Turning on the Module with a Button

The power up scenario is illustrated in the following figure.

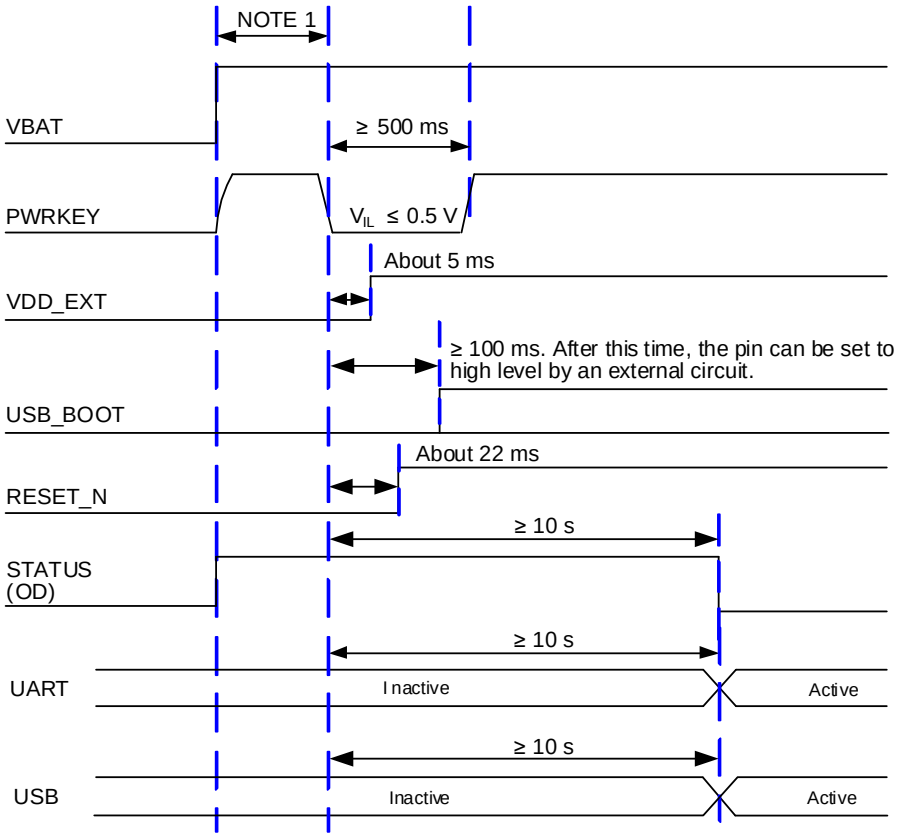


Figure 12: Power-up Timing

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 4.7 kΩ resistor if module needs to be powered on automatically and shutdown is not needed.

3.6. Turn Off

3.6.1. Turn off the Module with PWRKEY

Driving the PWRKEY low for at least 650 ms, then the module will execute power-down procedure after the PWRKEY is released. The timing of turning off the module is illustrated in the following figure.

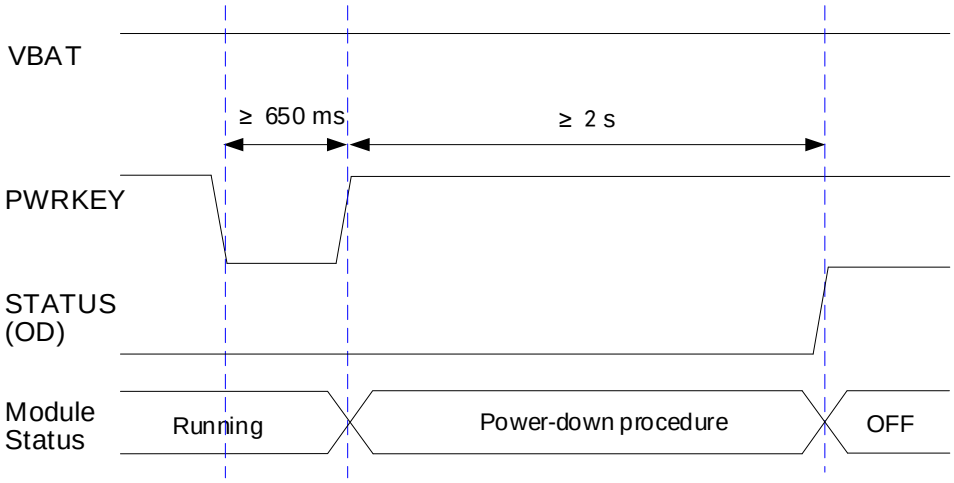


Figure 13: Timing of Turning off Module

3.6.2. Turn off the Module with AT Command

It is safe to use **AT+QPOWD** to turn off the module, which is equal to turn off the module via PWRKEY Pin. See ***document [2]*** for details about **AT+QPOWD**.

NOTE

1. To avoid damaging internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off module with the AT command, please keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on again after successfully turn-off.

3.7. Reset

The module can be reset by driving the RESET_N low for at least 300 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Definition of RESET

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	1.8 V power domain. Active low after module startup.

The recommended circuit is equal to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

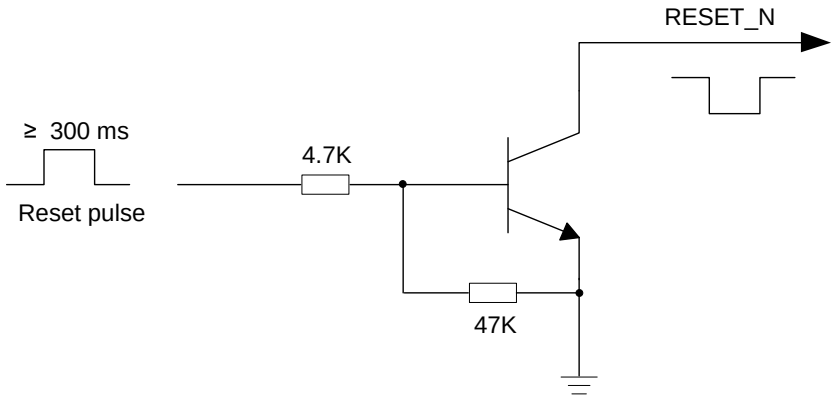


Figure 14: Reference Circuit of RESET_N with Driving Circuit

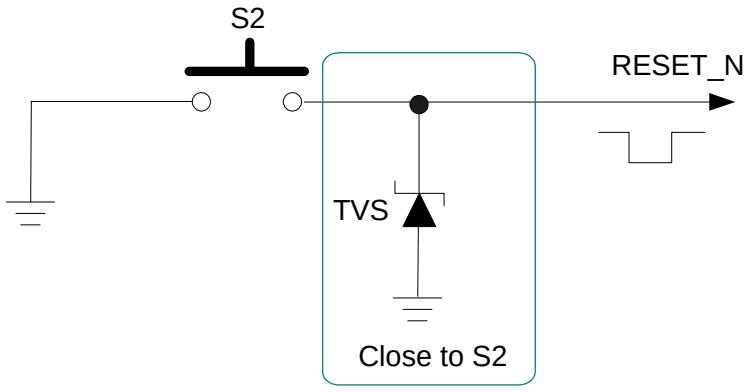


Figure 15: Reference Circuit of RESET_N with Button

The timing of resetting module is illustrated in the following figure.

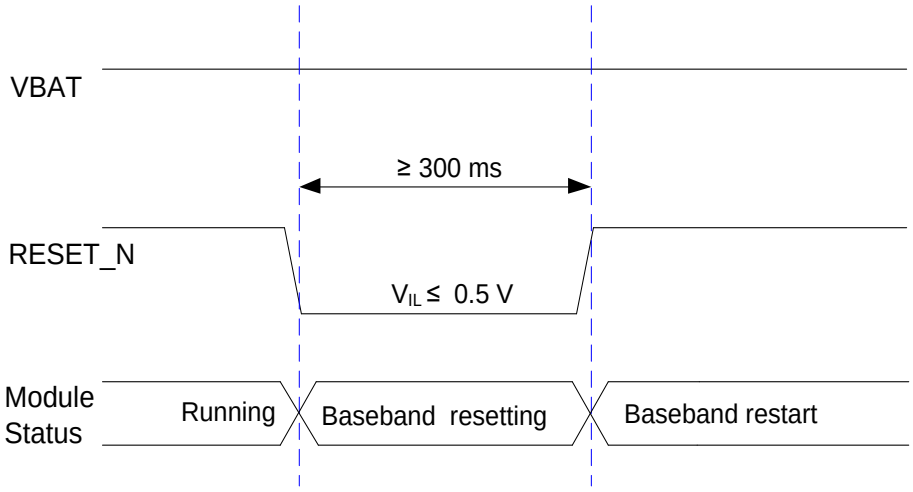


Figure 16: Timing of Resetting Module

NOTE

1. Please ensure that there is no large capacitance with the maximum value exceeding 10 nF on PWRKEY and RESET_N pins.
2. RESET_N only resets the internal baseband chip of the module and does not reset the power management chip.

4 Application Interfaces

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve as a slave device and is used for AT command communication, data transmission, software debugging and firmware upgrade.

Pin definition of the USB interface is here as follows:

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	71	AI	USB connection detect	Typical value is 5.0 V. If unused, keep it open.
USB_DP	69	AIO	USB differential data (+)	90 Ω differential impedance. USB 2.0 compliant. If unused, keep them open.
USB_DM	70	AIO	USB differential data (-)	

It is recommended to reserve test points for debugging and firmware upgrade in your designs. The following figure shows a reference circuit of USB interface.

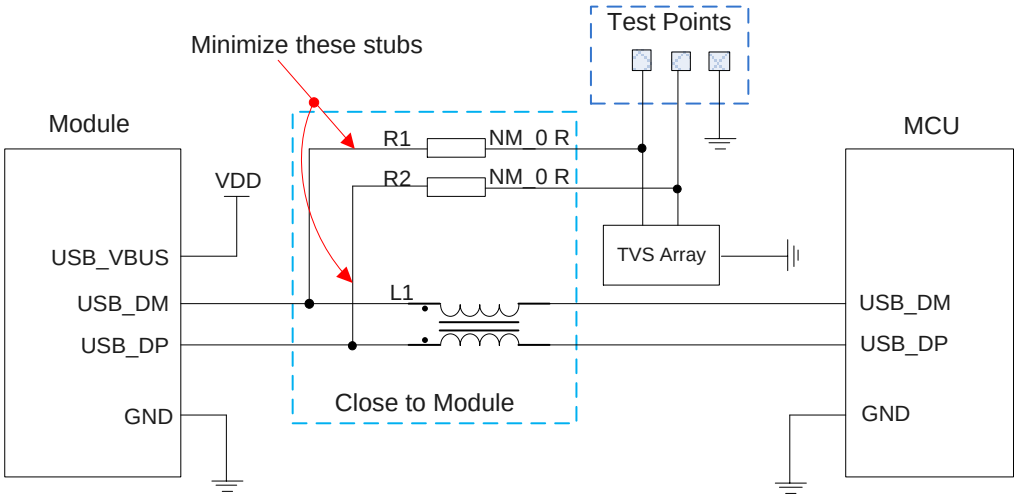


Figure 17: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure the integrity of USB data line signal, L1, R1 and R2 components must be placed close to the module, and R1 and R2 should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when designing the USB interface to meet USB specifications.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices, high speed signal traces and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Junction capacitance of the ESD protection device might cause influences on USB data lines, so please pay attention to the selection of the device. Typically, the stray capacitance should be less than 2 pF for USB.
- If possible, reserve a 0 Ω resistor on USB_DP and USB_DM lines respectively.

For more details about the USB specifications, please visit http://www.usb.org/home.

4.2. USB_BOOT Interface

The module provides a USB_BOOT pin. You can pull USB_BOOT up to VDD_EXT before turning on the module, thus the module will enter emergency download mode when turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 12: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Forces the module to enter download mode	1.8 V power domain. Active High. It is recommended to reserve test points.

The following figure shows a reference circuit of USB_BOOT interface.

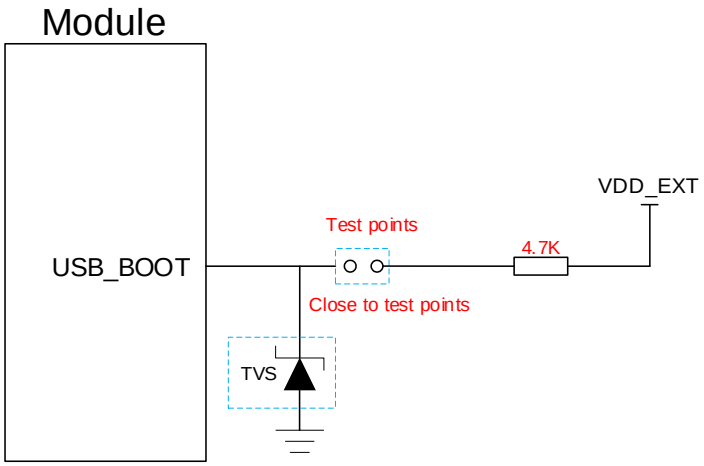


Figure 18: Reference Circuit of USB_BOOT Interface

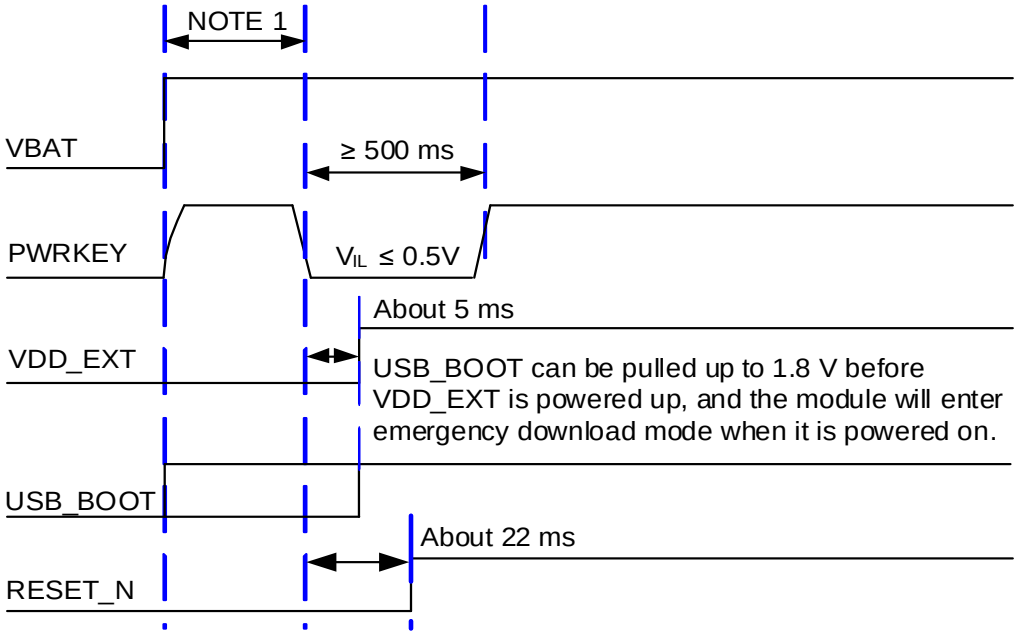


Figure 19: Timing Sequence for Entering Emergency Download Mode

NOTE

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. When using MCU to control module to enter the emergency download mode, please follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Directly connect the test points as shown in ***Figure 18*** can manually force the module into download mode.
3. USB_BOOT cannot be pulled up to a high level before startup.

4.3. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 13: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_GND	10		Specified ground for (U)SIM card	It is connected to (U)SIM card connector.

USIM_VDD	14	PO	(U)SIM card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM_DATA	15	DIO	(U)SIM card data	
USIM_CLK	16	DO	(U)SIM card clock	
USIM_RST	17	DO	(U)SIM card reset	
USIM_DET	13	DI	(U)SIM card hot-plug detect	1.8 V power domain. If unused, keep it open.

The module supports (U)SIM card hot-plug via the USIM_DET pin, the function supports low-level and high-level detections. It is disabled by default, and can be configured via **AT+QSIMDET**. See ***document [2]*** for details about the command.

The reference circuit of the 8-pin (U)SIM interface is as follows.

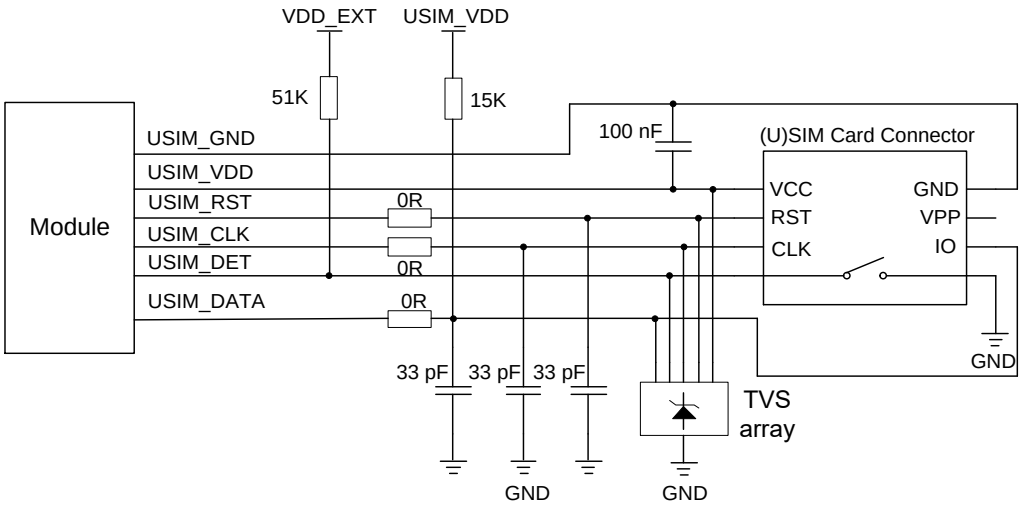


Figure 20: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

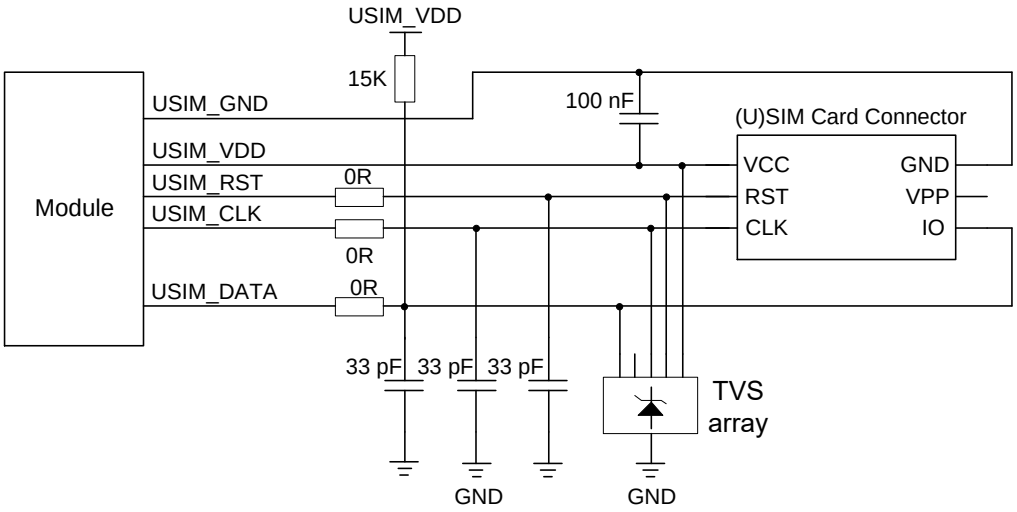


Figure 21: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Keep (U)SIM card connector as close as possible to the module. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signal traces away from RF and VCC traces.
- The maximum value of bypass capacitor of USIM_VDD does not exceed 1 μF.
- Ensure the ground between the module and the (U)SIM card connector is short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground surrounded.
- To offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors on the USIM_DATA, USIM_CLK and USIM_RST trances are used for filtering interference. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

4.4. PCM and I2C Interfaces

The module provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the primary mode (short frame synchronization) and the module works as both master and slave*.

The module supports one I2C interface which can only be used as primary devices in applications related to I2C interfaces, and multi-master mode is not supported.

Table 14: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	26	DIO	PCM data frame sync	1.8 V power domain. In master mode, it is in output state. In slave mode*, it is in input state. If unused, keep them open.
PCM_CLK	27	DIO	PCM clock	
PCM_DIN	24	DI	PCM data input	1.8 V power domain. If unused, keep them open.
PCM_DOUT	25	DO	PCM data output	

Table 15: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	41	OD	I2C serial clock	Used for external Codec. An external 1.8 V pull-up resistor is needed. If unused, keep them open.
I2C_SDA	42	OD	I2C serial data	

The module supports a 16-bit linear encoding format. The following figure shows the sequence diagram of short frame mode. (PCM_SYNC = 8 kHz, PCM_CLK = 2048 kHz).

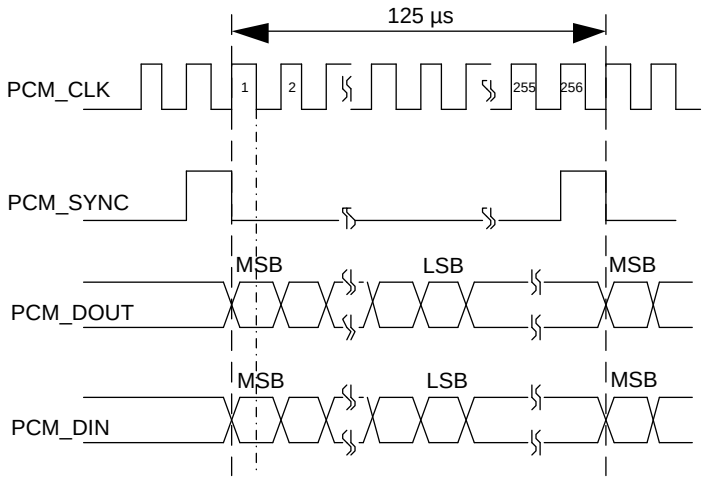


Figure 22: Timing Sequence for Short frame mode

In short frame mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz, 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4069 kHz PCM_CLK at 16 kHz PCM_SYNC.

Clock and mode can be configured by AT command, and the default configuration is short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [2]*** for details.

The following is a reference design for the PCM and I2C interfaces with external Codec chip

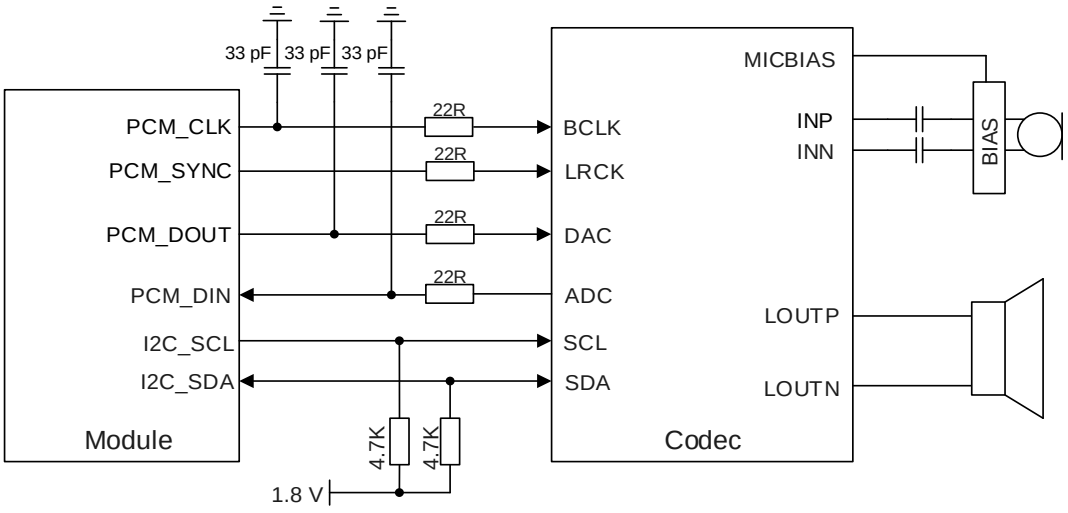


Figure 23: PCM and I2C Interface Circuit Reference Design

NOTE

It is recommended to reserve the RC (R = 22 Ω, C = 33 pF) circuit on the PCM signal trace and the capacitor should be placed close to the module, especially on PCM_CLK.

4.5. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps baud rates, and the baud rate is 115200 bps by default. This interface is used for data transmission and AT command communication. Also, it supports RTS and CTS hardware flow control.
- The debug UART interface supports 115200 bps baud rate. It is used for the output of partial logs.

Table 16: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	62	DO	Main UART ring indication	1.8 V power domain. If unused, keep them open.
MAIN_DCD	63	DO	Main UART data carrier detect	
MAIN_CTS	64	DO	DTE clear to send signal from DCE	1.8 V power domain. Connect to DTE's CTS. If unused, keep it open.
MAIN_RTS	65	DI	DTE request to send signal to DCE	1.8 V power domain. Connect to DTE's RTS. If unused, keep it open.
MAIN_DTR	66	DI	Main UART data terminal ready	1.8 V power domain. If unused, keep them open.
MAIN_RXD	68	DI	Main UART receive	
MAIN_TXD	67	DO	Main UART transmit	

Table 17: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	11	DI	Debug UART receive	1.8 V power domain.

DBG_TXD	12	DO	Debug UART transmit	If unused, keep them open.

The module provides a 1.8 V UART interface. A level translator should be used if the application is equipped with a 3.3 V UART interface. A level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

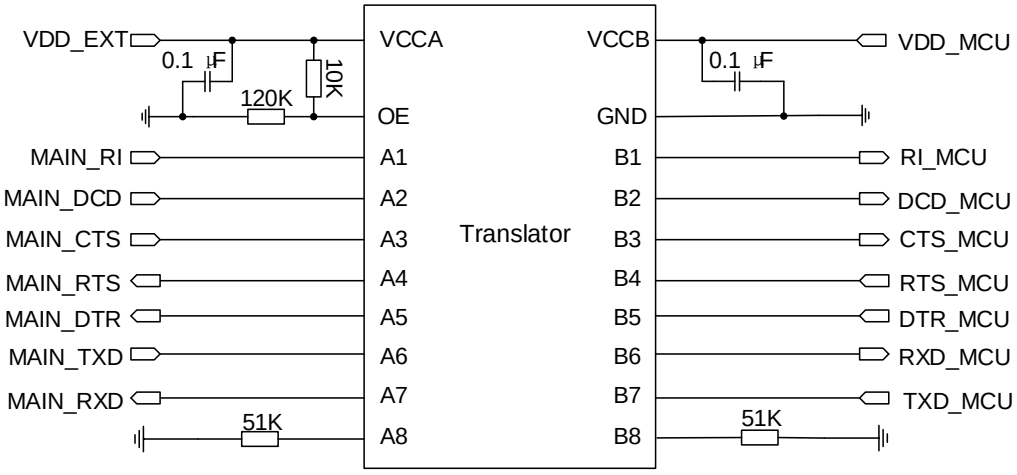


Figure 24: Reference Circuit with Level-shifting Chip

Please visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, please refer to that shown in solid lines, but pay attention to the direction of connection.

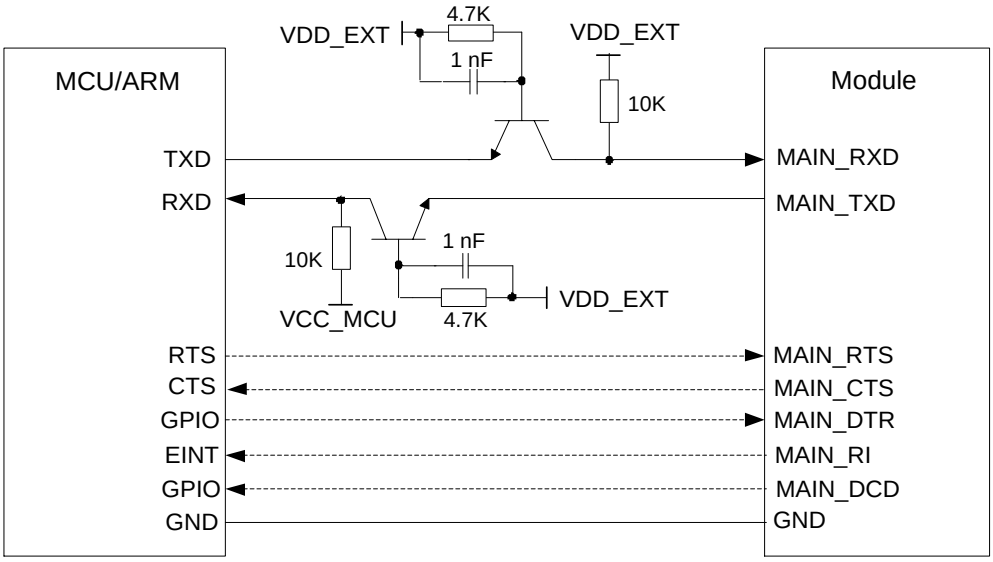


Figure 25: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS. Please pay attention to the I/O direction.

4.6. SD Card Interface

The module provides one SD card interface which supports SD 3.0 protocol.

Table 18: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_SDIO_CLK	32	DO	SD card SDIO clock	1.8/2.8 V power domain. If unused, keep them open.
SD_SDIO_CMD	33	DIO	SD card SDIO command	
SD_SDIO_DATA0	31	DIO	SD card SDIO data bit 0	
SD_SDIO_DATA1	30	DIO	SD card SDIO data bit 1	
SD_SDIO_DATA2	29	DIO	SD card SDIO data bit 2	
SD_SDIO_DATA3	28	DIO	SD card SDIO data bit 3	
SD_SDIO_VDD	34	PO	SD card SDIO power supply	
SD_DET*	23	DI	SD card hot-plug detect	1.8 V power domain. If unused, keep it open.

The following figure illustrates a reference design of SD card interface with the module.

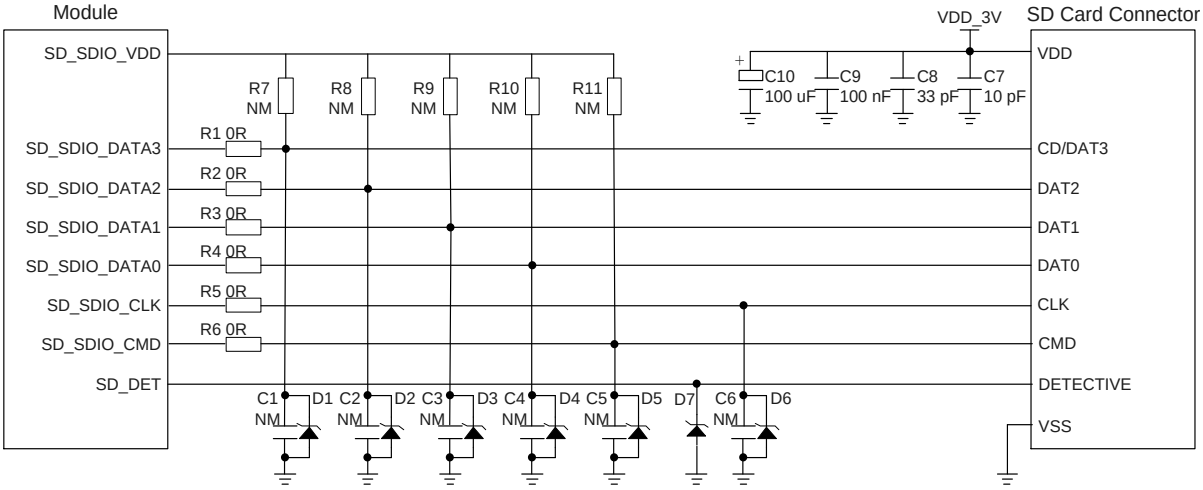


Figure 26: Reference Circuit of SD Card Interface

In SD card interface design, to ensure good communication performance with SD card, the following design principles should be complied with:

- The voltage range of SD card power supply VDD_3V is 2.7–3.6 V and a sufficient current up to 800 mA should be provided. The maximum output current of SD_SDIO_VDD is 50 mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, R7–R11 are needed to pull up the SDIO to SD_SDIO_VDD. The value of these resistors is among 10 kΩ to 100 kΩ and the recommended value is 100 kΩ. SD_SDIO_VDD should be used as the pull-up power supply.
- To improve signal quality, it is recommended to add 0 Ω resistors R1–R6 in series between the module and the SD card. The bypass capacitors C1–C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- To offer good ESD protection, it is recommended to add a TVS diode on SD card pins near the SD card connector with junction capacitance less than 15 pF.
- It is important to route the SDIO signal traces with ground surrounded. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals.
- It is recommended to keep the traces of SD_SDIO_CLK, SD_SDIO_DATA [0:3] and SD_SDIO_CMD with equal length (the difference among them is less than 1 mm) and the total routing length needs to be less than 50 mm.
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 15 pF.

4.7. ADC Interfaces

The module provides two Analog-to-Digital Converter (ADC) interfaces. To improve the accuracy of ADC, the trace of ADC interfaces should be surrounded by ground.

Table 19: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	45	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	44	AI		

The voltage value on ADC pins can be read via **AT+QADC=<port>**:

- **AT+QADC=0:** Read the voltage value on ADC0.
- **AT+QADC=1:** Read the voltage value on ADC1.

For more details about the AT command, see ***document [2]***.

The resolution of the ADC is up to 12 bits. The following table describes the characteristic of the ADC interface.

Table 20: Characteristics of ADC Interfaces

Name	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	VBAT_BB	V
ADC1 Voltage Range	0	-	VBAT_BB	V
ADC Resolution	-	12	-	bits

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application and the divider resistance should not exceed 100 kΩ.

4.8. Indication Signal

The pin definition of indication signal is as follows:

Table 21: Pin Definition of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network registration mode	1.8 V power domain. If unused, keep them open.
NET_STATUS	6	DO	Indicate the module's network activity status	
STATUS	61	OD	Indicate the module's operation status	External pull-up is required. If unused, keep it open.
MAIN_RI	62	DO	Main UART ring indication	1.8 V power domain. If unused, keep it open.

4.8.1. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two network indication pins: NET_MODE and NET_STATUS.

Table 22: Working State of the Network Connection Status/Activity Indication

Pin Name	Status	Description
NET_MODE	Always High	Registered on UMTS network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transmission is ongoing
	Always High	Voice calling

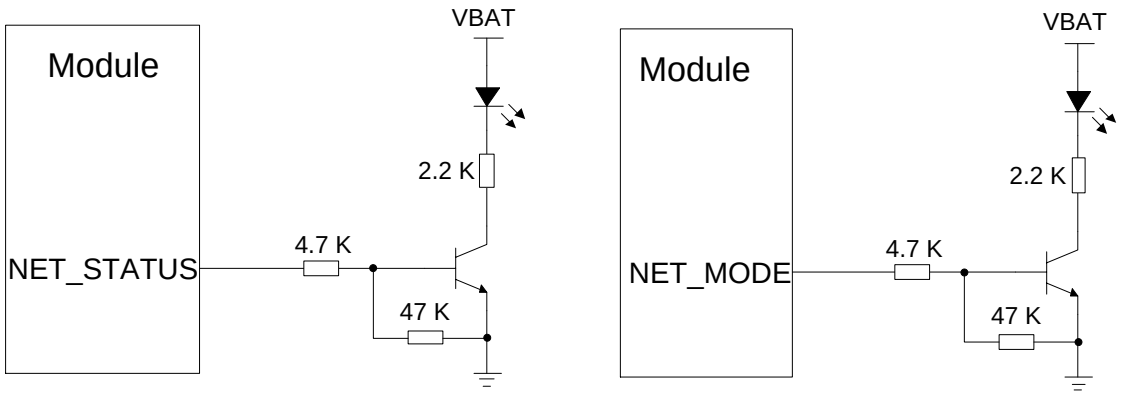


Figure 27: Reference Circuit of the Network Status Indication

4.8.2. STATUS

The STATUS pin is an open drain output for module's operation status indication. It can be connected to a GPIO of DTE with a pulled-up resistor, or as an LED indication circuit as below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

The following figure shows different circuit designs of STATUS, and you can choose either one according to the application demands.

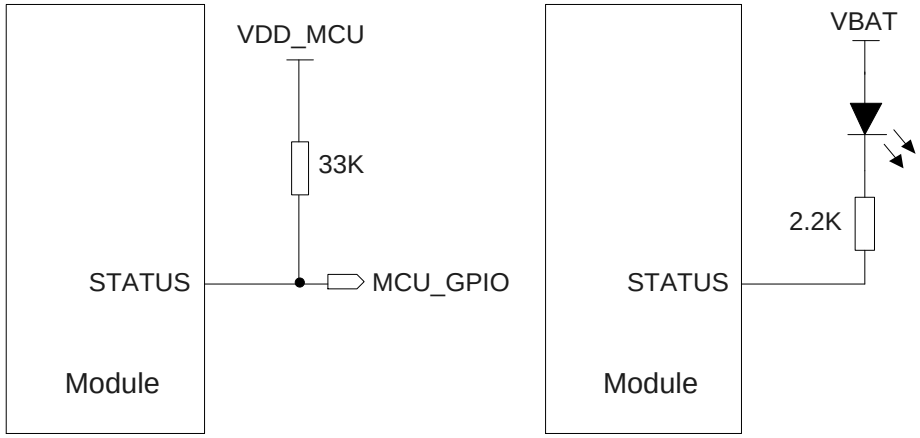


Figure 28: Reference Circuits of STATUS

NOTE

The status pin cannot be used as indication of module shutdown status when VBAT is removed.

4.8.3. MAIN_RI

AT+QCFG="risignaltype","physical" can be used to configure MAIN_RI behaviors. No matter on which port a URC is presented, the URC will trigger the behaviors of MAIN_RI pin.

NOTE

The URC can be outputted via UART port, USB AT port and USB modem port, which can be set by **AT+QURCCFG**. The default port is USB AT port.

In addition, MAIN_RI behavior can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 23: Behaviors of the MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns

The MAIN_RI behavior can be changed via **AT+QCFG**. See ***document [2]*** for details.

5 RF Specifications

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

Table 24: Pin Definition of Cellular Network Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	AIO	Main antenna interface	50 Ω impedance.

NOTE

Only passive antennas are supported.

Table 25: Operating Frequency

Operating Frequency	Transmit (MHz)	Receive (MHz)
GSM850	824–849	869–894
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990
WCDMA B1	1922–1978	2112–2168
WCDMA B2	1852–1908	1932–1988

WCDMA B5	826–847	871–892
WCDMA B8	882–913	927–958

5.1.2. Tx Power

Table 26: Tx Power

Frequency	Max. Tx Power	Min. Tx Power
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
GSM850 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
PCS1900 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
WCDMA B1/B2/B5/B8	24 dBm +1/-3 dB	< -49 dBm

NOTE

In GPRS 4 slots Tx mode, the maximum output power is reduced by 4 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

5.1.3. Rx Sensitivity

Table 27: Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO	
GSM850	-108 dBm	-	-	-102 dBm
EGSM900	-108 dBm	-	-	-102 dBm
DCS1800	-107.5 dBm	-	-	-102 dBm
PCS1900	-107 dBm	-	-	-102 dBm
WCDMA B1	-110 dBm	-	-	-106.7 dBm
WCDMA B2	-109 dBm	-	-	-104.7 dBm
WCDMA B5	-109.5 dBm	-	-	-104.7 dBm
WCDMA B8	-110 dBm	-	-	-103.7 dBm

5.1.4. Reference Design

The module provides one RF antenna interfaces for antenna connection.

It is recommended to reserve a Π-type matching circuit for better RF performance, and the Π-type matching components (C1, R1, C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

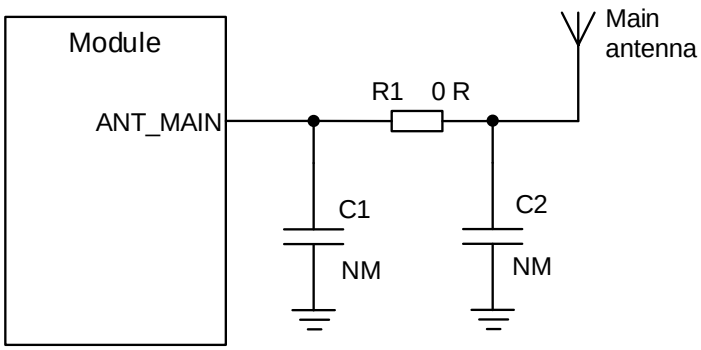


Figure 29: Reference Circuit for RF Antenna Interfaces

5.2. Reference Design of RF Routing

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

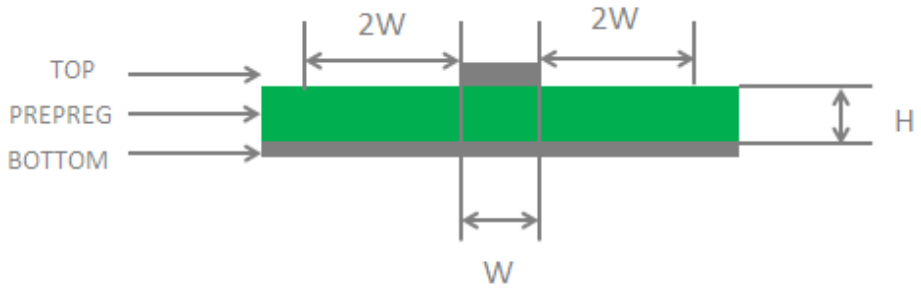


Figure 30: Microstrip Design on a 2-layer PCB

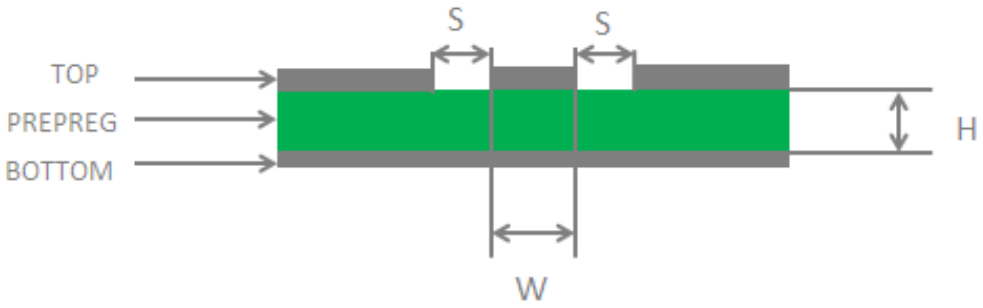


Figure 31: Coplanar Waveguide Design on a 2-layer PCB

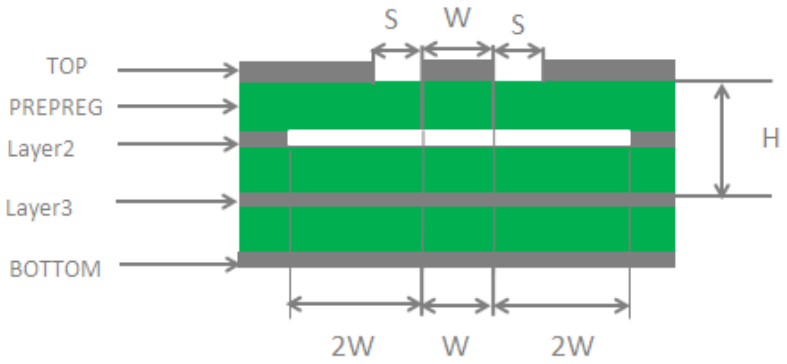


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

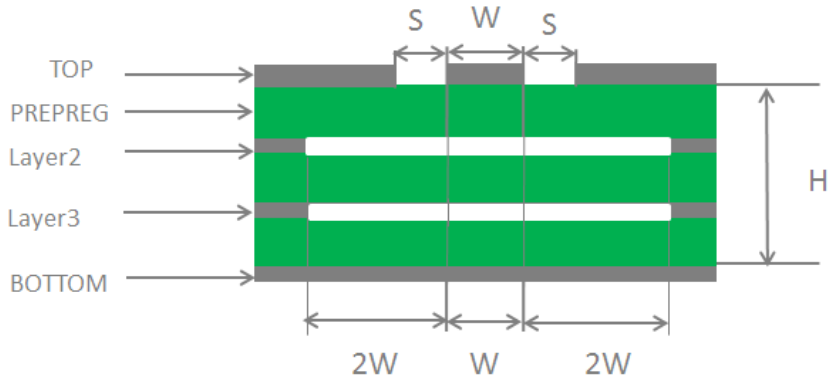


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.3. Requirements for Antenna Design

Table 28: Requirements for Antenna Design

Antenna Type	Requirements
GSM/UMTS	VSWR: ≤ 2 Efficiency: > 30 % Gain:1 dBi Max. input power: 50 W Input impedance: 50 Ω Polarization: vertical Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz)

5.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

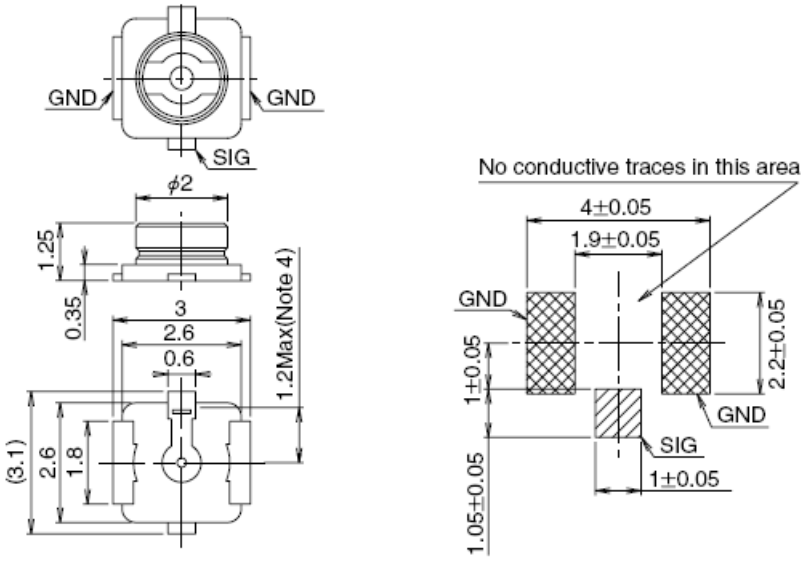


Figure 34: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series connectors listed in the following figure can be used to match the U.FL-R-SMT.

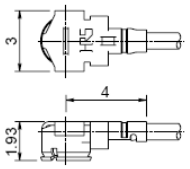
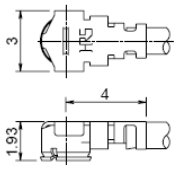
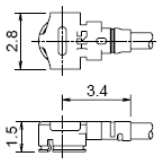
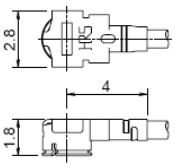
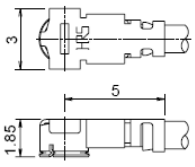
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 35: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of mated connector.

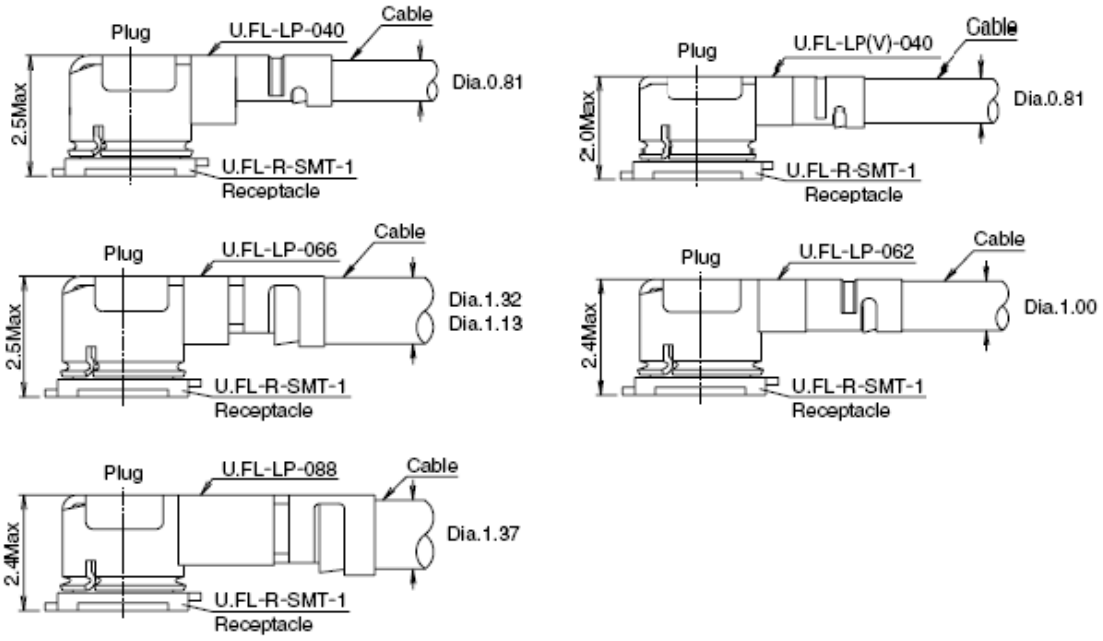


Figure 36: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 29: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	5.5	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	2.0	A
Voltage on Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

6.2. Power Supply Ratings

Table 30: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.4	3.8	4.5	V
	Voltage drop during burst transmission.	Maximum power control level at EGSM900.	0	0	400	mV
I_{VBAT_RF}	Peak supply current (during transmission slot)	Maximum power control level at EGSM900.	-	-	2.0	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

6.3. Power Consumption

Table 31: Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	12	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.89	mA
	EGSM900 @ DRX = 2 (USB disconnected)	1.81	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.35	mA
	EGSM900 @ DRX = 5 (USB suspend)	1.52	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.25	mA
	DCS1800 @ DRX = 2 (USB disconnected)	1.77	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.35	mA
	DCS1800 @ DRX = 5 (USB suspend)	1.48	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.26	mA

	WCDMA @ PF = 64 (USB disconnected)	2.33	mA
	WCDMA @ PF = 64 (USB suspend)	2.49	mA
	WCDMA @ PF = 128 (USB disconnected)	1.65	mA
	WCDMA @ PF = 256 (USB disconnected)	1.31	mA
	WCDMA @ PF = 512 (USB disconnected)	1.15	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	19.99	mA
	EGSM900 @ DRX = 5 (USB connected)	34.56	mA
	WCDMA @ PF = 64 (USB disconnected)	19.75	mA
	WCDMA @ PF = 64 (USB connected)	34.31	mA
GPRS data transmission	GSM850 4DL/1UL @ 32.78 dBm	300	mA
	GSM850 3DL/2UL @ 32.78 dBm	460	mA
	GSM850 2DL/3UL @ 31.22 dBm	550	mA
	GSM850 1DL/4UL @ 29.19 dBm	610	mA
	EGSM900 4DL/1UL @ 32.34 dBm	300	mA
	EGSM900 3DL/2UL @ 32.31 dBm	450	mA
	EGSM900 2DL/3UL @ 31.08 dBm	540	mA
	EGSM900 1DL/4UL @ 29.28 dBm	600	mA
	DCS1800 4DL/1UL @ 29.65 dBm	260	mA
	DCS1800 3DL/2UL @ 29.58 dBm	400	mA
	DCS1800 2DL/3UL @ 28.03 dBm	480	mA
	DCS1800 1DL/4UL @ 26.16 dBm	560	mA
	PCS1900 4DL/1UL @ 29.63 dBm	260	mA
	PCS1900 3DL/2UL @ 29.63 dBm	400	mA
	PCS1900 2DL/3UL @ 28.11 dBm	480	mA
	PCS1900 1DL/4UL @ 26.24 dBm	560	mA

EDGE data transmission	GSM850 4DL/1UL @ 27.53 dBm	270	mA
	GSM850 3DL/2UL @ 27.51 dBm	400	mA
	GSM850 2DL/3UL @ 25.47 dBm	520	mA
	GSM850 1DL/4UL @ 23.28 dBm	600	mA
	EGSM900 4DL/1UL @ 27.06 dBm	270	mA
	EGSM900 3DL/2UL @ 26.87 dBm	400	mA
	EGSM900 2DL/3UL @ 25.01 dBm	520	mA
	EGSM900 1DL/4UL @ 22.87 dBm	600	mA
	DCS1800 4DL/1UL @ 25.66 dBm	240	mA
	DCS1800 3DL/2UL @ 25.50 dBm	340	mA
	DCS1800 2DL/3UL @ 23.95 dBm	420	mA
	DCS1800 1DL/4UL @ 21.93 dBm	500	mA
	PCS1900 4DL/1UL @ 26.62 dBm	240	mA
	PCS1900 3DL/2UL @ 26.06 dBm	340	mA
	PCS1900 2DL/3UL @ 24.38 dBm	420	mA
	PCS1900 1DL/4UL @ 22.30 dBm	500	mA
WCDMA data transmission	WCDMA B1 HSDPA @ 22. 6 dBm	610	mA
	WCDMA B2 HSDPA @ 22.26 dBm	600	mA
	WCDMA B5 HSDPA @ 22.68 dBm	550	mA
	WCDMA B8 HSDPA @ 22.64 dBm	570	mA
	WCDMA B1 HSUPA @ 22.30 dBm	610	mA
	WCDMA B2 HSUPA @ 22.30 dBm	600	mA
	WCDMA B5 HSUPA @ 22.20 dBm	550	mA
	WCDMA B8 HSUPA @ 22.30 dBm	570	mA

GSM voice call	GSM900 PCL = 5 @ 32.24 dBm	290	mA
	GSM900 PCL = 12 @ 19.09 dBm	160	mA
	GSM900 PCL = 19 @ 5.82 dBm	120	mA
	EGSM900 PCL = 5 @ 32.24 dBm	300	mA
	EGSM900 PCL = 12 @ 19.09 dBm	160	mA
	EGSM900 PCL = 19 @ 5.82 dBm	130	mA
	DCS1800 PCL = 0 @ 29.40 dBm	260	mA
	DCS1800 PCL = 7 @ 15.75 dBm	160	mA
	DCS1800 PCL = 15 @ -0.43 dBm	140	mA
	PCS1800 PCL = 0 @ 29.40 dBm	250	mA
	PCS1800 PCL = 7 @ 15.75 dBm	150	mA
	PCS1800 PCL = 15 @ -0.43 dBm	130	mA
WCDMA voice call	WCDMA B1 @ 22.77 dBm	600	mA
	WCDMA B2 @ 22.77 dBm	610	mA
	WCDMA B5 @ 22.42 dBm	550	mA
	WCDMA B8 @ 22.43 dBm	580	mA

6.4. Digital I/O Characteristic

Table 32: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.2	2.0	V
V_{IL}	Input low voltage	-0.3	0.6	V
V_{OH}	Output high voltage	1.35	1.8	V
V_{OL}	Output low voltage	-0.3	0.45	V

Table 33: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.7	1.9	V
V_{IH}	Input high voltage	1.2	2.0	V
V_{IL}	Input low voltage	-0.3	0.6	V
V_{OH}	Output high voltage	1.35	1.8	V
V_{OL}	Output low voltage	-0.3	0.45	V

Table 34: (U)SIM 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.05	V
V_{IH}	Input high voltage	1.95	3.05	V
V_{IL}	Input low voltage	-0.3	1.0	V
V_{OH}	Output high voltage	2.55	3.0	V
V_{OL}	Output low voltage	-0.3	0.45	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

ESD characteristics of the module's pins are as follows:

Table 35: Electrostatics Discharge Characteristics (25 °C, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±10	kV

Antenna Interfaces	±8	±10	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 36: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [3]	-35	+25	+75	°C
Extended Operating Temperature Range [4]	-40	-	+85	°C
Storage temperature range	-40	-	+90	°C

[3] Within the operating temperature range, the module meets 3GPP specifications.
[4] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

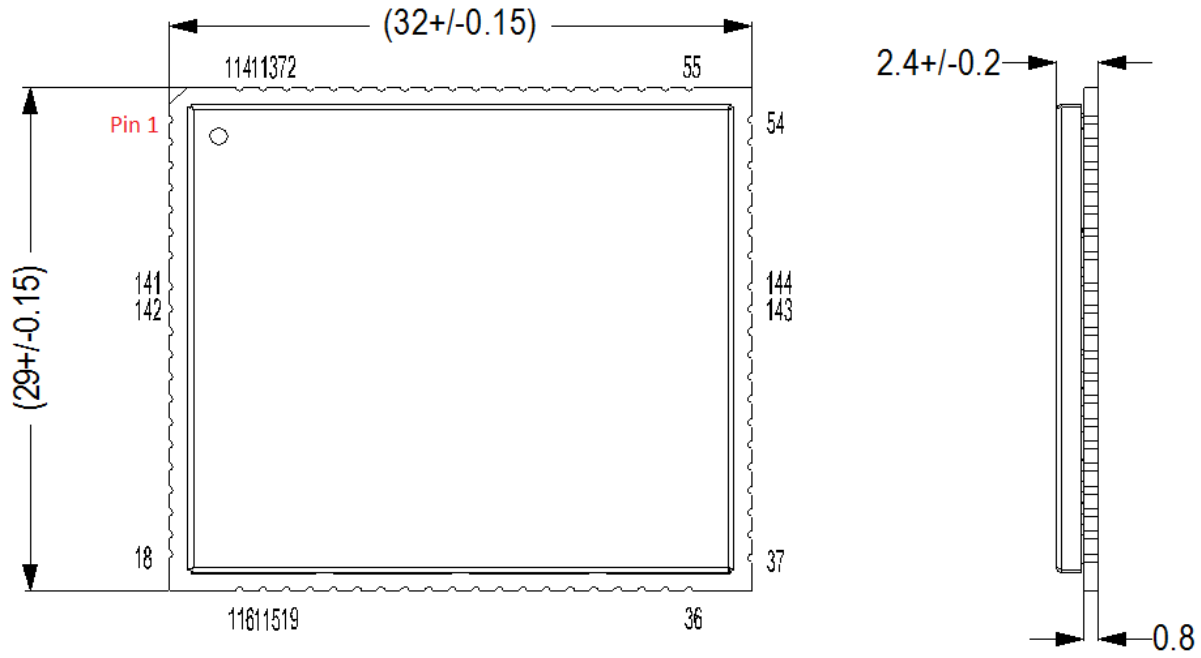


Figure 37: Module Top and Side Dimensions (Unit: mm)

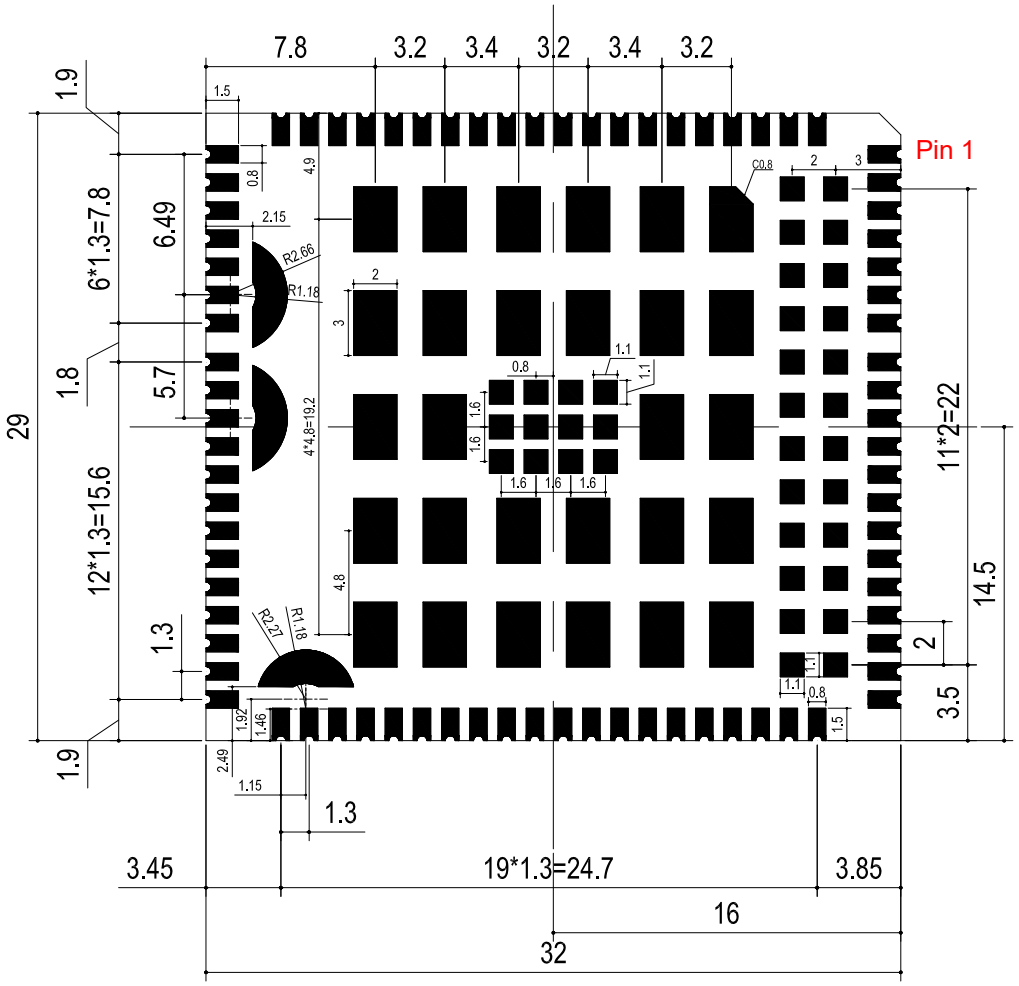


Figure 38: Module Bottom Dimensions View (Unit: mm)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

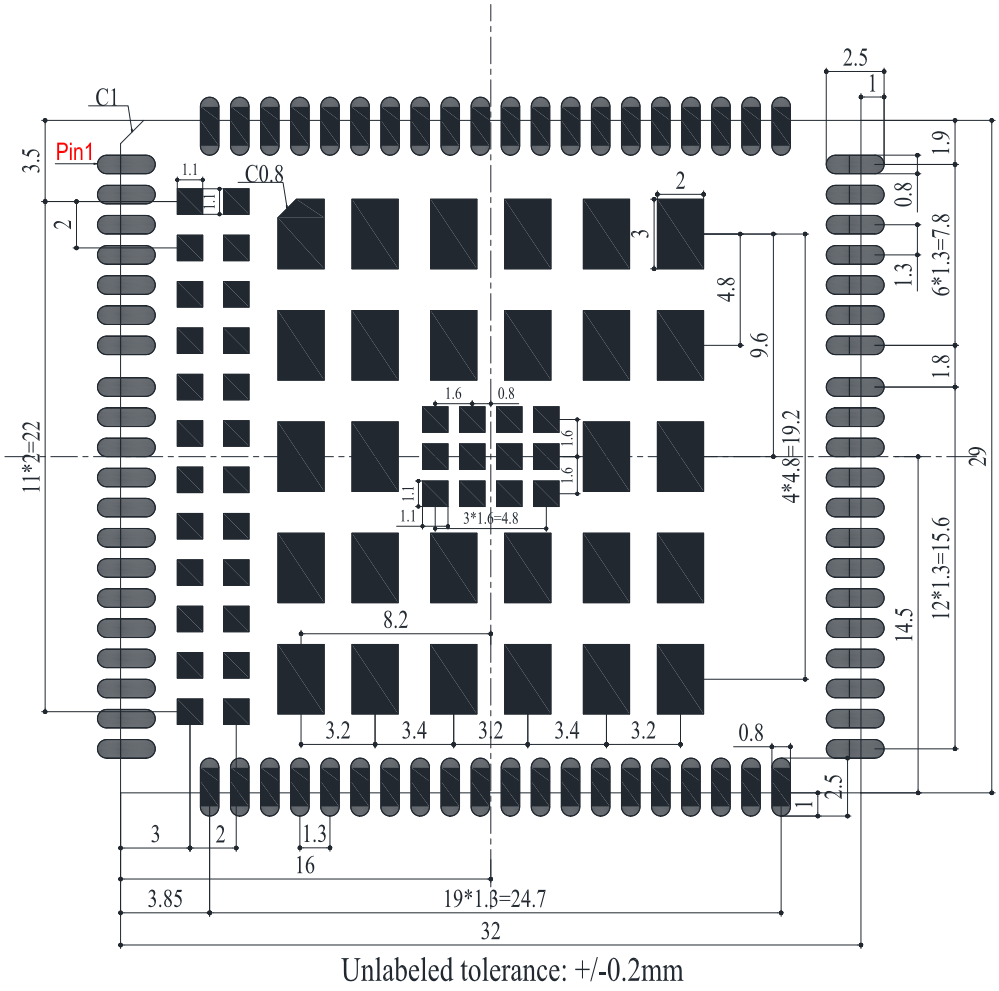


Figure 39: Recommended Footprint (Bottom View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

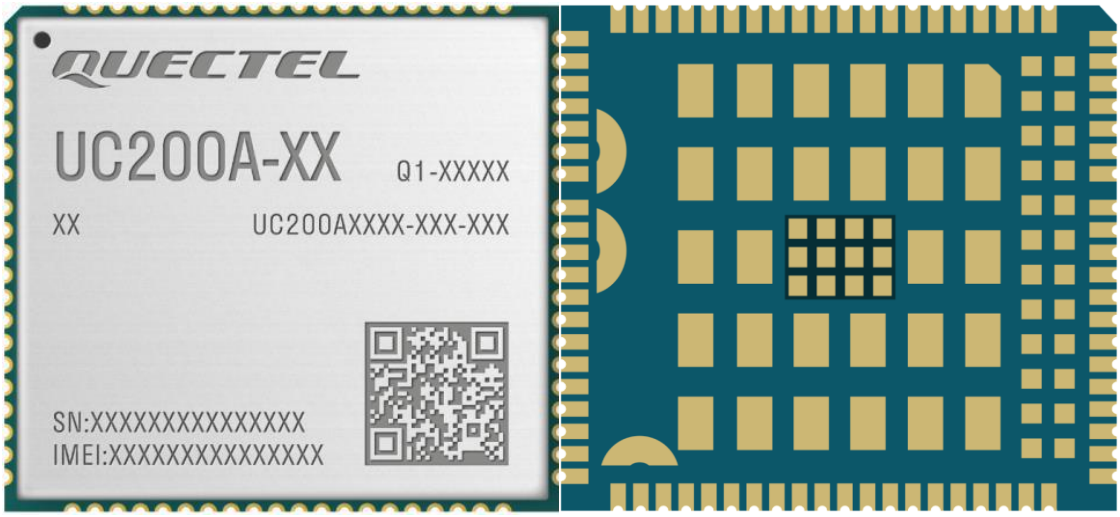


Figure 40: Top and Bottom View of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed package. MSL of the module is rated as 3, and its storage restrictions are shown as below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [5] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[5] This floor life is only applicable when the environment conforms to IPC/JEDEC J-STD-033. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to IPC/JEDEC J-STD-033. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document [4]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

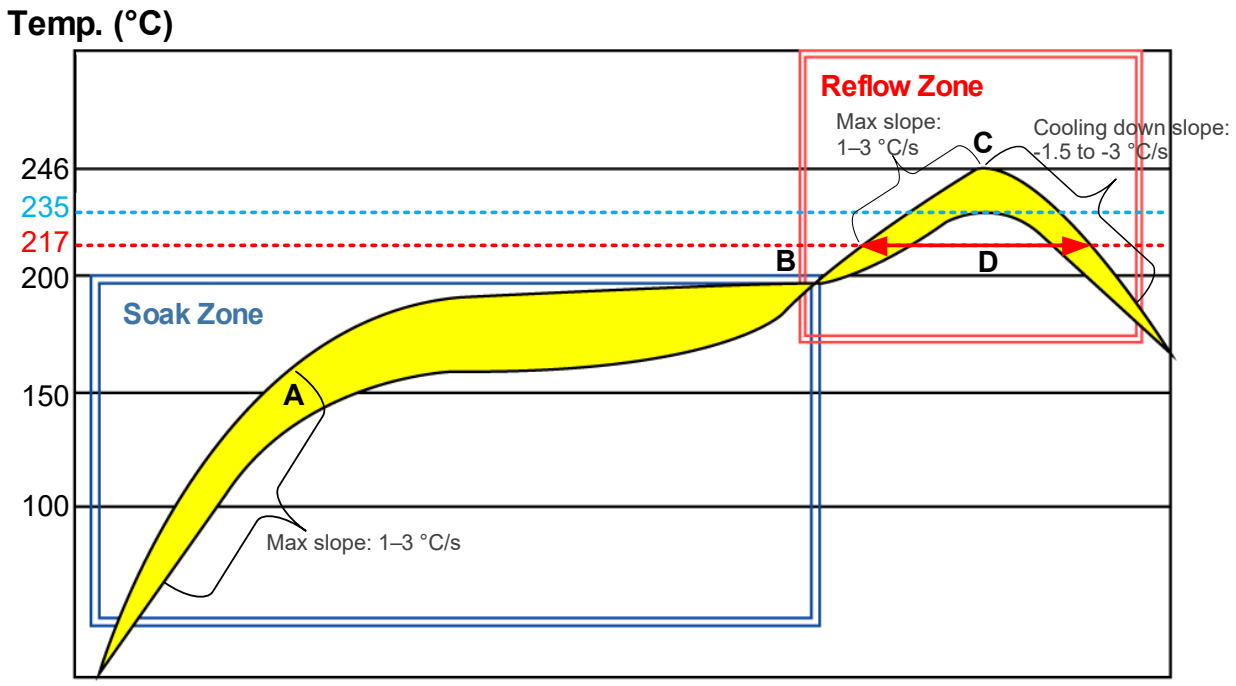


Figure 41: Recommended Reflow Soldering Thermal Profile

Table 37: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	1–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235 °C to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts injection tray packaging and details are as follow:

8.3.1. Carrier Tape

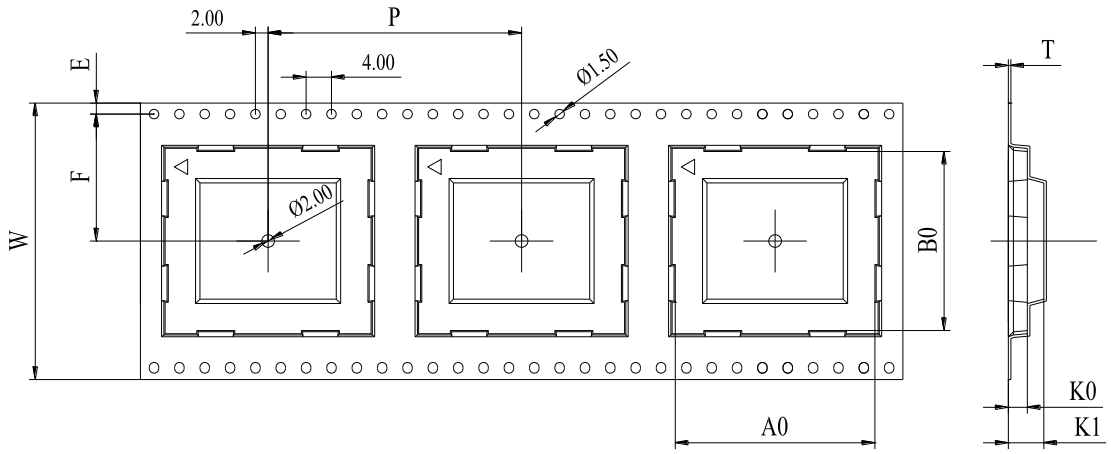


Figure 42: Carrier Tape Dimension Drawing

Table 38: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	44	0.35	32.5	29.5	3.0	3.8	20.2	1.75

8.3.2. Plastic Reel

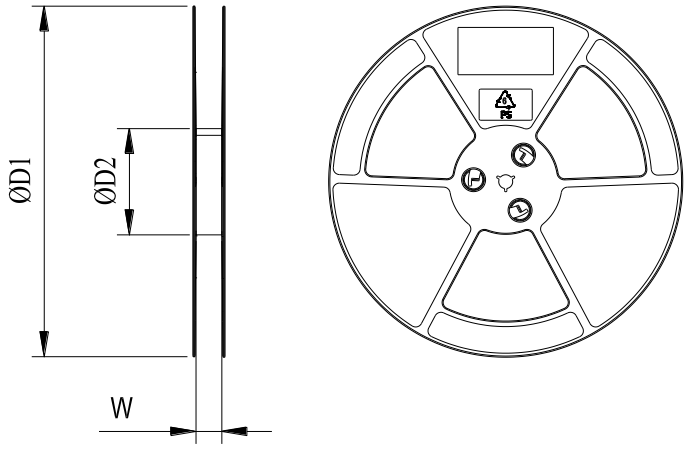
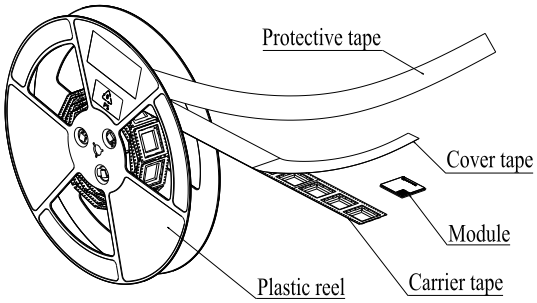


Figure 43: Plastic Reel Dimension Drawing

Table 39: Plastic Reel Dimension Table (Unit: mm)

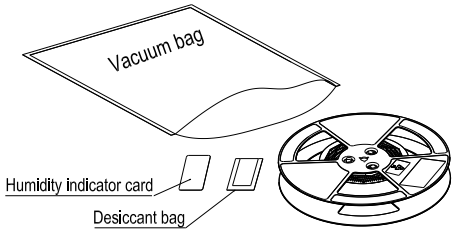
øD1	øD2	W
330	100	44.5

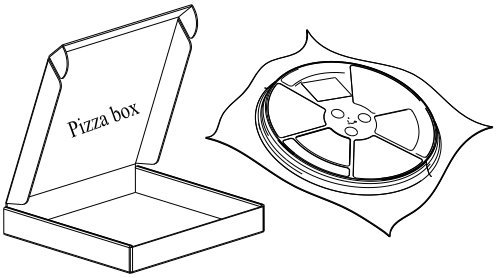
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 1000 modules.

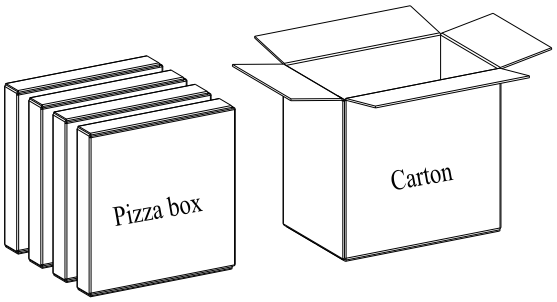


Figure 44: Packaging Process

9 Appendix References

Table 40: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_UC200T_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_Secondary_SMT_Application_Note

Table 41: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
AMR	Adaptive Multi-Rate
AMR-WB	Adaptive Multi-Rate Wideband
bps	Bytes per second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection MUX
CPE	Customer-Premise Equipment
CS	Coding Scheme
CTS	Clear To Send
DCS	Data Coding Scheme
DFOTA	Delta Firmware Upgrade Over-The-Air

DRX	Discontinuous Reception
DTE	Data Terminal Equipment
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FILE	File Protocol
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP over SSL
GMSK	Gaussian Filtered Minimum Shift Keying
GND	Ground
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA+	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IMT-2000	International Mobile Telecommunications 2000

LCC	Leadless Chip Carrier (package)
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MCU	Microcontroller Unit
MCS	Modulation and Coding Scheme
MLCC	Multi-layer Ceramic Capacitor
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MSB	Most Significant Bit
MSL	Moisture Sensitivity Levels
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
OTT	Over The Top
PA	Power Amplifier
PAM	Power Amplifier Module
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PF	Paging Frame
PING	Packet Internet Groper
PPP	Point-to-Point Protocol

PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RAM	Random Access Memory
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SDIO	Secure Digital Input and Output Card
SMS	Short Message Service
SMT	Surface Mount Technology
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}	High-level Input Voltage

V_{IL}	Low-level Input Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access