FCM360W Hardware Design

Wi-Fi&Bluetooth Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-03-08	Mark WU	Creation of the document
1.0	2023-10-18	Rudolf YANG/Orange LI	First official release

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio
- Apply anti-copy encryption technology to enhance product safety

This document defines FCM360W in QuecOpen® solution and describes its air interfaces and hardware interfaces, which are connected with your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument, and so on, it indicates that the function, feature, interface, pin, AT command, argument, and so on, is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

FCM360W is a high-performance MCU Wi-Fi and Bluetooth module supporting IEEE 802.11b/g/n/ax and BLE 5.1 standards. The module provides multiple interfaces including UART, SPI, I2C*, I2S, SDIO*, ADC and PWM for various applications.

FCM360W is an SMD module with compact packaging. It includes:

- 240 MHz RISC processor
- 48 KB ROM, 512 KB SRAM and a built-in 4 MB/ 8 MB flash
- Support secondary development

Table 2: Basic Information

FCM360W	
Packaging type	LCC
Pin counts	39
Dimensions	(25.5 ±0.2) mm × (18.0 ±0.2) mm × (3.2 ±0.2) mm
Weight	Approx. 1.65 g

2.1. Key Features

Table 3: Key Features

Basic Information	
Protocols and Standards	● Wi-Fi Protocols: IEEE 802.11b/g/n/ax ● Bluetooth protocol: BLE 5.1 ● All hardware components are fully compliant with EU RoHS directive
Power Supply	**VBAT Power Supply:** ● 3.0–3.6 V ● Typ.: 3.3 V
Temperature Ranges [1]	● **Design Solution 1:** − Operating temperature: -40 to +85 °C − Storage temperature: -45 to +95 °C ● **Design Solution 2:** − Operating temperature: -40 to +105 °C − Storage temperature: -45 to +115 °C
EVB Kit	FCM360W TE-B [2]
Antenna/Antenna Interface	
Antenna/Antenna Interfaces [3]	● Pin antenna interface (ANT_WIFI/BT) ● PCB antenna ● RF coaxial connector ● 50 Ω characteristic impedance
Application Interfaces [4]	
Application Interfaces	UART, SPI, I2C*, I2S, SDIO*, PWM, ADC

[1] The module is provided with two temperature design solutions. For more details, please contact Quectel Technical Support. Within the operating temperature range, the module's related performance meets IEEE and Bluetooth specifications.
[2] For more details about the EVB, see ***document [1]***.
[3] The module is provided with one of the three antenna/antenna interface designs. For more details, please contact Quectel Technical Support.
[4] For more details about the interfaces, see ***Chapter 3.3*** and ***Chapter 3.4***.

2.2. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

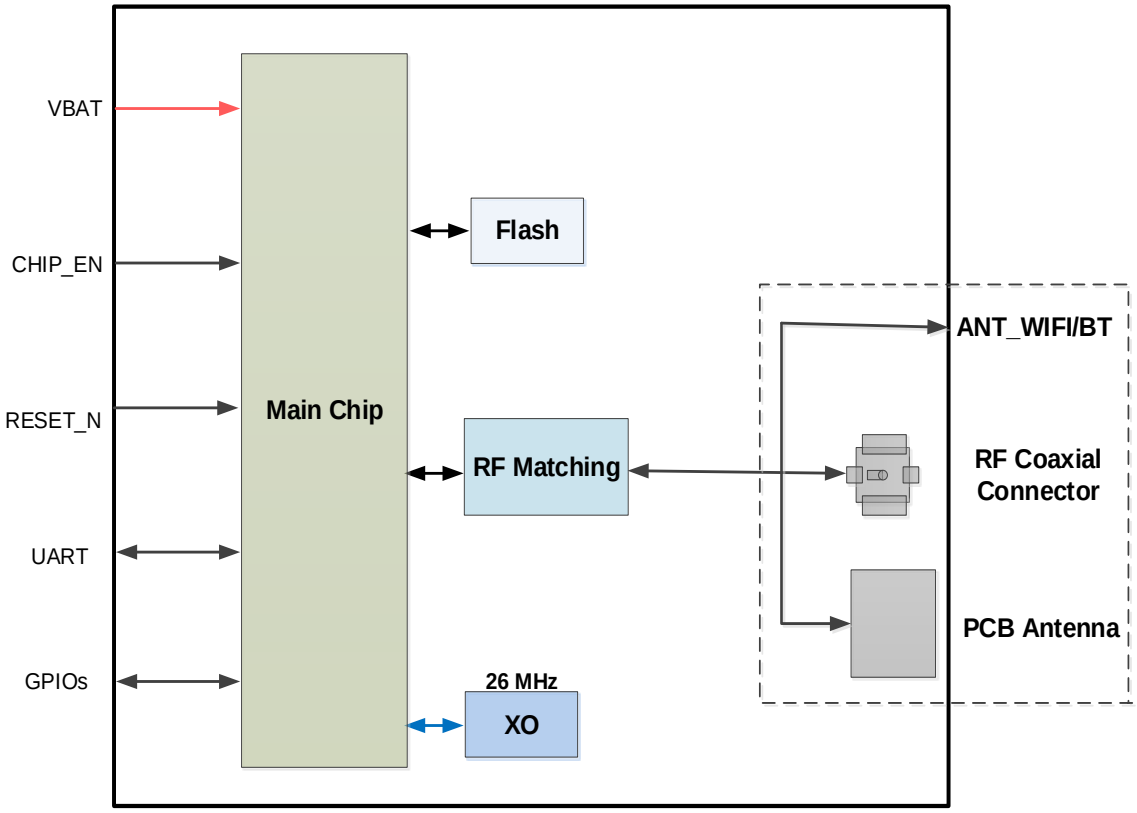


Figure 1: Functional Diagram

NOTE

The module is provided with one of the three antenna/antenna interface designs. For more details, please contact Quectel Technical Support.

3 Application Interfaces

3.1. Pin Assignment

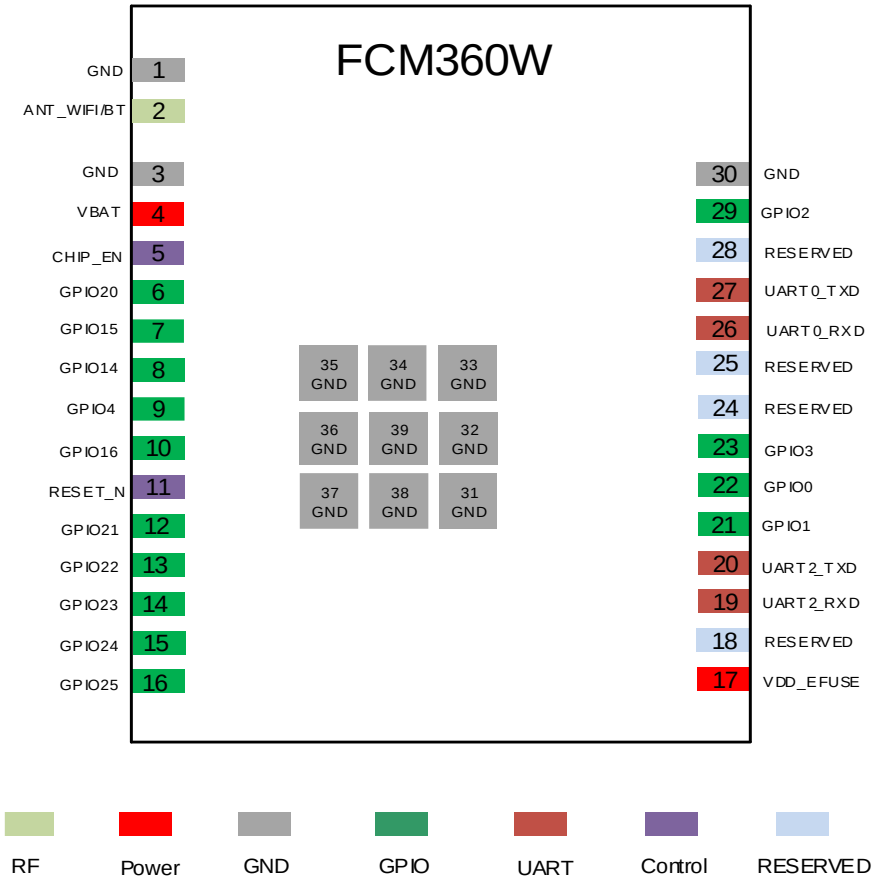


Figure 2: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED and unused pins open.
2. All GND pins should be connected to ground.
3. The module provides 2 UARTs and 14 GPIO interfaces by default. In the case of multiplexing, it supports interfaces including SPI, I2C*, SDIO*, PWM, I2S and ADC. For more details, see ***Chapter 3.3*** and ***Chapter 3.4***.

3.2. Pin Description

Table 4: Parameter Description

Parameter	Description
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input

DC characteristics include power domain and rated current.

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	4	PI	Power supply for the module	Vmax = 3.6 V Vmin = 3.0 V Vnom = 3.3 V	It must be provided with sufficient current more than 0.6 A.
VDD_EFUSE	17	PI	Power supply for eFuse programming	Vmax = 3.3 V Vmin = 0 V Vnom = 1.8 V	If unused, keep it open.
GND	1, 3, 30, 31–39				
Control Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	11	DI	Reset the module	VBAT	Internally pulled up to VBAT. Active low.
CHIP_EN	5	DI	Enable the module		Internally pulled up to VBAT. Active high.

UARTs					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART0_TXD	27	DO	UART0 transmit	VBAT	
UART0_RXD	26	DI	UART0 receive		
UART2_TXD	20	DO	UART2 transmit		Test points must be reserved.
UART2_RXD	19	DI	UART2 receive		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO20	6	DIO	General-purpose input/output	VBAT	
GPIO15	7	DIO	General-purpose input/output		
GPIO14	8	DIO	General-purpose input/output		
GPIO4	9	DIO	General-purpose input/output		
GPIO16	10	DIO	General-purpose input/output		
GPIO21	12	DIO	General-purpose input/output		
GPIO22	13	DIO	General-purpose input/output		
GPIO23	14	DIO	General-purpose input/output		
GPIO24	15	DIO	General-purpose input/output		
GPIO25	16	DIO	General-purpose input/output		
GPIO1	21	DIO	General-purpose input/output		Interrupt wakeup.
GPIO0	22	DIO	General-purpose input/output		
GPIO3	23	DIO	General-purpose input/output		
GPIO2	29	DIO	General-purpose input/output		Interrupt wakeup.

RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_WIFI/BT	2	AIO	Wi-Fi/Bluetooth antenna interface		50 Ω characteristic impedance.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	18, 24, 25, 28				Keep them open.

3.3. GPIO Multiplexing

The module provides 14 GPIO interfaces by default, and can support up to 18 GPIO interfaces in the case of multiplexing. Pins are defined as follows:

Table 6: GPIO Multiplexing

Pin Name	Pin No.	Alternate Function 0 (GPIO No.)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	Alternate Function 5	Comment
GPIO4	9	GPIO4	TRST	UART0_RTS	PWM0	SPI_CS2	-	TRST: JTAG test reset
GPIO16	10	GPIO16	PWM2	UART1_CTS	IR_OUT	-	-	IR_OUT: IrDA output
GPIO21	12	GPIO21	SDIO_CMD	UART0_RXD	I2S_TXD	I2C_SDA	-	
GPIO22	13	GPIO22	PWM0	SDIO_DATA0	UART0_TXD	I2S_TX_WS	-	
GPIO23	14	GPIO23	PWM1	SDIO_DATA1	UART1_RTS	I2S_TX_SCK	-	
GPIO24	15	GPIO24	PWM2	SDIO_DATA2	UART1_CTS	I2S_MCLK	-	
GPIO25	16	GPIO25	PWM3	SDIO_DATA3	I2C_SDA	-	-	
GPIO20	6	GPIO20	ADC2	PWM3	I2S_MCLK	SD_DET	-	
GPIO15	7	GPIO15	ADC1	BOOTMODE1	PWM5	I2S_TX_WS	-	

GPIO14	8	GPIO14	ADC0	BOOTMODE0	PWM4	I2S_TXD	-	
UART2_RXD	19	GPIO17	WAKEUP	SPI_WP	PWM5	I2S_TX_WS	-	
UART2_TXD	20	GPIO13	SDIO_CLK	I2C_SCL	I2S_RXD	-	-	
GPIO1	21	GPIO1	SPI_CS0	TMS	UART1_RXD	PWM1	I2S_RXD	TMS: JTAG test mode selection
GPIO0	22	GPIO0	SPI_CLK	TCK	UART2_TXD	PWM0	I2S_TX_SCK	TCK: JTAG test clock
GPIO3	23	GPIO3	SPI_MISO	TDI	UART0_CTS	PWM3	I2C_SDA	TDI: JTAG test data input
GPIO2	29	GPIO2	SPI_MOSI	TDO	UART1_TXD	PWM2	I2C_SCL	TDO: JTAG test data output
UART0_RXD	26	GPIO5	40M_CLK_OUT	IR_OUT	I2S_RX_WS	XTAL_I_32K	-	IR_OUT: IrDA output
UART0_TXD	27	GPIO6	COLD_RESET	32K_CLK_OUT	I2S_RX_SCK	XTAL_O_32K	-	

NOTE

1. The GPIO0, GPIO1, GPIO2 and UART2_RXD can be used as interrupt wake-up to wake up the module and then make the module into operating state by pulling them down.
2. The maximum number of application interfaces multiplexed through GPIOs isn't available simultaneously. For the maximum number of different application interfaces that the module can support, see ***Chapter 3.4*** for details.

3.4. Application Interfaces

3.4.1. UARTs

The module supports 2 UARTs by default: UART0 and UART2. In the case of multiplexing, it supports 3 UARTs: UART0, UART1 and UART2.

Table 7: Pin Definition of UARTs

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
UART0_TXD	27	-	DO	UART0 transmit	Other configurations for UART, see ***Table 6***.
UART0_RXD	26	-	DI	UART0 receive	
GPIO3	23	UART0_CTS	DO	Clear to send signal to the module	
GPIO4	9	UART0_RTS	DI	Request to send signal from the module	
GPIO2	29	UART1_TXD	DO	UART1 transmit	
GPIO1	21	UART1_RXD	DI	UART1 receive	
GPIO16	10	UART1_CTS	DO	Clear to send signal to the module	
GPIO23	14	UART1_RTS	DI	Request to send signal from the module	
UART2_TXD	20	-	DO	UART2 transmit	
UART2_RXD	19	-	DI	UART2 receive	

The UART0 can be used for data transmission with the baud rate of 115200 bps by default, and the actual measurement can reach 2 Mbps. The UART0 can also be used for firmware upgrade with the baud rate of 921600 bps by default, and the baud rate can be configurable. Among them, the default UART0 (pins 26 and 27) can be used for data transmission, downloading, debugging, and log printing; the UART0 multiplexed through pins 12 and 13 can only be used for data transmission and debugging.

The module provides 3.3 V UARTs. You can use a voltage-level translator between the module and external MCU's UART if the MCU is equipped with a 1.8 V UART.

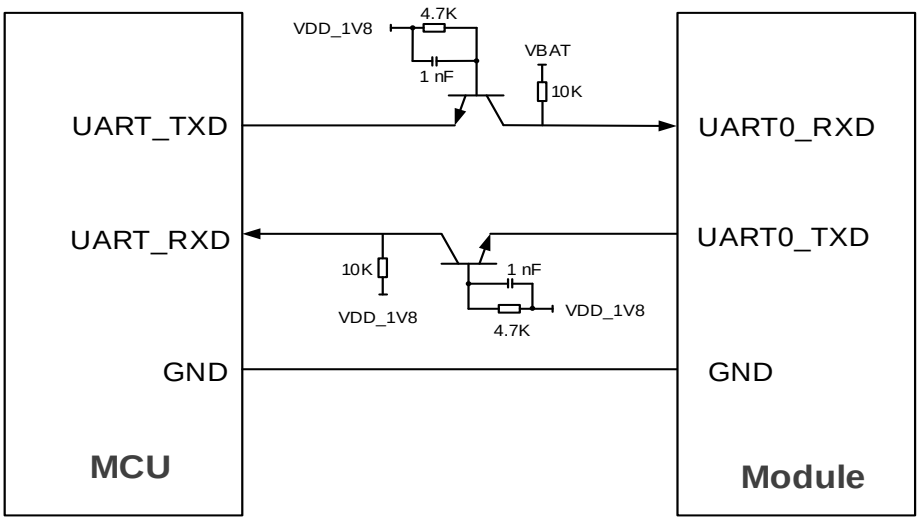


Figure 3: Level-shifting Circuit for UART0

NOTE

The transistor level-shifting circuit above is not suitable for applications with baud rates exceeding 460800 bps.

The UART1 and UART2 can all be used for data transmission, AT command communication and debugging with default baud rate of 115200 bps, but they are not recommended to be used for downloading. The UART2 is used for AT command communication by default in the standard firmware.

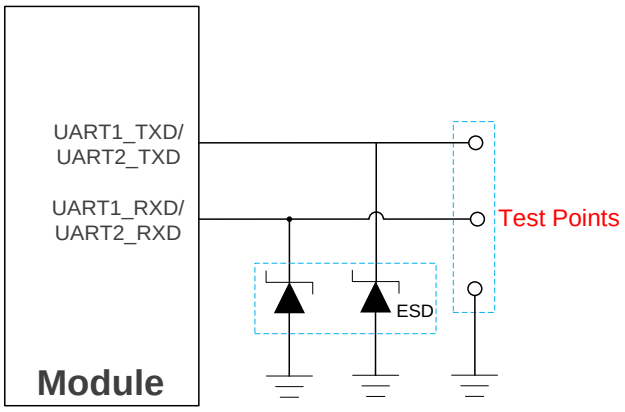


Figure 4: UART1/UART2 Reference Design

NOTE

Test points must be reserved for UART1_TXD, UART2_TXD, UART1_RXD and UART2_RXD.

3.4.2. SPI

In the case of multiplexing, the module provides one SPI that supports both master and slave modes. The maximum clock frequency of the interface can reach 20 MHz in slave mode, and 40 MHz in master mode.

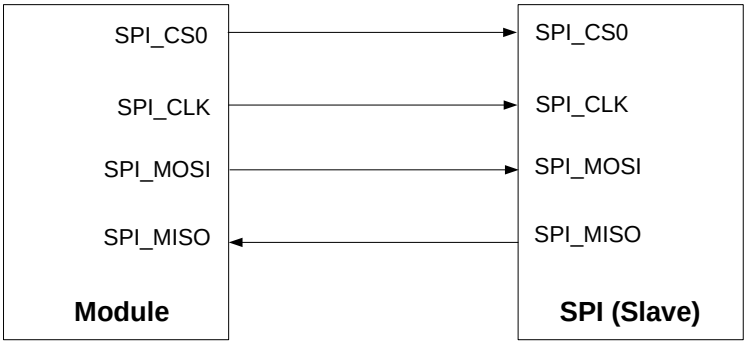


Figure 5: SPI Connection (Master Mode)

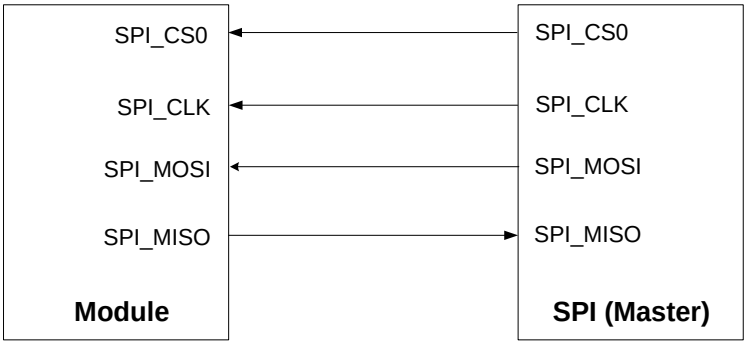


Figure 6: SPI Connection (Slave Mode)

Table 8: Pin Definition of SPI

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO1	21	SPI_CS0	DIO	SPI chip select	In master mode, it is an output signal; In slave mode, it is an input signal.
GPIO0	22	SPI_CLK	DIO	SPI clock	In master mode, it is an output signal; In slave mode, it is an input signal.
GPIO3	23	SPI_MISO	DIO	SPI master-in	In master mode, it is an input

				slave-out	signal; In slave mode, it is an output signal.
GPIO2	29	SPI_MOSI	DIO	SPI master-out slave-in	In master mode, it is an output signal; In slave mode, it is an input signal.

3.4.3. I2C Interface*

In the case of multiplexing, the module provides one I2C interface that supports both master and slave modes. It supports:

- AMBA 2.0 APB bus protocol
- Standard-mode (100 kbps) and fast-mode (400 kbps)
- Programmable master and slave modes
- 7-bit and 10-bit addressing modes
- Automatic clock stretching
- Programmable clock and data timing
- DMA data transmission
- Universal call address

Table 9: Pin Definition of I2C Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO2	29	I2C_SCL	OD	I2C serial clock	Other configurations for I2C, see ***Table 6***.
GPIO3	23	I2C_SDA	OD	I2C serial data	

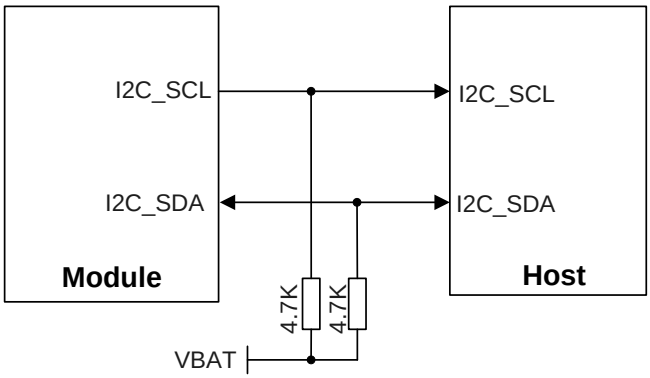


Figure 7: Reference Design for I2C Interface

3.4.4. SDIO Interface*

In the case of multiplexing, the module provides one SDIO interface that supports master mode only.

Table 10: Pin Definition of SDIO Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description
GPIO21	12	SDIO_CMD	DIO	SDIO command
UART2_TXD	20	SDIO_CLK	DI	SDIO clock
GPIO25	16	SDIO_DATA3	DIO	SDIO data bit 3
GPIO24	15	SDIO_DATA2	DIO	SDIO data bit 2
GPIO22	13	SDIO_DATA0	DIO	SDIO data bit 0
GPIO23	14	SDIO_DATA1	DIO	SDIO data bit 1
GPIO20	6	SD_DET	DI	SD card hot-plug detect

The SDIO interface connection between the module and the SD card connector is illustrated in the following figure.

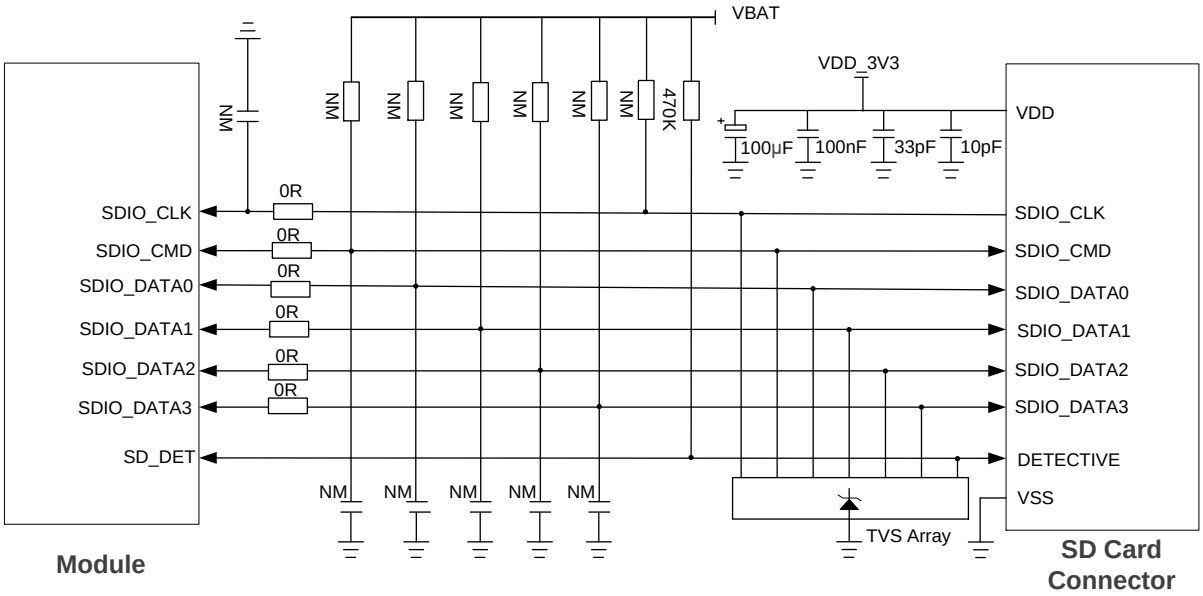


Figure 8: Reference Design for SDIO Interface

To ensure compliance of interface design with the SDIO 3.0 specification, please comply with the following principles for SDIO interface design.

- To enhance signal quality, add 0 Ω resistors in series and reserve capacitors (not mounted by default) between the module and the SD card connector. All resistors and capacitors should be placed close to the connector.
- Place the TVS array close to the SD card connector with a parasitic capacitance no greater than 2 pF.
- Route the SDIO traces in inner layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below. The impedance of SDIO signal trace is 50 Ω ±10 %.
- Keep SDIO signals far away from other sensitive circuits/signals, such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- The distance between SDIO signals and other signals must be greater than twice the trace width, and the bus load capacitance must be less than 15 pF.
- SDIO signal traces need to be equal length (the distance between the traces should be less than 0.5 mm).

3.4.5. PWM Interfaces

In the case of multiplexing, the module supports 6 PWM channels. Pin description of PWM interfaces are as follows.

Table 11: Pin Definition of PWM Interfaces

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO16	10	PWM2	DO	PWM2 out	Other configurations for PWM, see ***Table 6***.
GPIO23	14	PWM1	DO	PWM1 out	
GPIO25	16	PWM3	DO	PWM3 out	
GPIO15	7	PWM5	DO	PWM5 out	
GPIO14	8	PWM4	DO	PWM4 out	
GPIO4	9	PWM0	DO	PWM0 out	

3.4.6. I2S Interface

In the case of multiplexing, the module supports one I2S interface for transmission of digital audio data between internal components of the system, such as Codec, DSP, digital input/output interface, ADC, DAC and digital filter.

Table 12: Pin Definition of I2S Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
GPIO1	21	I2S_RXD	DI	I2S receive data	Other configurations for I2S, see ***Table 6***.
GPIO14	8	I2S_TXD	DO	I2S transmit data	
GPIO20	6	I2S_MCLK	OD	I2S master clock	
GPIO0	22	I2S_TX_SCK	DIO	I2S transmit serial clock	
GPIO15	7	I2S_TX_WS	DIO	I2S transmit word select	

3.4.7. ADC Interfaces

In the case of multiplexing, the module supports 3 ADC interfaces, whose voltage range is 0–3.3 V. To improve ADC accuracy, surround ADC trace with ground.

Table 13: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Multiplexing Function	I/O	Description
GPIO20	6	ADC2	AI	General-purpose ADC interface
GPIO15	7	ADC1	AI	General-purpose ADC interface
GPIO14	8	ADC0	AI	General-purpose ADC interface

Table 14: ADC Features

Parameter	Min.	Typ.	Max.	Unit
ADC Voltage Range	0	-	3.3	V
ADC Resolution	-	12	-	bit
ADC Sample Rate	-	1.25	-	MHz

NOTE

1. It is prohibited to directly supply any voltage to ADC interfaces when the module is not powered by the VBAT.
2. It is recommended to use resistor divider circuit for ADC interface application with 1 % accuracy resistor divider.

4 Operating Characteristics

4.1. Power Supply

Power supply pin and ground pins of the module are defined in the following table.

Table 15: Pin Definition of Power Supply and GND Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT	4	PI	Power supply for the module	3.0	3.3	3.6	V
GND	1, 3, 30, 31–39						

4.1.1. Reference Design for Power Supply

The module is powered by VBAT, and it is recommended that the power supply chip for VBAT provide sufficient current of 0.6 A at least. For better power supply performance, it is recommended to parallel a 22 μF decoupling capacitor, and two filter capacitors (1 μF and 100 nF) near the module's VBAT pin. Reserve C4 for debugging which is not mounted by default. In addition, it is recommended to add a TVS near the VBAT to improve the surge voltage bearing capacity of the module. In principle, the longer the VBAT trace is, the wider it should be.

VBAT reference circuit is shown below:

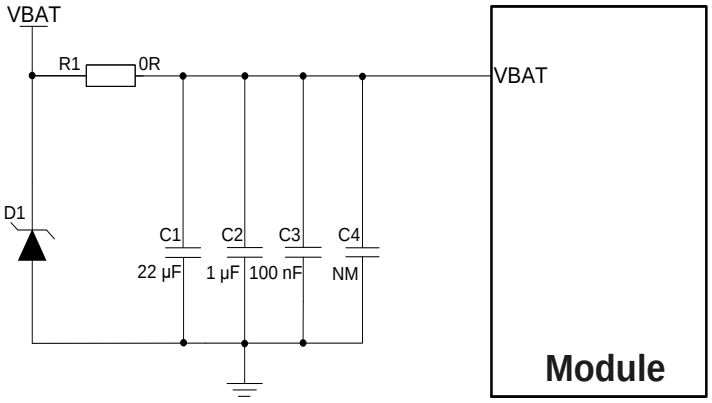


Figure 9: VBAT Reference Circuit

4.2. Turn On

After the module VBAT is powered on, keep the CHIP_EN pin at high level to realize the automatic startup of the module.

Table 16: Pin Definition of CHIP_EN

Pin Name	Pin No.	I/O	Description	Comment
CHIP_EN	5	DI	Enable the module	Internally pulled up to VBAT. Active high.

The turn-on timing is shown below:

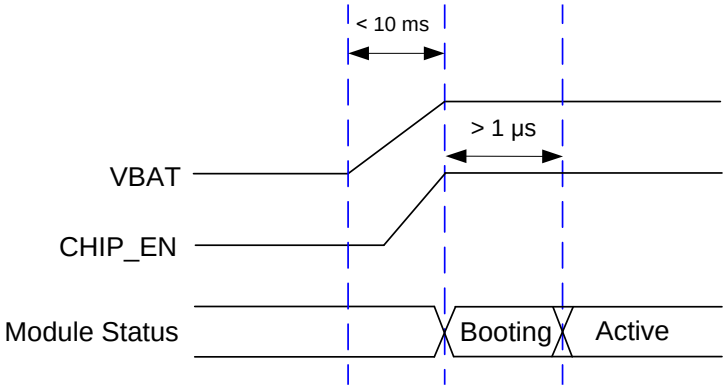


Figure 10: Turn-on Timing

4.3. Reset

Drive RESET_N low for at least 100 ms and then release it to reset the module.

Table 17: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	11	DI	Reset the module	Internally pulled up to VBAT. Active low.

The reference design for resetting the module is shown below. An open collector driving circuit can be used to control the RESET_N pin.

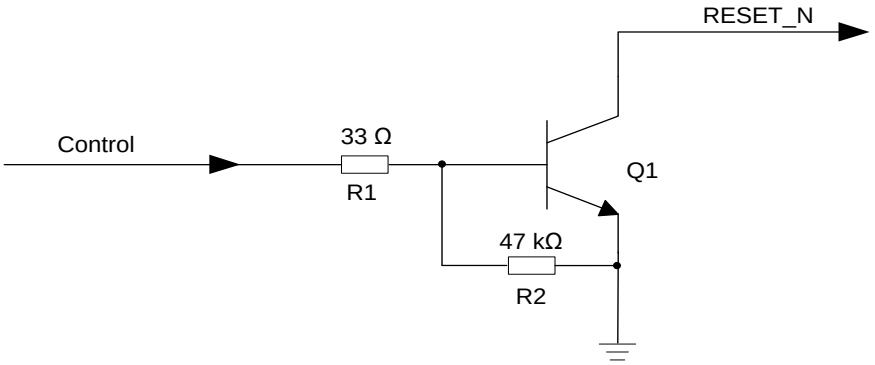


Figure 11: Reference Circuit of RESET_N by Using A Driving Circuit

Another way to control the RESET_N is by using a button directly. A TVS component should be placed near the button for ESD protection.

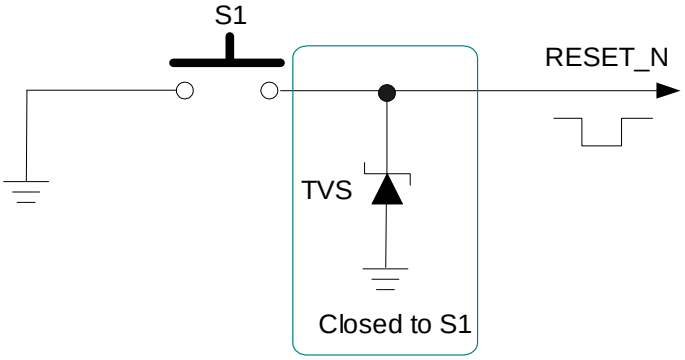


Figure 12: Reference Circuit of RESET_N with A Button

The module reset timing is illustrated in the following figure.

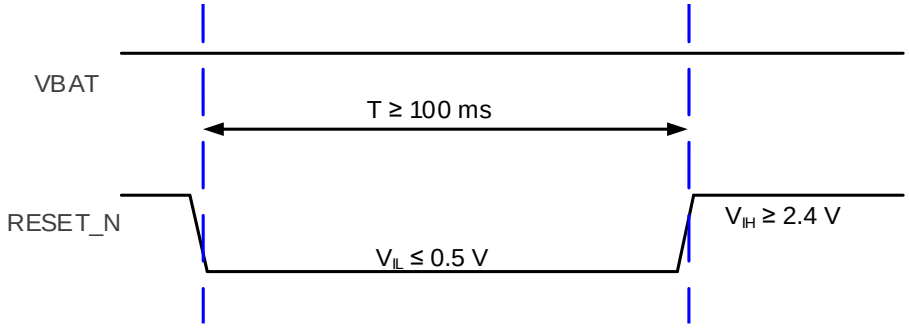


Figure 13: Reset Timing

4.4. Download Mode

Keep RESET_N of the module at low level during resetting or power-up and the module will enter download mode. In the download mode, the firmware can be download through the UART0. During the hardware design, connect the RESET_N of the module to the RTS of the serial port chip, or control RESET_N through the host GPIO according to the waveform in the figure, otherwise the download will fail.

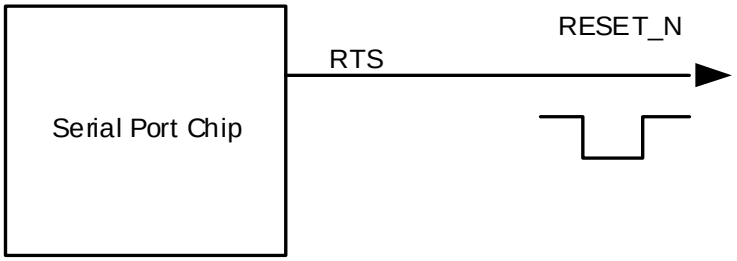


Figure 14: Reference Design for Download Mode

5 RF Performances

5.1. Wi-Fi Performances

Table 18: Wi-Fi Performances

Operating Frequency				
2.4 GHz: 2.400–2.4835 GHz				
Modulation				
BPSK, QPSK, CCK, 16QAM, 64QAM				
Operating Mode				
● AP ● STA				
Encryption Mode				
WPA-PSK, WPA2-PSK, WPA3-SAE, AES-128				
Transmission Data Rate				
● 802.11b: 1 Mbps, 2 Mbps, 5.5 Mbps, 11 Mbps ● 802.11g: 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps ● 802.11n: HT20 (MCS 0–MCS 7), HT40 (MCS 0–MCS 7) ● 802.11ax: HT20 (MCS 0–MCS 7)				
Condition (VBAT = 3.3 V; Temp. 25°C)		**EVM**	**Typ.; Unit: dBm, Tolerance: ±2 dB**	
			Transmitting Power	**Receiving Sensitivity**
2.4 GHz	802.11b @ 1 Mbps	≤ 35 %	17	-92
	802.11b @ 11 Mbps		17	-86
	802.11g @ 6 Mbps	≤ -5 dB	14	-89
	802.11g @ 54 Mbps	≤ -25 dB	14	-73

	802.11n, HT20 @ MCS 0	≤ -5 dB	14	-89
	802.11n, HT20 @ MCS 7	≤ -27 dB	14	-70
	802.11n, HT40 @ MCS 0	≤ -5 dB	13	-87
	802.11n, HT40 @ MCS 7	≤ -27 dB	13	-67
	802.11ax, HT20 @ MCS 0	≤ -5 dB	14	-89
	802.11ax, HT20 @ MCS 7	≤ -27 dB	14	-69

5.2. Bluetooth Performances

Table 19: Bluetooth Performances

Operating Frequency		
2.400–2.4835 GHz		
Modulation		
GFSK		
Operating Mode		
BLE		
Condition (VBAT = 3.3 V; Temp. 25°C)	**Typ.; Unit: dBm, Tolerance: ±2 dB [5]**	
	Transmitting Power	**Receiving Sensitivity**
BLE (1 Mbps)	6	-90
BLE (2 Mbps)	6	-89

[5] The tolerance for Bluetooth receiving sensitivity is ±4 dB in high channel (CH39).

5.3. Antenna/Antenna Interfaces

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module is provided in one of the three antenna/antenna interface designs: pin antenna interface (ANT_WIFI/BT), PCB antenna and RF coaxial connector. The RF coaxial connector is not available when the module is designed with ANT_WIFI/BT antenna interface or PCB antenna.

5.3.1. Pin Antenna Interface (ANT_WIFI/BT) [6]

Table 20: ANT_WIFI/BT Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	2	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω characteristic impedance.

5.3.1.1. Reference Design

The circuit of RF antenna interface is shown below. For better RF performance, it is necessary to reserve a π matching circuit and add ESD protection components. Reserved matching components such as R1, C1, C2, and D1 should be placed as close to the antenna as possible. C1, C2, and D1 are not mounted by default. The parasitic capacitance of TVS should be less than 0.05 pF and R1 is recommended to be 0 Ω.

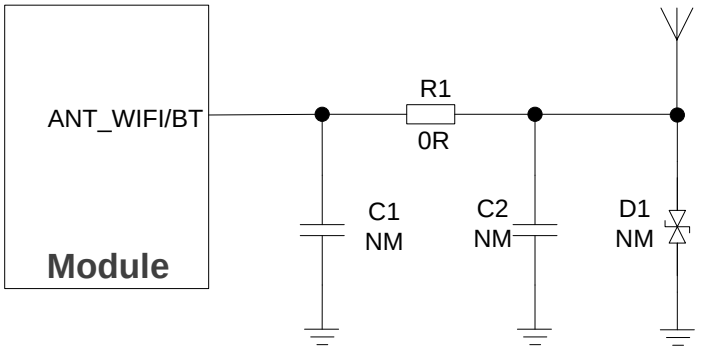


Figure 15: RF Antenna Reference Design

[6] The module is provided with one of the three antenna/antenna interface designs. For more details, please contact Quectel Technical Support.

5.3.1.2. Antenna Design Requirements

Table 21: Antenna Design Requirements

Parameter	Requirement
Frequency Range (GHz)	2.400–2.4835
Cable Insertion Loss (dB)	< 1
VSWR	≤ 2
Gain (dBi)	1 (Typ.)
Max. input power (W)	50
Input impedance (Ω)	50
Polarization type	Vertical

5.3.1.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

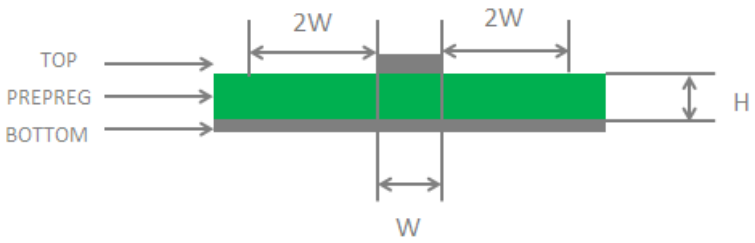


Figure 16: Microstrip Design on a 2-layer PCB

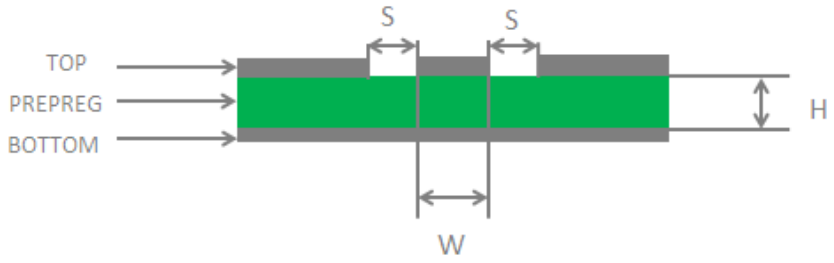


Figure 17: Coplanar Waveguide Design on a 2-layer PCB

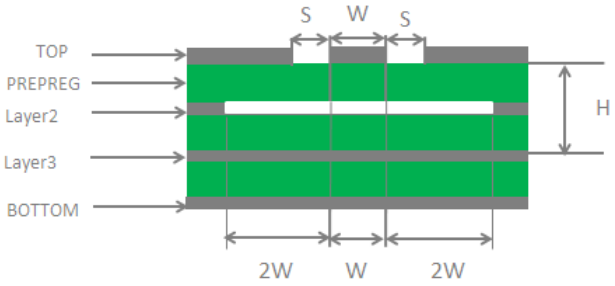


Figure 18: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

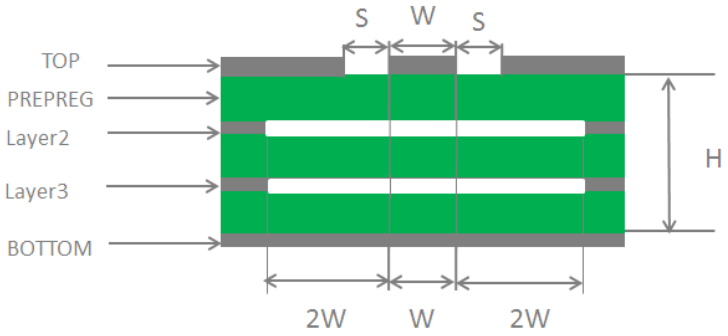


Figure 19: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to control the characteristic impedance of RF traces to 50 Ω.
- GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to the ground.
- The distance between the RF pins and the RF connector should be as short as possible and all right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.

- The reference ground of RF traces should be complete. In addition, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [2]***.

5.3.1.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

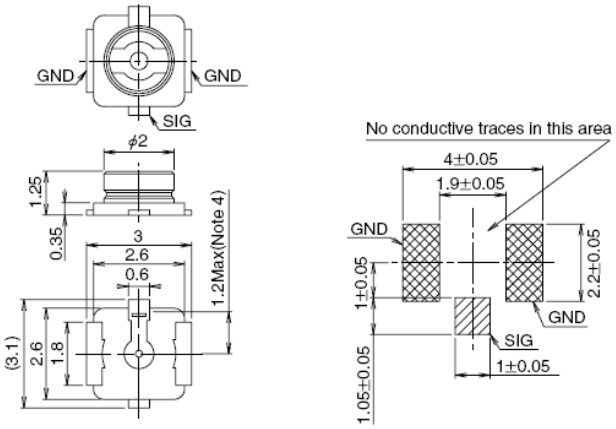


Figure 20: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

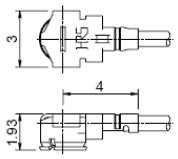
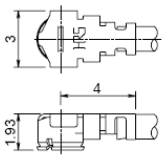
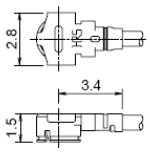
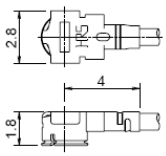
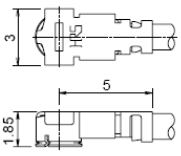
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 21: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

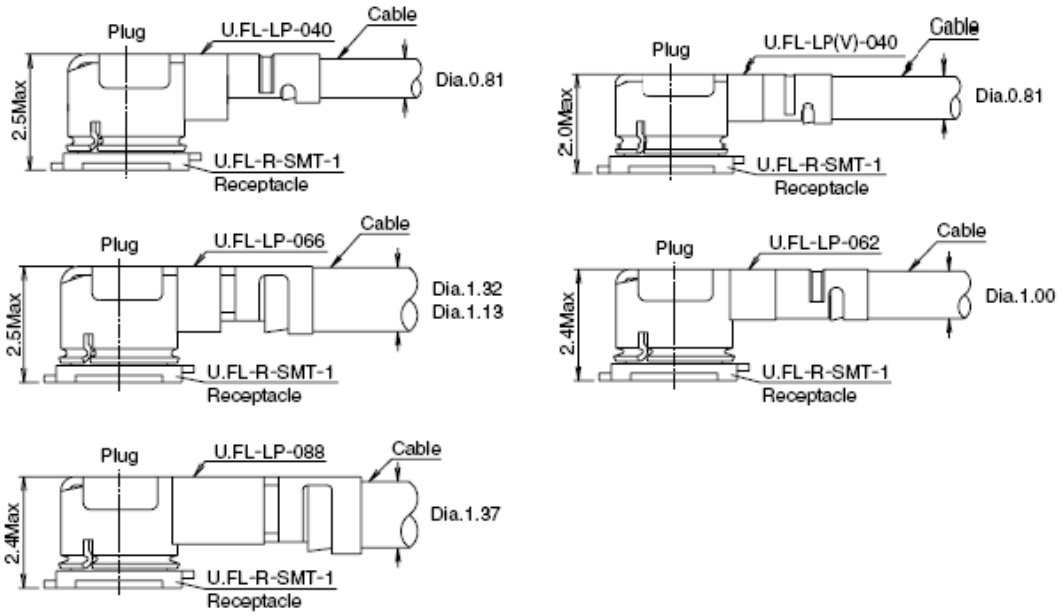


Figure 22: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://www.hirose.com.

5.3.2. PCB Antenna [7]

Table 22: PCB Antenna Specifications

Parameter	Requirement
Frequency Range (GHz)	2.400–2.500
Input Impedance (Ω)	50
VSWR	≤ 3
Gain (dBi)	-0.38 (Typ.)
Efficiency	26 %

When using the PCB antenna on the module, the module should be placed at the side of the motherboard. The distance between the PCB antenna and connectors, vias, traces, ethernet port and any other metal components on the motherboard should be at least 16 mm. All layers in the PCB of the motherboard under the PCB antenna should be designed as a keepout area.

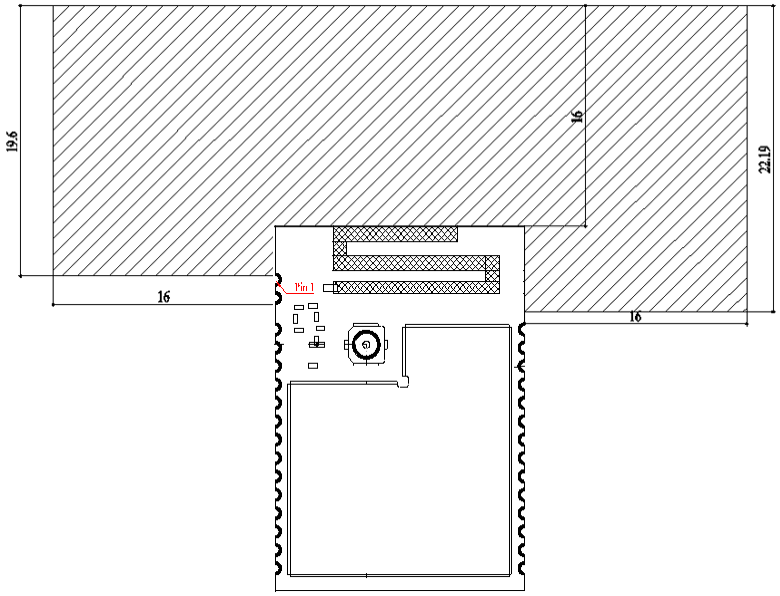


Figure 23: Keepout Area on Motherboard

Do not routing at the RF test point at the bottom of the module to ensure its performances during PCB design.

[7] The module is provided with one of the three antenna/antenna interface designs. For more details, please contact Quectel Technical Support.

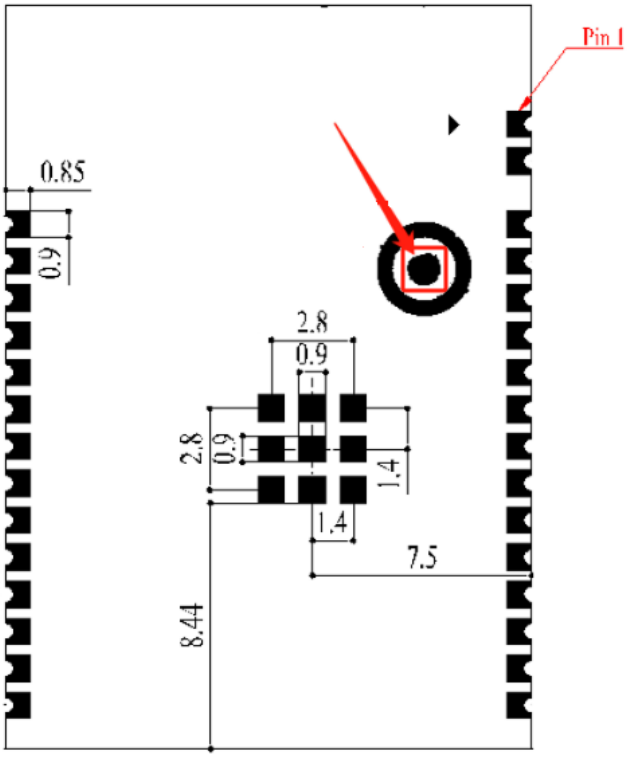


Figure 24: Prohibited Area for Routing

5.3.3. Coaxial RF Connector [8]

5.3.3.1. Receptacle Specifications

The mechanical dimensions of the receptacle supported by the module are as follows.

[8] The module is provided with one of the three antenna/antenna interface designs. For more details, please contact Quectel Technical Support.

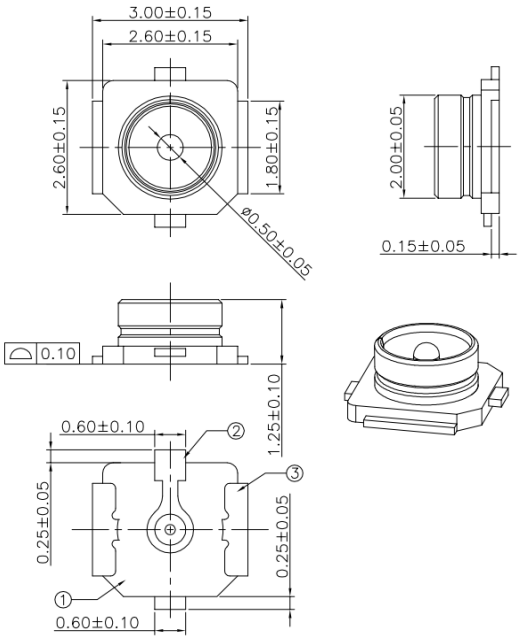


Figure 25: Dimensions of the Receptacle (Unit: mm)

Table 23: Major Specifications of the RF Connector

Item	Specification
Nominal Frequency Range	DC to 6 GHz
Nominal Impedance	50 Ω
Temperature Rating	-40 °C to +85 °C
Voltage Standing Wave Ratio (VSWR)	Meet the requirements of: Max. 1.3 (DC–3 GHz) Max. 1.45 (3–6 GHz)

The mated plug listed in the following figure can be used to match the connector.

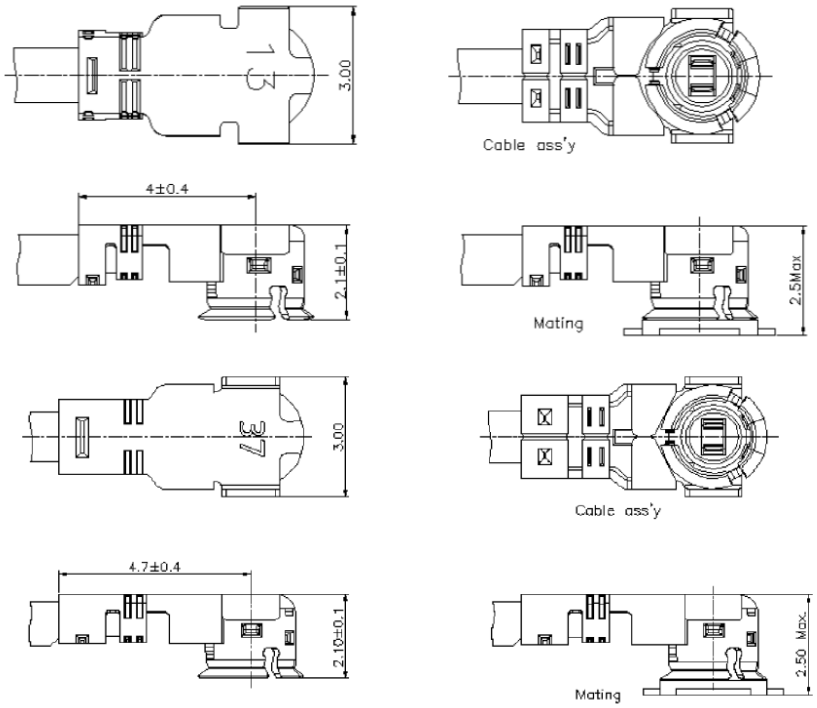


Figure 26: Specifications of Mated Plugs (Unit: mm)

5.3.3.2. Assemble Coaxial Cable Plug Manually

The pictures for plugging in a coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

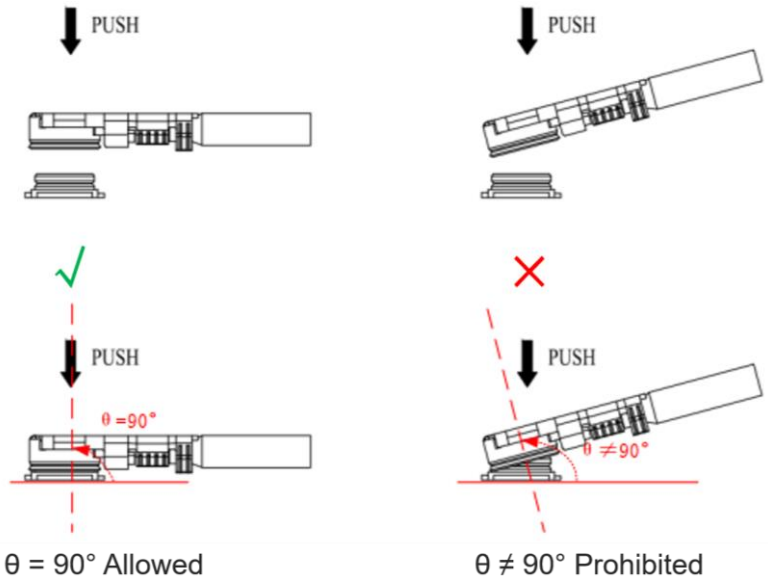


Figure 27: Plug in a Coaxial Cable Plug

The pictures of pulling out the coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

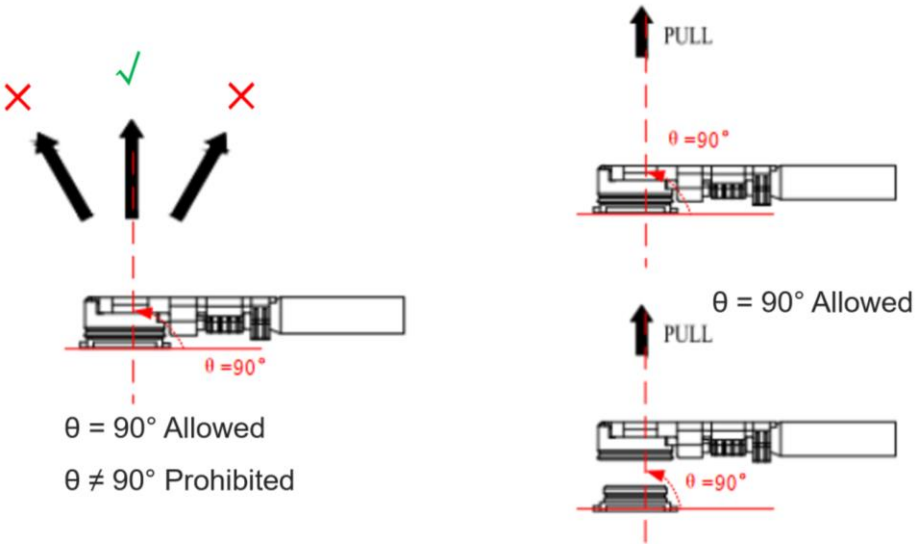


Figure 28: Pull out a Coaxial Cable Plug

5.3.3.3. Assemble Coaxial Cable Plug with Jig

The pictures of installing the coaxial cable plug with a jig is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

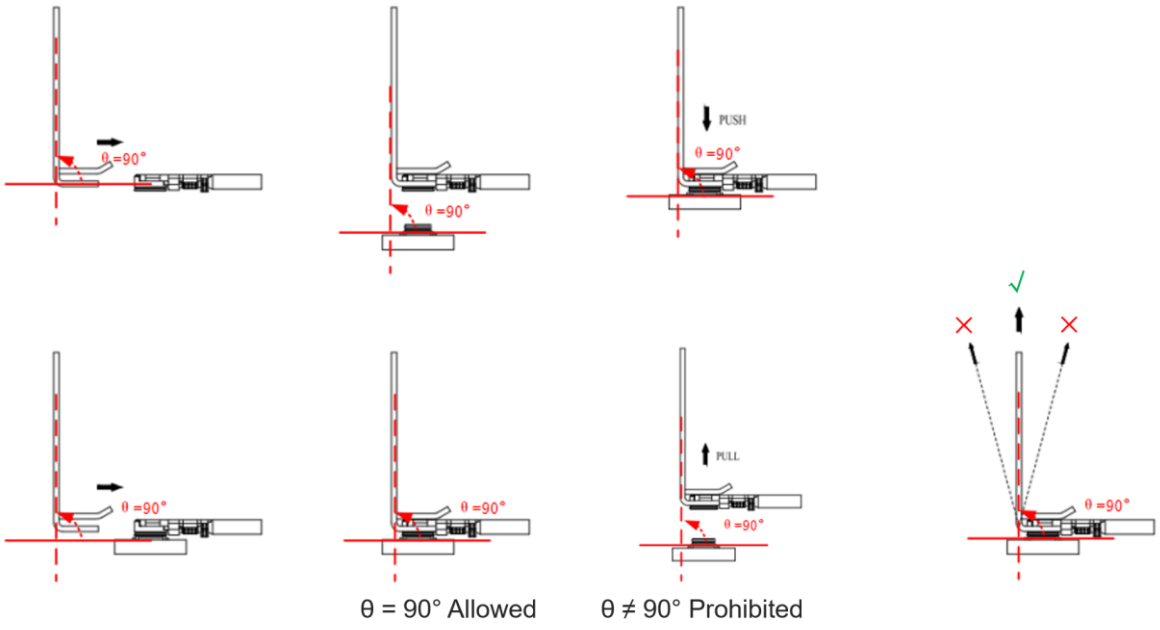


Figure 29: Install the Coaxial Cable Plug with Jig

5.3.3.4. Recommended Manufacturers of RF Connector and Cable

RF connectors and cables by I-PEX are recommended. For more details, visit https://www.i-pex.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 24: Absolute Maximum Ratings (Unit: V)

Parameter	Min.	Max.
VBAT	-0.3	3.6
Voltage at Digital Pins	-0.3	3.6
Voltage at ADC[0:2]	0	3.3

6.2. Power Supply Ratings

Table 25: Module Power Supply Ratings (Unit: V)

Parameter	Description	Condition	Min.	Typ.	Max.
VBAT	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	3.0	3.3	3.6

6.3. Power Consumption

Table 26: Power Consumption in Non-signaling Mode (Unit: mA)

Condition			I_{VBAT} (Typ.)
2.4 GHz	802.11b	Tx 1Mbps @ 17 dBm	285
		Tx 11 Mbps @ 17 dBm	277
	802.11g	Tx 6 Mbps @ 14 dBm	182
		Tx 54 Mbps @ 14 dBm	167
	802.11n	Tx HT20 MCS 0 @ 14 dBm	184
		Tx HT20 MCS 7 @ 14 dBm	179
	802.11n	Tx HT40 MCS 0 @ 13 dBm	183
		Tx HT40 MCS 7 @ 13 dBm	172
	802.11ax	Tx HT20 MCS 0 @ 14 dBm	184
		Tx HT20 MCS 7 @ 14 dBm	180

6.4. Digital I/O Characteristics

Table 27: VBAT I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.7 × VBAT	VBAT
V_{IL}	Low-level input voltage	0	0.3 × VBAT
V_{OH}	High-level output voltage	0.9 × VBAT	-
V_{OL}	Low-level output voltage	-	0.1 × VBAT

6.5. ESD Protection

Static electricity occurs naturally and may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 28: ESD Characteristics (Unit: kV)

Model	Test Result	Standard
Human Body Model (HBM)	±4	*ANSI/ESDA/JEDEC JS-001-2017*
Charged Device Model (CDM)	±0.5	*ANSI/ESDA/JEDEC JS-002-2018*

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeters (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

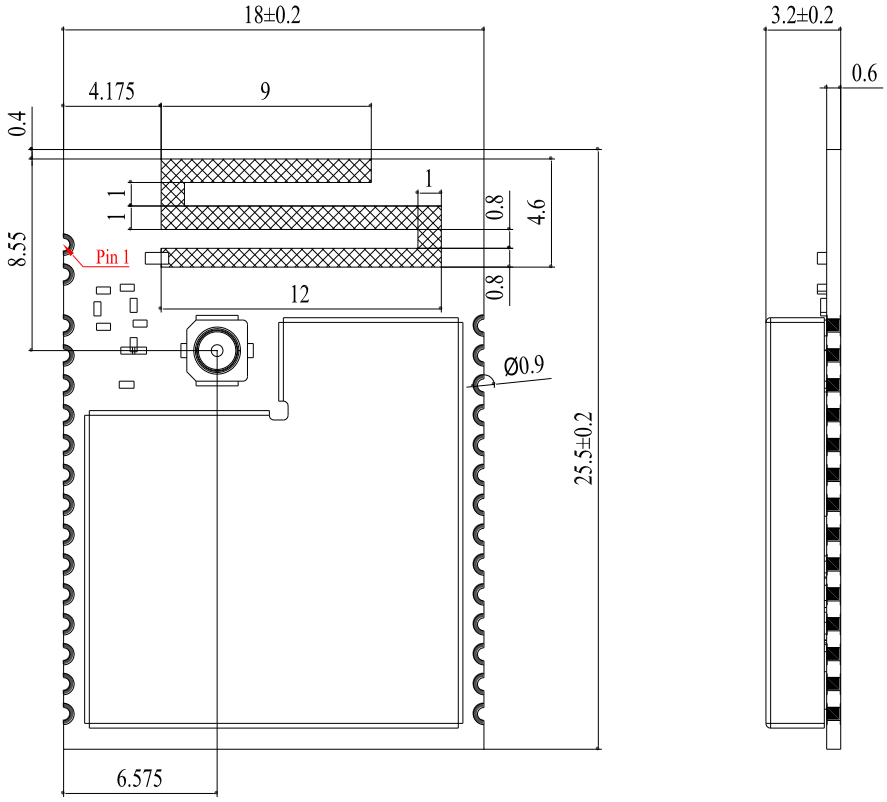


Figure 30: Top and Side Dimensions

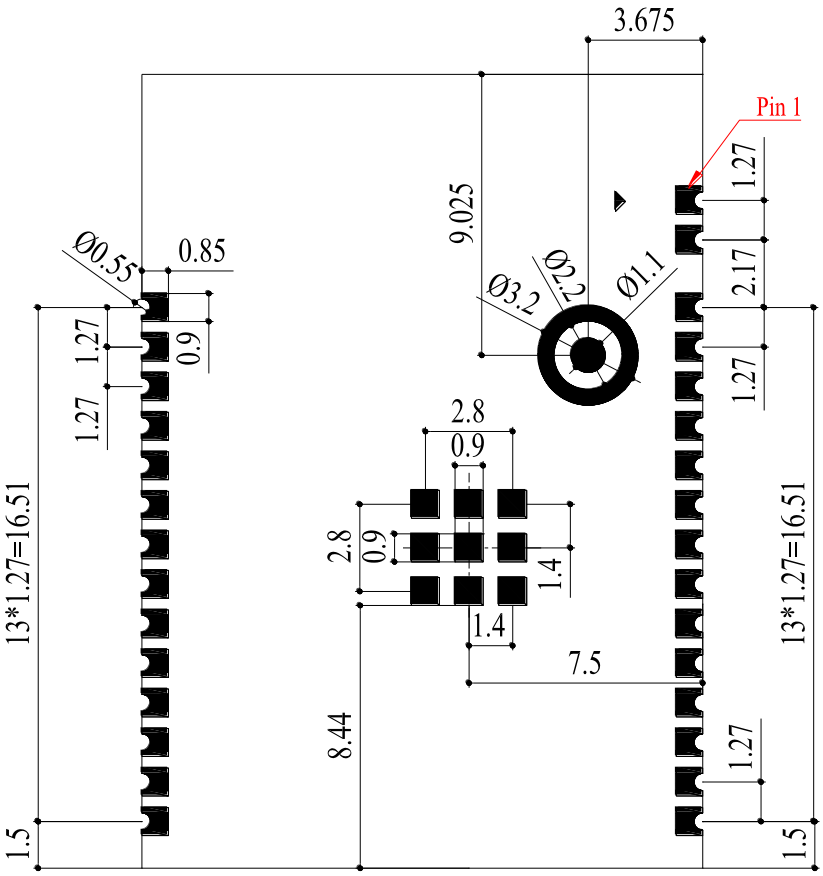


Figure 31: Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module refers to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

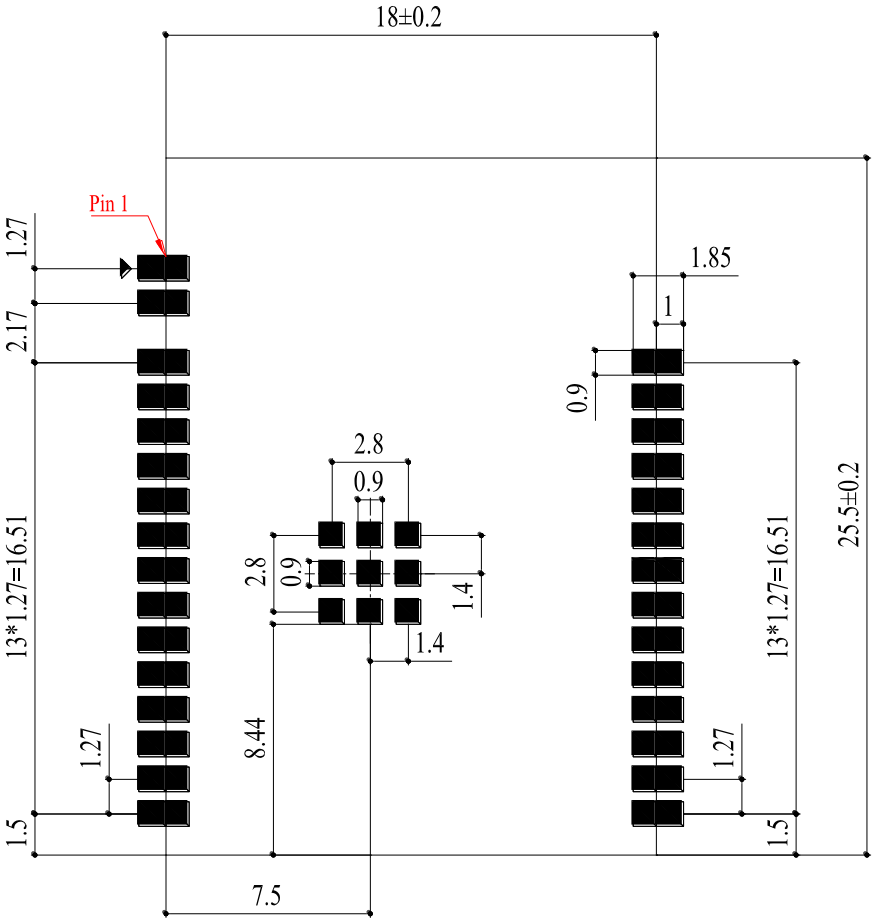


Figure 32: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

Figure 33: Top and Bottom Views (Pin Antenna Interface)

Figure 34: Top and Bottom Views (PCB Antenna)

Figure 35: Top and Bottom Views (RF Coaxial Connector)

NOTE

1. Images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.
2. The RF coaxial connector is not mounted on the module when using pin antenna interface (ANT_WIFI/BT) or PCB antenna.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [9] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[9] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [3]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

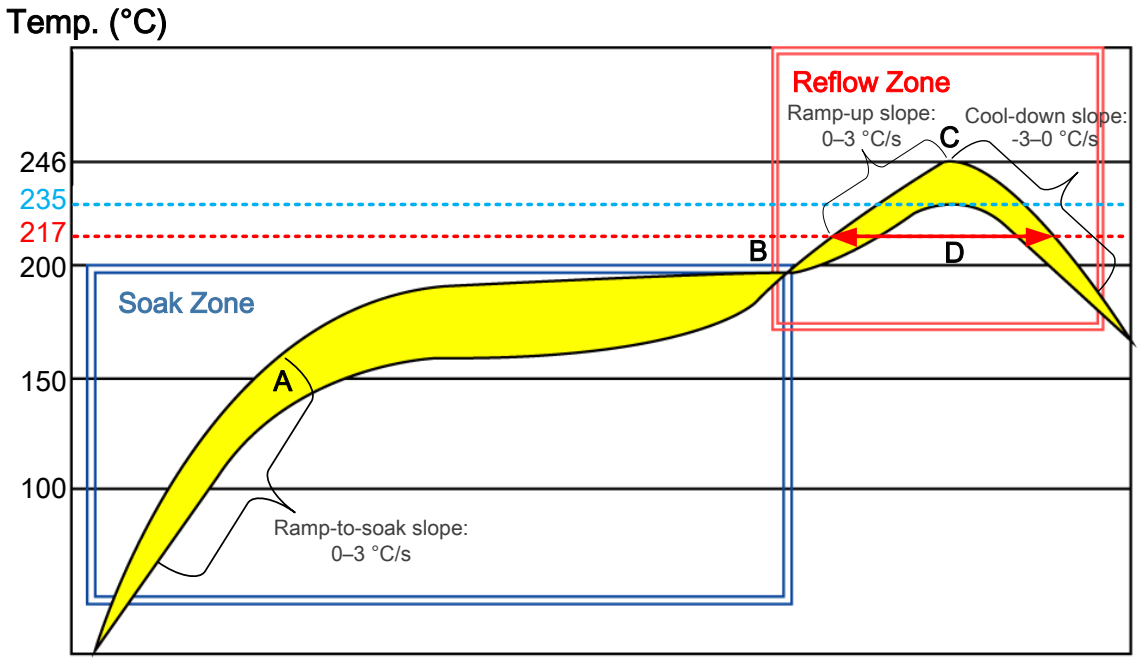


Figure 36: Recommended Reflow Soldering Thermal Profile

Table 29: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [3]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Carrier tape dimensions are detailed below:

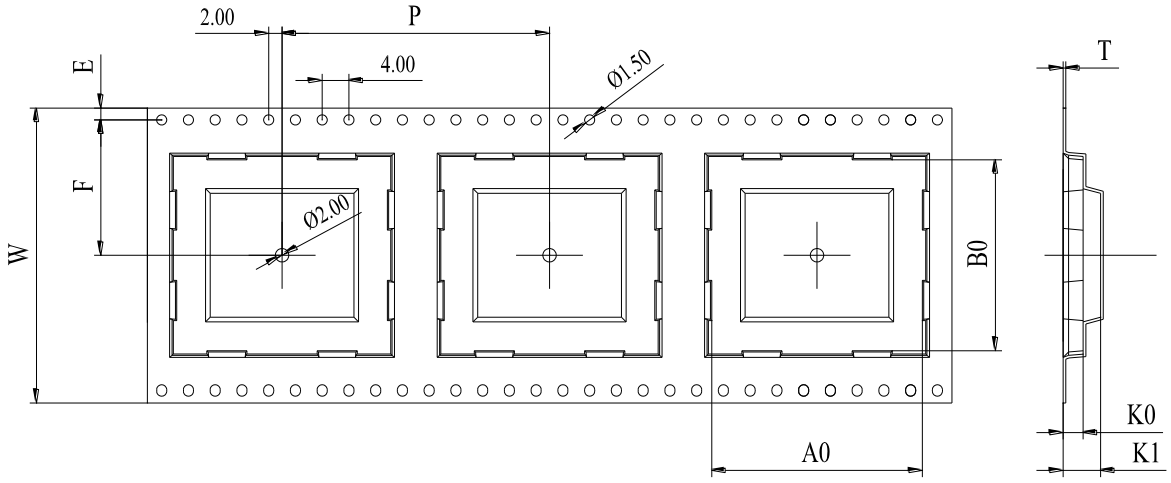


Figure 37: Tape Specifications

Table 30: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.4	18.4	25.9	3.7	6.8	20.2	1.75

8.3.2. Plastic Reel

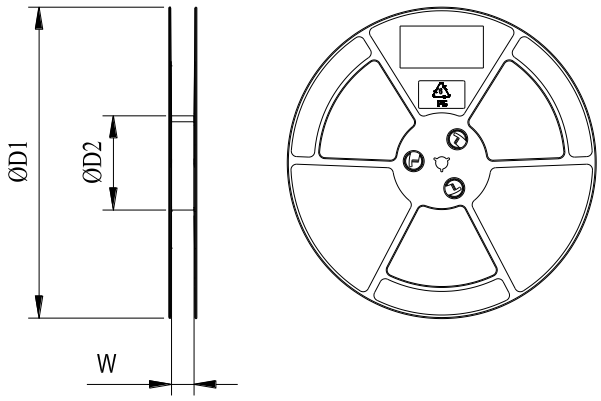


Figure 38: Plastic Reel Dimension Drawing

Table 31: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

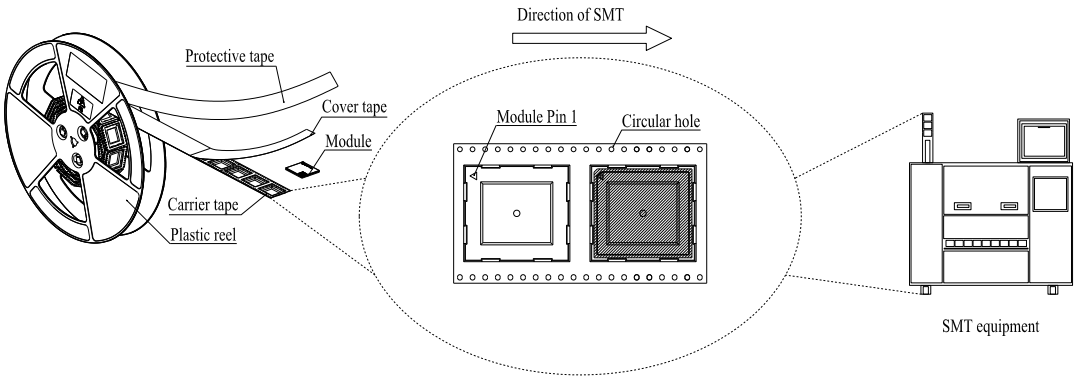
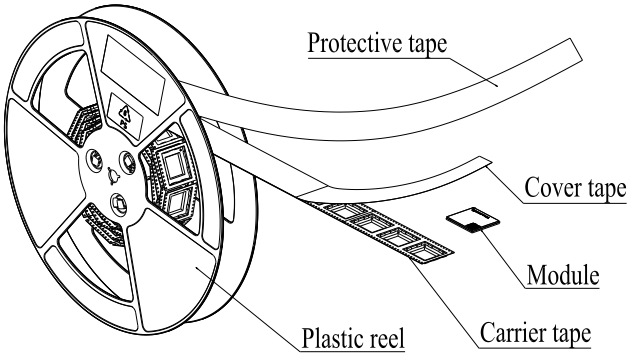


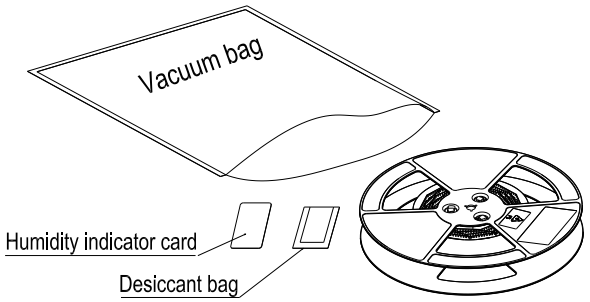
Figure 39: Mounting Direction

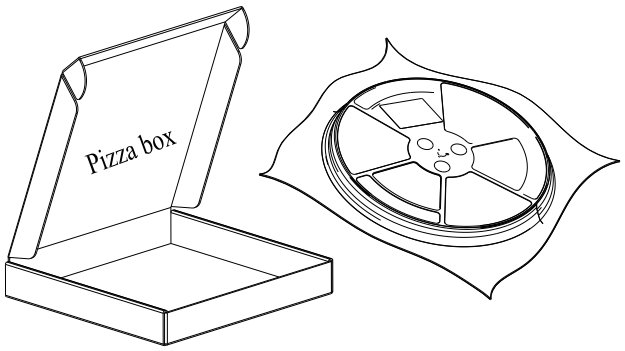
8.3.4. Packaging Process



Place the modules into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape on the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel inside the pizza box.

Place 4 packaged pizza boxes inside 1 carton box and seal it. 1 carton box can pack 1000 modules.

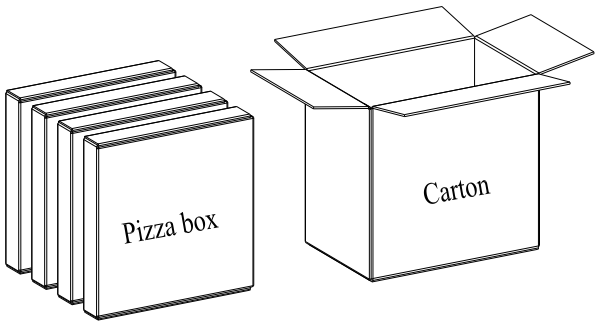


Figure 40: Packaging Process

9 Appendix References

Table 32: Related Documents

Document Name
[1] Quectel_FCM360W_TE-B_User_Guide
[2] Quectel_RF_Layout_Application_Note
[3] Quectel_Module_SMT_Application_Note

Table 33: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AMBA	Advanced Microcontroller Bus Architecture
AP	Access Point
APB	Advanced Peripheral Bus
BLE	Bluetooth Low Energy
BPSK	Binary Phase Shift Keying
CCK	Complementary Code Keying
CDM	Charged Device Model
CS	Chip Select
DAC	Digital-to-Analog Converter
DC	Direct Current
DMA	Direct Memory Access

DSP	Digital Signal Processor
ESD	Electrostatic Discharge
EVM	Error Vector Magnitude
GFSK	Gauss frequency Shift Keying
GND	Ground
GPIO	General-Purpose Input/Output
HT	High Throughput
I/O	Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
IEEE	Institute of Electrical and Electronics Engineers
LNA	Low Noise Amplifier
LCC	Leadless Chip Carrier (package)
MCS	Modulation and Coding Scheme
Mbps	Million Bits Per Second
MISO	Master In Slave Out
MMC	MultiMedia Card
MOSI	Master Out Slave In
OTA	Over-the-Air
PA	Power Amplifier
PCB	Printed Circuit Board
PMU	Power Management Unit
PSK	Pre-Shared Key
PWM	Pulse Width Modulation
QAM	Quadrature Amplitude Modulation

QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RISC	Reduced Instruction-Set Computer
RoHS	Restriction of Hazardous Substances
ROM	Read Only Memory
SAE	Simultaneous Authentication of Equals
SMT	Surface Mount Technology
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
STA	Station
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
(U)SIM	(Universal) Subscriber Identity Module
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WPA	Wi-Fi Protected Access
XO	Crystal Oscillator