EG915U Series QuecOpen Reference Design

LTE Standard Module Series

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About the Document

Revision History

Version	Date	Author	Description
-	2022-06-30	Len CHEN	Creation of the document
1.0	2023-09-26	Phoebe FU/ Woping WANG	First official release

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EG915U series module in QuecOpen® solution, including block diagrams of module design, power supply, antenna, (U)SIM, analog audio, UART, camera, LCM, external flash and SD card interfaces.

1.2. Special Mark

Table 1: Special Mark

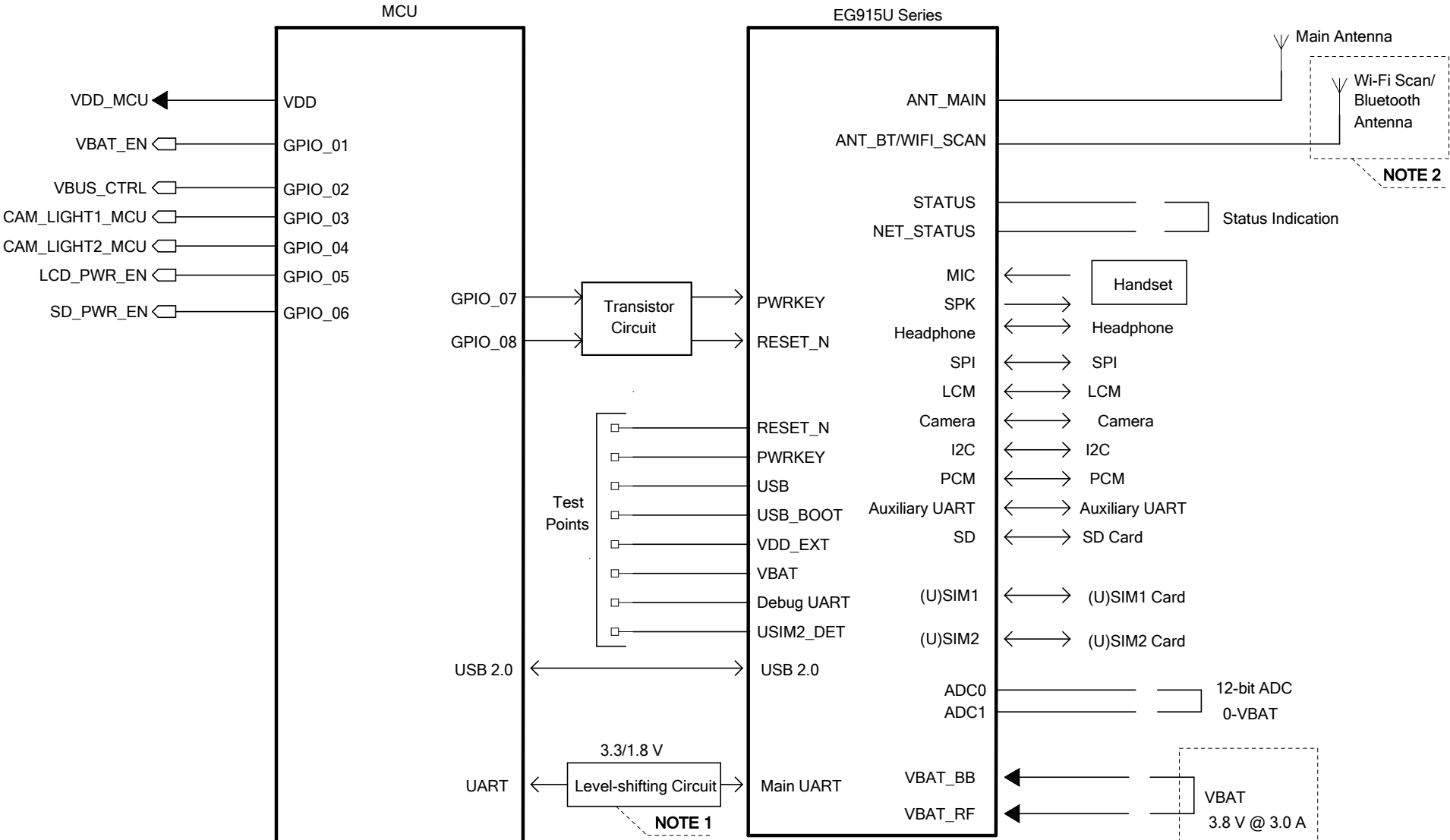| Mark	Definition
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO_DATA pins, SDIO_DATA0, SDIO_DATA1, SDIO_DATA2 and SDIO_DATA3.

1.3. Schematics

The schematics illustrated in the following pages are provided for your reference only.

NOTE

It is required to confirm the applicability and price from the supplier about the IC involved in the reference design.

Block Diagram

MCU
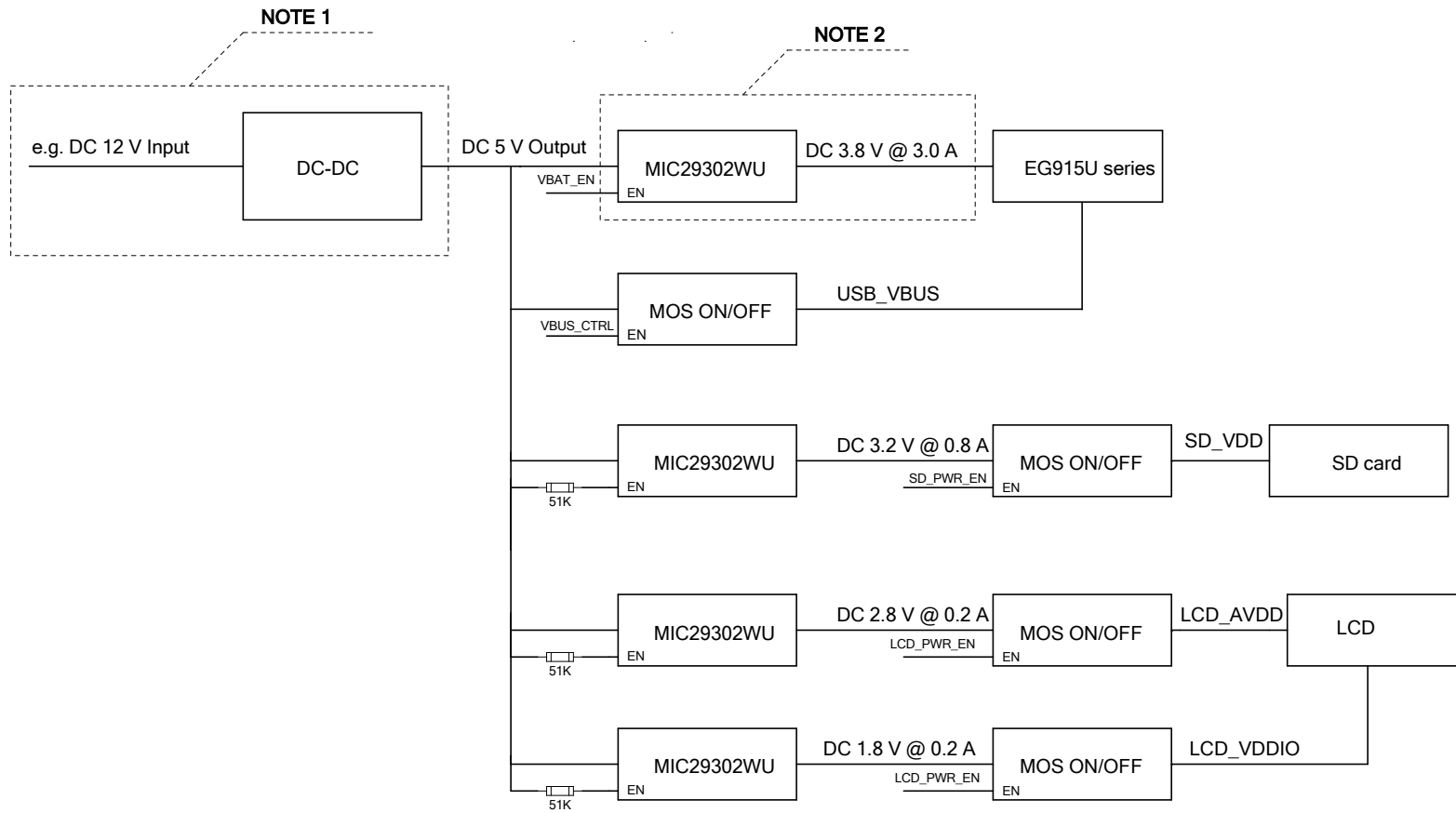
EG915U Series

VDD_MCU ← VDD

ANT_MAIN → Main Antenna

ANT_BT/WIFI_SCAN → Wi-Fi Scan/ Bluetooth Antenna

NOTE 2

VBAT_EN — GPIO_01

VBUS_CTRL — GPIO_02

CAM_LIGHT1_MCU — GPIO_03

CAM_LIGHT2_MCU — GPIO_04

LCD_PWR_EN — GPIO_05

SD_PWR_EN — GPIO_06

STATUS → Status Indication
NET_STATUS →

MIC ← Handset
SPK →

GPIO_07 → Transistor Circuit → PWRKEY

GPIO_08 → RESET_N

Headphone ←→ Headphone

SPI ←→ SPI

LCM ←→ LCM

Camera ←→ Camera

I2C ←→ I2C

PCM ←→ PCM

Test Points

RESET_N
PWRKEY
USB
USB_BOOT
VDD_EXT
VBAT
Debug UART
USIM2_DET

Auxiliary UART ←→ Auxiliary UART

SD ←→ SD Card

(U)SIM1 ←→ (U)SIM1 Card

(U)SIM2 ←→ (U)SIM2 Card

USB 2.0 ←→ USB 2.0

ADC0 — 12-bit ADC
ADC1 — 0-VBAT

3.3/1.8 V

UART ←→ Level-shifting Circuit ←→ Main UART

VBAT_BB ← VBAT 3.8 V @ 3.0 A
VBAT_RF ←

NOTE 1

NOTE 3

NOTE:

1. A transistor circuit or a voltage-level translator TXS0104EPWR provided by Texas Instruments is recommended.
2. The module supports both Wi-Fi Scan and Bluetooth functions. However, as the antenna interface is shared, the two functions cannot be used simultaneously. For details about specific models, contact Quectel Technical Support.
3. The power supply should be able to provide sufficient current of at least 3.0 A for the module.

Power System Block Diagram

e.g. DC 12 V Input — **DC-DC** — DC 5 V Output

NOTE 1

NOTE 2

MIC29302WU — DC 3.8 V @ 3.0 A — EG915U series
VBAT_EN / EN

MOS ON/OFF — USB_VBUS
VBUS_CTRL / EN

MIC29302WU — DC 3.2 V @ 0.8 A — MOS ON/OFF — SD_VDD — SD card
EN / 51K / SD_PWR_EN / EN

MIC29302WU — DC 2.8 V @ 0.2 A — MOS ON/OFF — LCD_AVDD — LCD
EN / 51K / LCD_PWR_EN / EN

MIC29302WU — DC 1.8 V @ 0.2 A — MOS ON/OFF — LCD_VDDIO
EN / 51K / LCD_PWR_EN / EN

NOTE:

1. When the input voltage is above 7.0 V, use a DC-DC converter to convert a high input voltage into 5.0 V.

2. The LDO is used to convert the input voltage into 3.8 V typical voltage and the power supply should provide at least 3 A current for the module.
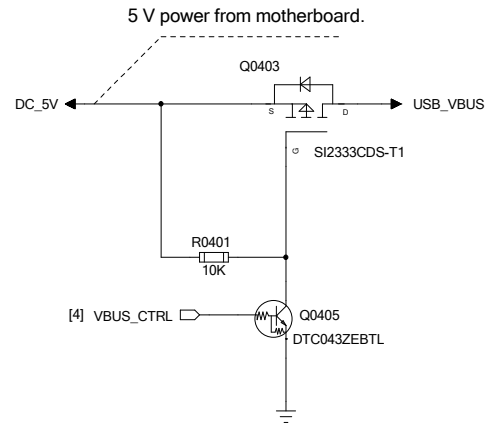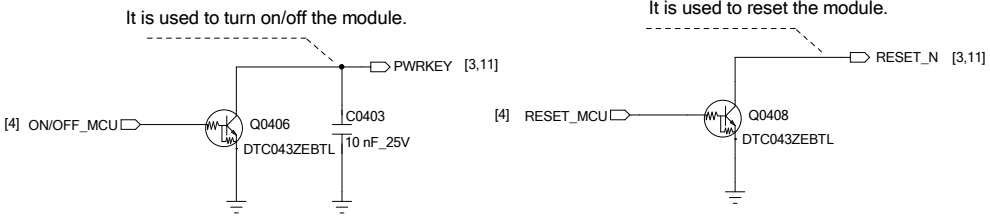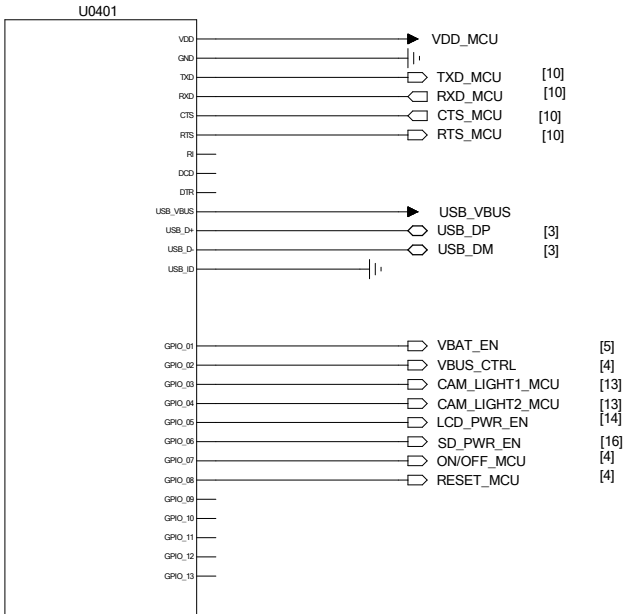
Module Interfaces
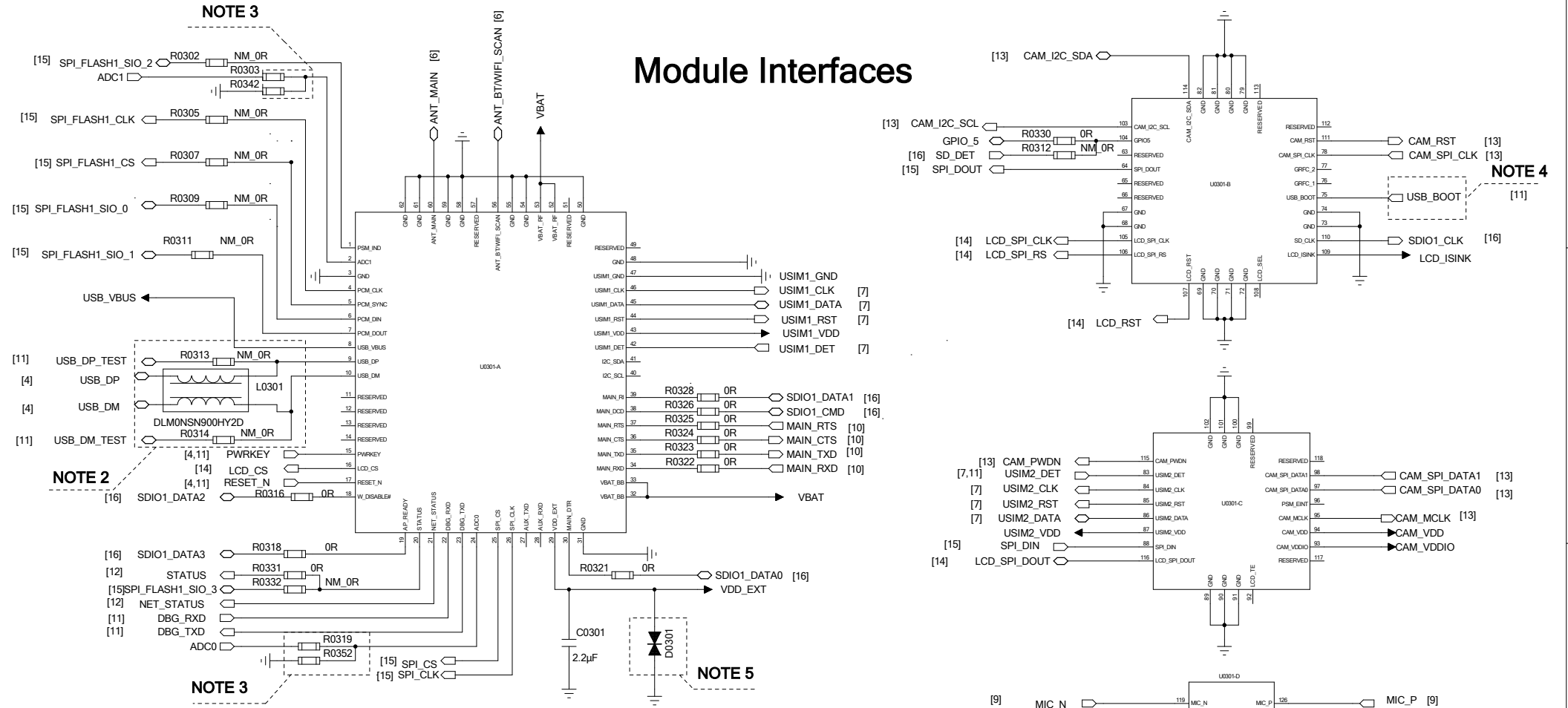
NOTE:

1. Keep unused and RESERVED pins open, and all GND pins are connected to the ground.

2. A common mode choke L0301 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission.

   Meanwhile, reserve test points for upgrading the firmware and debugging software over USB interface and minimize the extra stubs of the trace.

   L0301 and the two resistors R0313 and R0314 should be placed close to the module to ensure the integrity of USB signal.

3. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins,

   it is strongly recommended to reserve the voltage divider circuit for better compatibility with other Quectel modules.

   The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced.

   When the divider circuit is not used, the ADC pins require 1 kΩ resistor in series.

4. When emergency download function is not required, USB_BOOT cannot be pulled up before the module starts up.

5. The maximum reverse working voltage of the ESD protection components on VDD_EXT traces should not exceed 5 V.

6. Test points must be reserved for DBG_TXD, DBG_RXD, USB_DP, USB_DM, USB_VBUS and USIM2_DET.

   It is recommended to reserve test points for USB_BOOT, VDD_EXT, VBAT and PWRKEY.

   It is recommended to reserve a test point for RESET_N if it is unused.

MCU Interfaces

It is used to turn on/off the module.

PWRKEY [3,11]

[4] ON/OFF_MCU   Q0406   C0403

DTC043ZEBTL   10 nF_25V

It is used to reset the module.

RESET_N [3,11]

[4] RESET_MCU   Q0408

DTC043ZEBTL

U0401

VDD	VDD_MCU
GND	
TXD	TXD_MCU [10]
RXD	RXD_MCU [10]
CTS	CTS_MCU [10]
RTS	RTS_MCU [10]
RI	
DCD	
DTR	
USB_VBUS	USB_VBUS
USB_D+	USB_DP [3]
USB_D-	USB_DM [3]
USB_ID	
GPIO_01	VBAT_EN [5]
GPIO_02	VBUS_CTRL [4]
GPIO_03	CAM_LIGHT1_MCU [13]
GPIO_04	CAM_LIGHT2_MCU [13]
GPIO_05	LCD_PWR_EN [14]
GPIO_06	SD_PWR_EN [16]
GPIO_07	ON/OFF_MCU [4]
GPIO_08	RESET_MCU [4]
GPIO_09	
GPIO_10	
GPIO_11	
GPIO_12	
GPIO_13	

5 V power from motherboard.

Q0403

DC_5V   S   D   USB_VBUS

SI2333CDS-T1

R0401
10K

[4] VBUS_CTRL   Q0405

DTC043ZEBTL

NOTE:

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V;
   if the GPIO interfaces of U0401 share the same power domain, then the related level-shifting circuit is not required.
2. The USB 2.0 interface of the module only serves as a slave device and supports high-speed and full-speed modes.
   To communicate with the USB interface, MCU needs to support USB host mode or OTG function. The USB_VBUS of the module
   and MCU should be powered by an external power system, and USB_VBUS is for USB detection. VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the default low-level GPIO pins of MCU as the control pins for PWRKEY and RESET_N of the module.
   Ensure that the maximum load capacitance of PWRKEY and RESET_N does not exceed 10 nF.

Power Supply Design

LDO Application

When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.

U0501
MIC29302WU

DC_5V
C0509
470 µF_16V
C0510
100 nF_16V
R0504
51K
IN (2)
EN (1)
GND (3)
ADJ (5)
OUT (4)
R0505
100K
1%
R0506
47K
1%
C0511
470 µF_16V
C0512
100 nF_16V
R0503
330R
VBAT

NOTE

[4] VBAT_EN
Q0501
DTC043ZEBTL
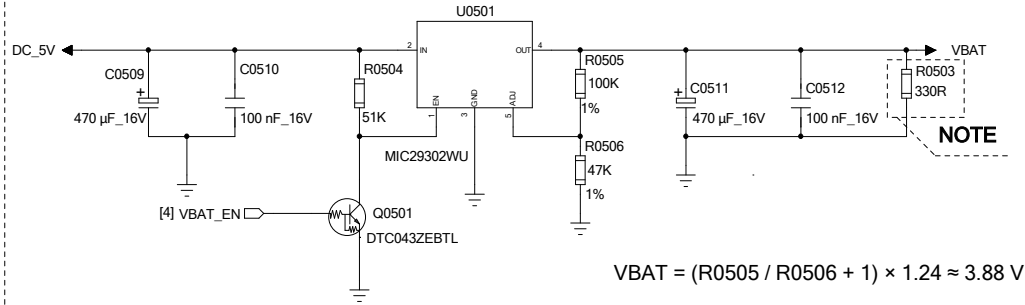
$VBAT = (R0505 / R0506 + 1) \times 1.24 \approx 3.88\ V$

NOTE: The recommended load current is greater than 10 mA.

VBAT Design

VBAT

D0501

Trace width above 2 mm — Connect VBAT_BB pins — VBAT

Trace width above 2.5 mm — Connect VBAT_RF pins — VBAT

C0501
100 µF_10V
C0502
100 nF_16V
C0503
33 pF_50V
C0504
10 pF_50V
C0505
100 µF_10V
C0506
100 nF_16V
C0507
33 pF_50V
C0508
10 pF_50V

Close to VBAT_BB pins   Close to VBAT_RF pins
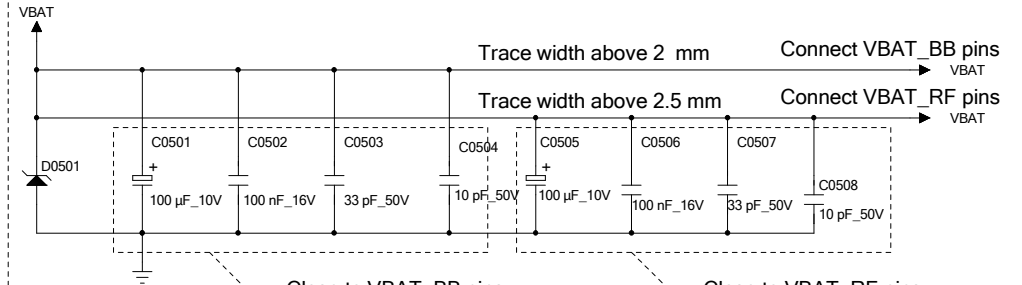
NOTE:
1. For more information about power supply of module,
   see the hardware design document of the module.
2. The VBAT traces must be connected to pins VBAT_BB and VBAT_RF in a star configuration.
3. The recommended operating voltage of VBAT is 3.3 V–4.3 V, and the typical value is 3.8 V.
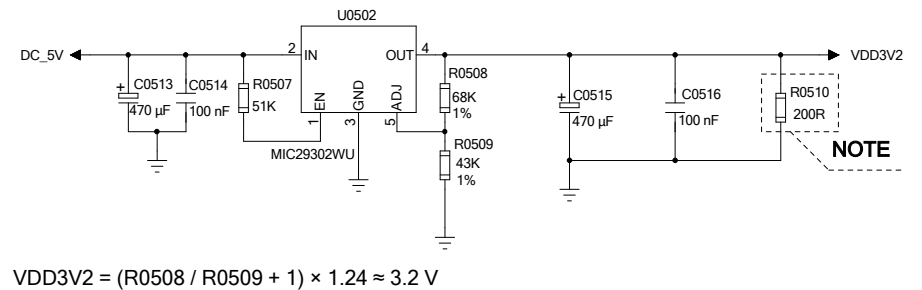
LCD Power Supply

U0503
MIC29302WU

DC_5V
C0530
470 µF
C0531
100 nF
R0532
51K
IN (2)
EN (1)
GND (3)
ADJ (5)
OUT (4)
R0515
43K
1%
R0516
33K
1%
C0523
470 µF
C0524
100 nF
R0018
200R
VDD3V
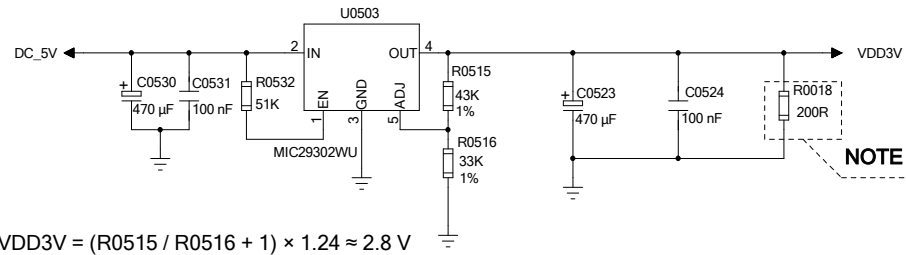
NOTE

$VDD3V = (R0515 / R0516 + 1) \times 1.24 \approx 2.8\ V$

U0504
MIC29302WU

DC_5V
C0525
470 µF
C0526
100 nF
R0519
51K
IN (2)
EN (1)
GND (3)
ADJ (5)
OUT (4)
R0520
15K
1%
R0521
33K
1%
C0527
470 µF
C0528
100 nF
R0522
100R
VDD1V8
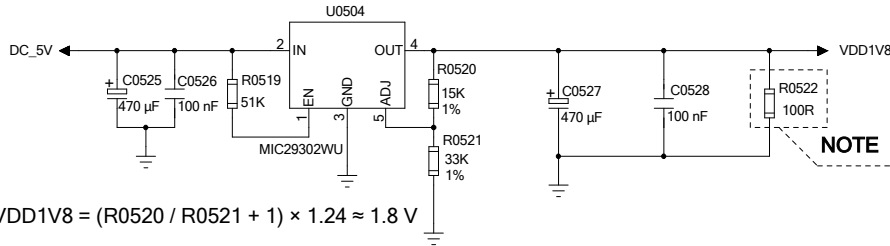
NOTE

$VDD1V8 = (R0520 / R0521 + 1) \times 1.24 \approx 1.8\ V$

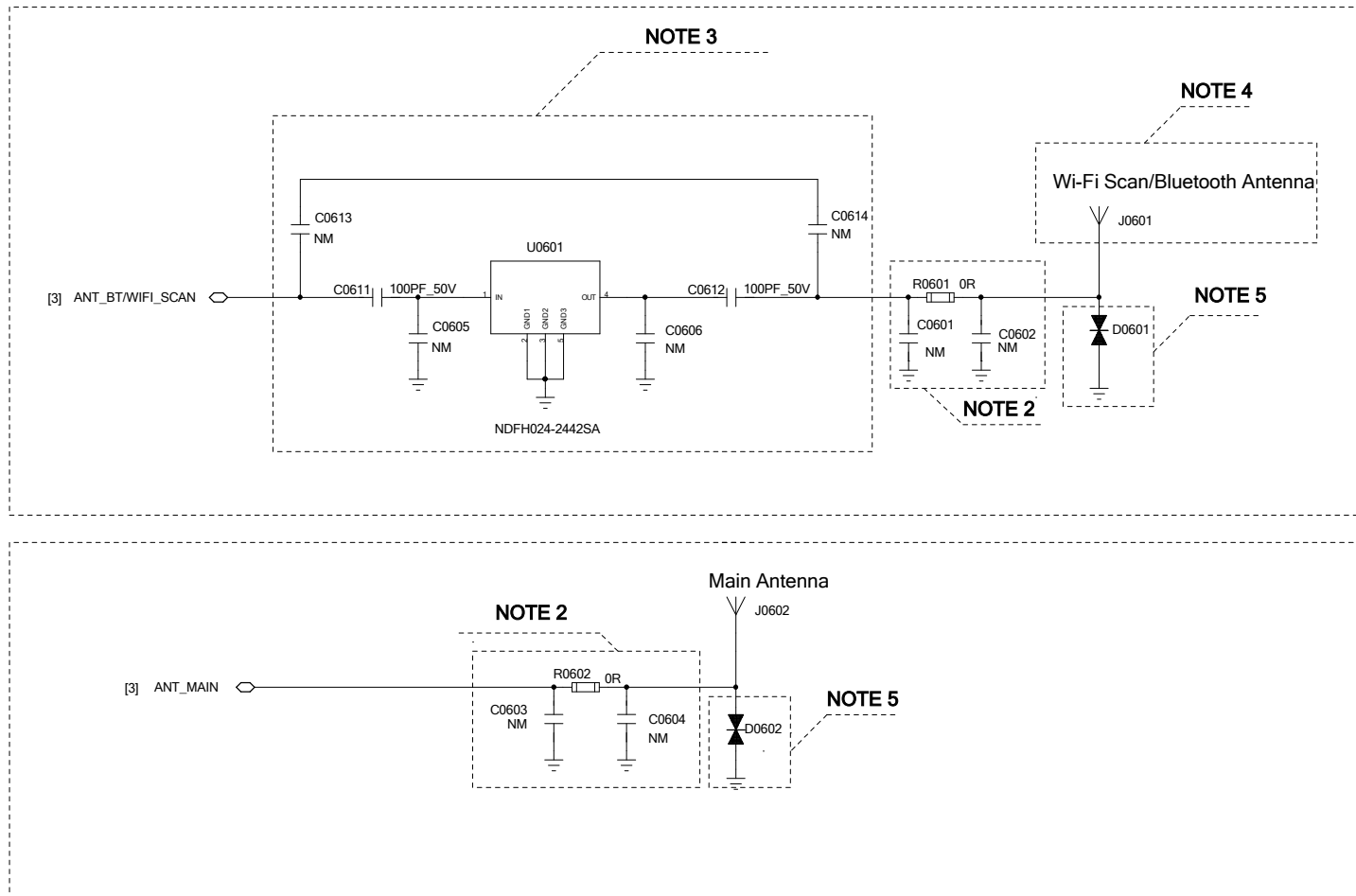**NOTE:** The recommended load current is greater than 10 mA.

SD Card Power Supply

U0502
MIC29302WU

DC_5V
C0513
470 µF
C0514
100 nF
R0507
51K
IN (2)
EN (1)
GND (3)
ADJ (5)
OUT (4)
R0508
68K
1%
R0509
43K
1%
C0515
470 µF
C0516
100 nF
R0510
200R
VDD3V2

NOTE

$VDD3V2 = (R0508 / R0509 + 1) \times 1.24 \approx 3.2\ V$

NOTE: The recommended load current is greater than 10 mA.

Antenna Interface Design

NOTE 3

NOTE 4

Wi-Fi Scan/Bluetooth Antenna

J0601

[3] ANT_BT/WIFI_SCAN

C0613
NM

C0614
NM

U0601

C0611 100PF_50V IN OUT C0612 100PF_50V

C0605
NM

GND1 GND2 GND3

C0606
NM

NDFH024-2442SA

R0601 0R

C0601
NM

C0602
NM

NOTE 5

D0601

NOTE 2

Main Antenna

J0602

NOTE 2

[3] ANT_MAIN

R0602 0R

C0603
NM

C0604
NM

NOTE 5

D0602

NOTE:

1. The single-ended impedance of the RF antenna is 50 Ω.

2. It is highly recommended to reserve a Π-type matching circuit for future debugging.

3. For EG915U-CN, you can select C0613 and C0614 in the compatible design, and C0605, C0606, C0611, C0612, U0601 are not mounted by default.
   For EG915U-EU/-LA, you can select C0605, C0606, C0611, C0612 and U0601 in the compatible design, and C0613 and C0614 are not mounted by default.

4. The module supports both Wi-Fi Scan and Bluetooth functions. However, as the antenna interface is shared, the two functions cannot be used simultaneously.
   Additionally, Bluetooth and Wi-Fi Scan functions are optional. For details, contact Quectel Technical Support.

5. It is recommended that the junction capacitance and peak reverse working voltage of the ESD protection components
   should not exceed 0.05 pF and 5 V respectively.

(U)SIM Interface Design

(U)SIM 1

(U)SIM 2
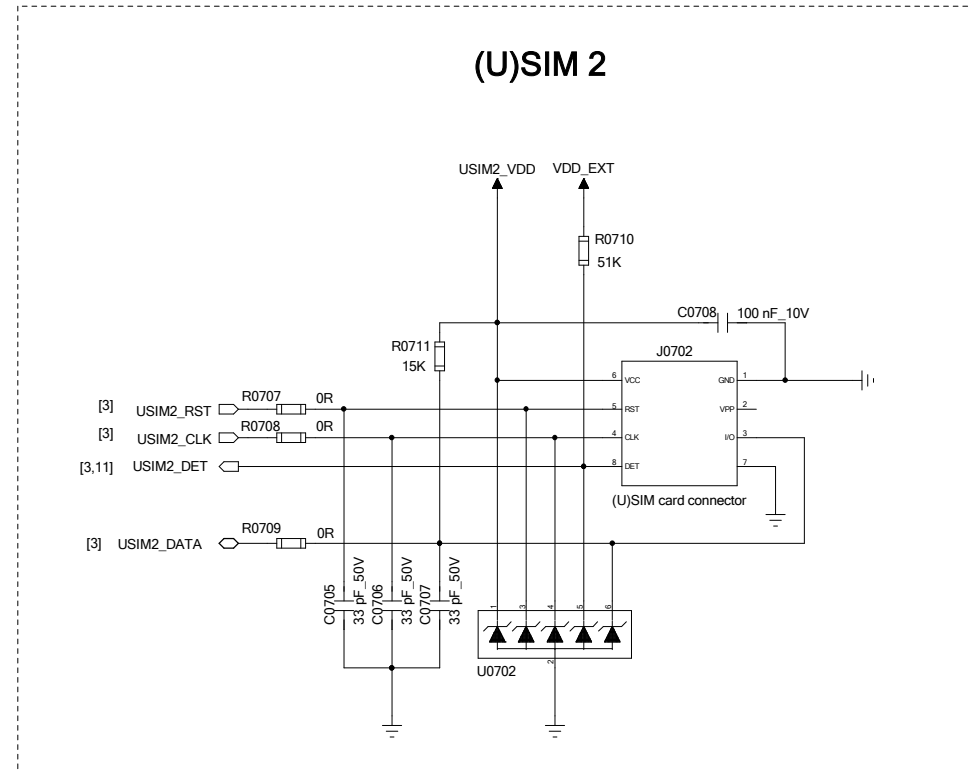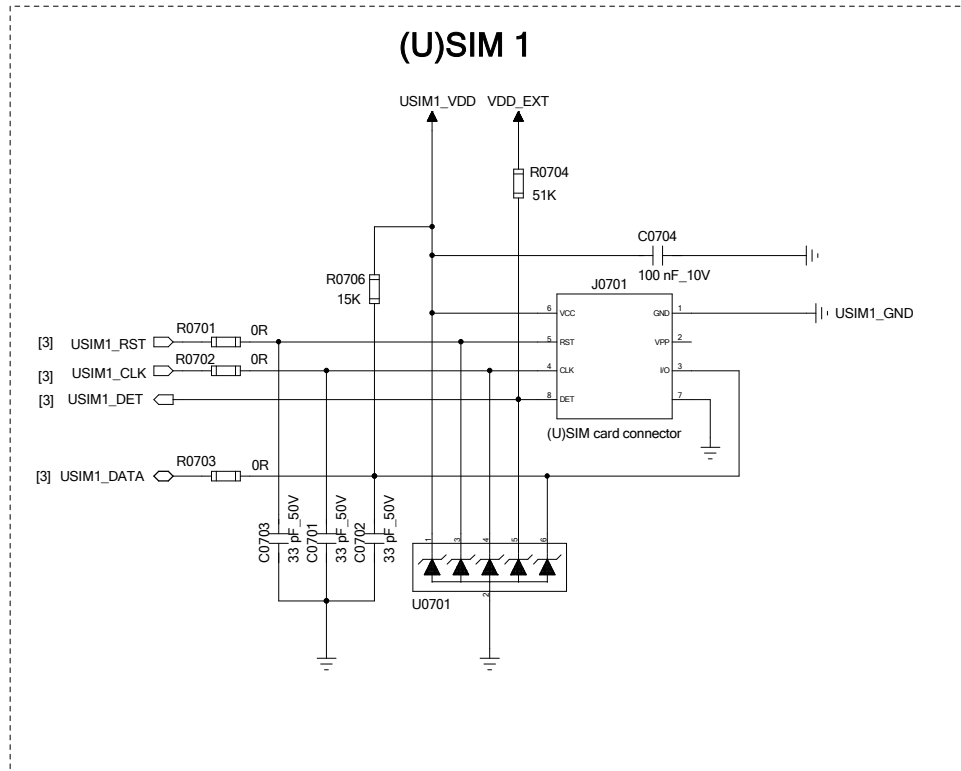
NOTE:

1. U0701 and U0702 are recommended to be used to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.

2. The pull-up resistor R0706 & R0711 can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.

3. R0701-R0703 and R0707-R0709 are used for debugging, and C0701-C0703 and C0705-C0707 are used for filtering out RF interference.

4. C0704 and C0708's capacitance should not exceed 1 μF and they should be placed close to the (U)SIM card connector.

5. The GND of the (U)SIM card connector is recommended to be connected to the GND layer directly.

6. The module supports (U)SIM card hot-plug via the USIM_DET pin and both high-level and low-level detections are supported. The function is disabled by default.

7. For more information about the layout of (U)SIM interface, see the hardware design document of the module.

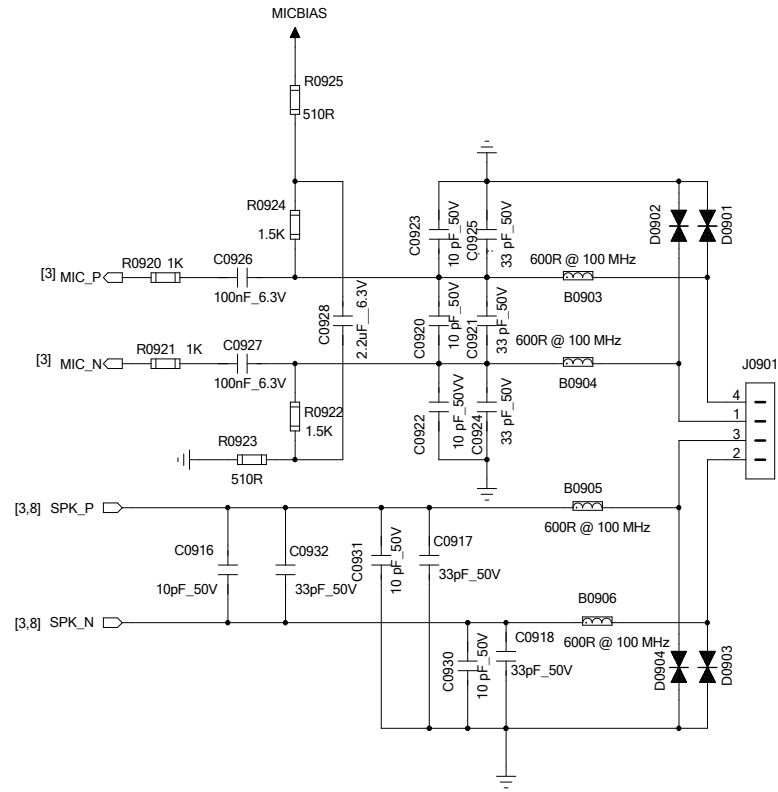# Analog Audio Design (External Audio Amplifier)
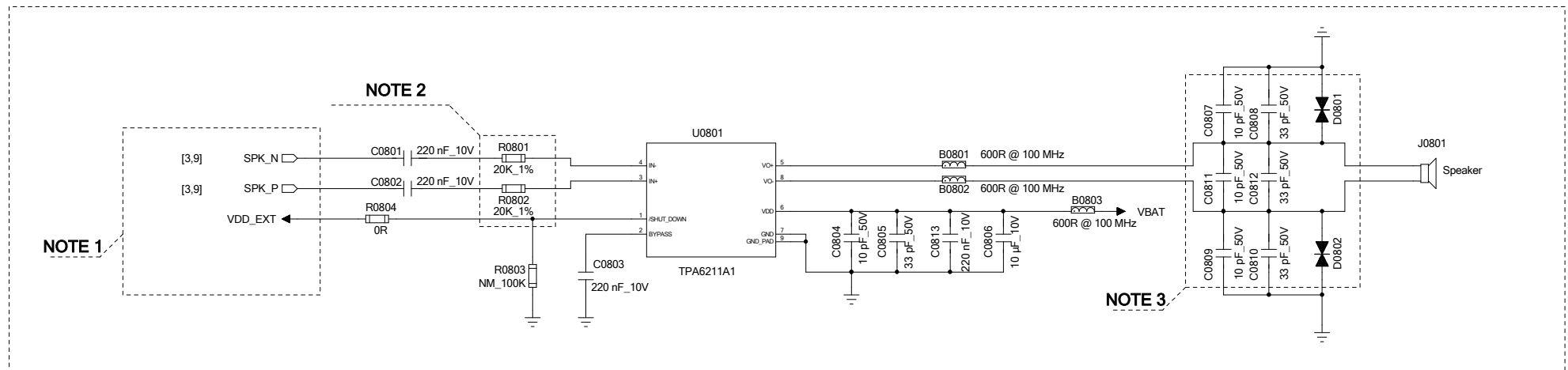
NOTE:

1. SPK_N and SPK_P are differential output channels that can connect an audio PA. When the channels are turned on or off, it is possible for the module to emit a pop sound, which can be eliminated by controlling the enable pin of the audio PA. For details, please contact Quectel Technical Support.
2. Choose the audio power amplifier with appropriate power according to the actual needs. Audio PA Gain = 40 kΩ / R0801 or R0802.
3. Place filter capacitors and ESD protection components close to the loudspeaker and the selection of ESD protection components is related to the selection of audio power amplifiers. Ensure that the output voltage of the audio power amplifier is within the maximum reverse working voltage range of the ESD protection components.
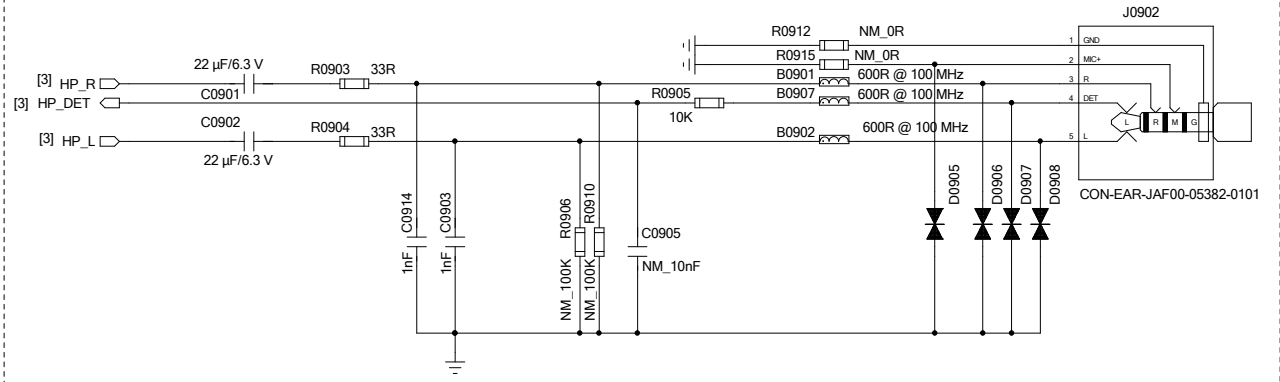
Analog Audio Interface Design

Handset (Microphone and Earpiece)

MICBIAS

R0925 510R
R0924 1.5K
R0920 1K
[3] MIC_P
C0926 100nF_6.3V
C0928 2.2uF_6.3V
C0923
C0925 33 pF_50V
C0920 10 pF_50V
C0921 33 pF_50V
D0902
D0901
B0903 600R @ 100 MHz
R0921 1K
[3] MIC_N
C0927 100nF_6.3V
C0922 10 pF_50V
C0924 33 pF_50V
R0922 1.5K
R0923
510R
B0904 600R @ 100 MHz
J0901
4
1
3
2
[3,8] SPK_P
C0916 10pF_50V
C0932 33pF_50V
C0931 10 pF_50V
C0917 33pF_50V
B0905 600R @ 100 MHz
[3,8] SPK_N
C0930 10 pF_50V
C0918 33pF_50V
B0906 600R @ 100 MHz
D0904
D0903

Headphone

J0902
R0912 NM_0R
R0915 NM_0R
B0901 600R @ 100 MHz
B0907 600R @ 100 MHz
B0902 600R @ 100 MHz
22 µF/6.3 V
[3] HP_R
C0901
R0903 33R
[3] HP_DET
C0902
R0904 33R
[3] HP_L
22 µF/6.3 V
R0905 10K
C0914 1nF
C0903 1nF
R0906 NM_100K
R0910 NM_100K
C0905 NM_10nF
1 GND
2 MIC+
3 R
4 DET
5 L
L R M G
CON-EAR-JAF00-05382-0101
D0905
D0906
D0907
D0908

Compatible Design

	CTIA	OMTP
R0912	NM	M
R0915	M	NM

Headphone Insertion Detection Mechanism

	Pins 4 and 5
Plug in	Connected
Plug out	Disconnected

Headphone type	Line sequence
OMTP	L, R, MIC+, GND
CTIA	L, R, GND, MIC+

NOTE:
1. Both the MIC and SPK signal traces need to be routed as differential pairs.
2. All MIC and SPK signal traces should be surrounded with ground on the layer and with ground planes above and below, and far away from noise sources.
3. ESD protection components should be placed as close to the audio interfaces as possible
and ensure that the audio voltage is within the maximum reverse working voltage range of the ESD protection components.

UART Interface Design

UART Level-shifting Circuit - Transistor Solution

VDD_EXT VDD_EXT

NOTE 3

C1003
1 nF_50V   R1005 4.7K   R1006 10K

[4,10] TXD_MCU   Q1003   MAIN_RXD [3,10]
2SC4617TLQ

VDD_MCU VDD_EXT

NOTE 3

R1003 10K   R1004 4.7K   C1002
1 nF_50V

[4,10] RXD_MCU   Q1002   MAIN_TXD [3,10]
2SC4617TLQ

UART Level-shifting Circuit - IC Solution

C1007 100 nF_10V

C1008 100 nF_10V

U0902

VDD_EXT
[3,10] MAIN_TXD
[3,10] MAIN_RXD
[3] MAIN_CTS
[3] MAIN_RTS

1 VCCA   VCCB 14   VDD_MCU
2 A1   B1 13   RXD_MCU [4,10]
3 A2   B2 12   TXD_MCU [4,10]
4 A3   B3 11   CTS_MCU [4]
5 A4   B4 10   RTS_MCU [4]
6 NC   NC 9
7 GND   OE 8

10K R1010   VDD_EXT
120K R1011

TXS0104EPWR

NOTE 5

NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter.

2. The power supply of TXS0104EPWR's VCCA should not exceed that of VCCB. For more information, see the datasheet of TXS0104EPWR.

3. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C1002 and C1003 of 1 nF can improve the signal quality.

4. The MAIN_RTS level-shifting circuit is similar to that of the MAIN_RXD.
   The MAIN_CTS level-shifting circuit is similar to that of the MAIN_TXD.

5. The module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS. In addition, pay attention to the direction of connection.
   The TXD and RXD of the module are respectively connected to the RXD and TXD of the MCU.

Test Points

USB Interface Test Points

J1102

1
2 — USB_DM_TEST [3]
3 — USB_DP_TEST [3]
4 — USB_VBUS

D1101 D1102 D1105
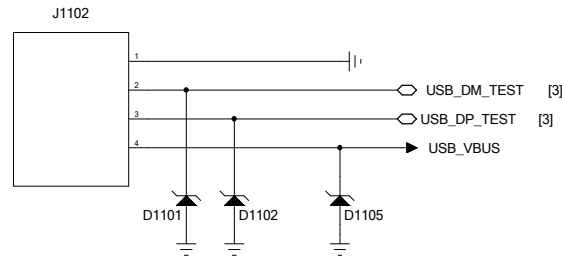
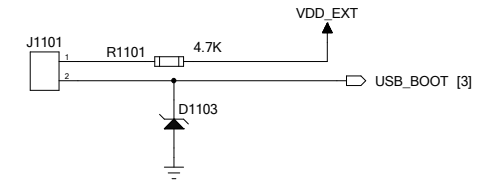**NOTE:**
1. Test points must be reserved for USB interface to debug software.
2. The module can upgrade the firmware over USB interface.
3. The parasitic capacitance of the ESD protection components on USB data traces should not exceed 2 pF. Ensure that the signal voltage is within the maximum reverse working voltage range of the ESD protection components.
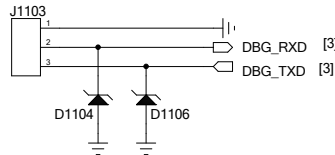
USB_BOOT Interface Test Points

VDD_EXT

J1101 R1101 4.7K
1
2 — USB_BOOT [3]

D1103

NOTE:
1. It is recommended to reserve a test point for USB_BOOT interface.
2. Pull up the USB_BOOT to VDD_EXT before the module starts up, and the module will enter emergency download mode after powering up. In this mode, the module supports firmware upgrade over USB interface.

Debug UART Test Points

J1103
1
2 — DBG_RXD [3]
3 — DBG_TXD [3]

D1104 D1106

NOTE:
1. Test points must be reserved for DBG_TXD and DBG_RXD for debugging.
2. The debug UART interface supports 1.8 V power domain, and a level-shifting circuit should be used if the power domain of your application is 3.3 V. For details, refer to "UART Interface Design" sheet.
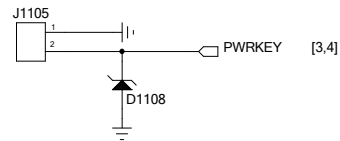3. The debug UART only supports the baud rate of 921600 bps.

USIM2_DET Test Point

J1104
1
2 — USIM2_DET [3,7]

D1107
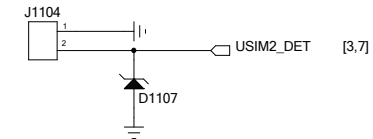
NOTE:
1. A test point must be reserved to capture CP logs.
2. The USIM2_DET test point supports 1.8 V power domain.
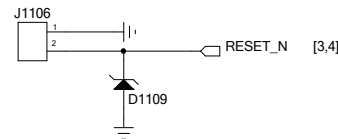3. When capturing the CP log, set the baud rate to 8000000 bps.

PWRKEY Test Point

J1105
1
2 — PWRKEY [3,4]

D1108

NOTE:

It is recommended to reserve a test point for PWRKEY.

RESET_N Test Point

J1106
1
2 — RESET_N [3,4]

D1109

NOTE:

It is recommended to reserve a test point for RESET_N if it is unused.

VBAT Test Point
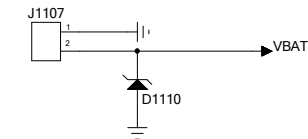
J1107
1
2 — VBAT

D1110

NOTE:

It is recommended to reserve a test point for VBAT.

Indicator Designs

DC_5V

D1201

R1202
2.2K

[3]   STATUS   Q1201
DTC043ZEBTL

DC_5V

D1202

R1203
2.2K

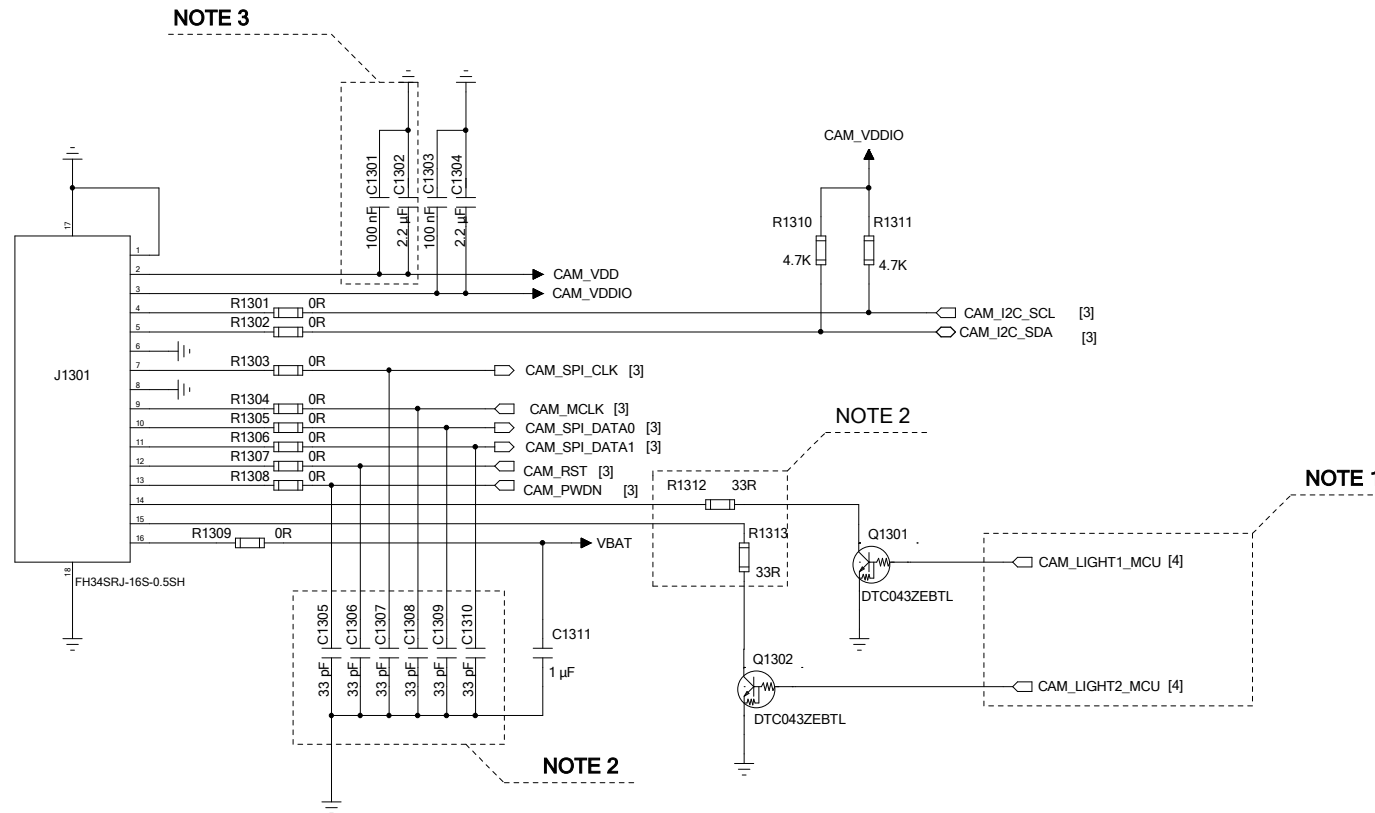[3]   NET_STATUS   Q1202
DTC043ZEBTL
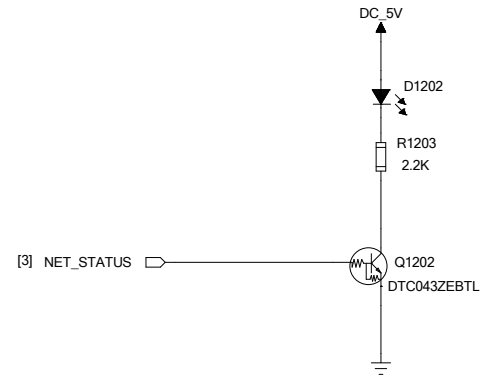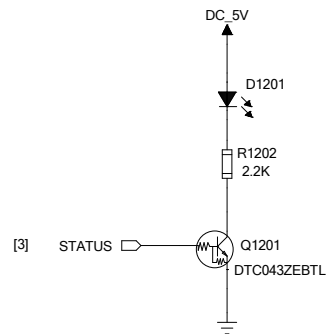
NOTE:

1. For more details about STATUS and NET_STATUS, see the hardware design document of the module.

2. If the low power consumption is required when your device is in sleep status, replace the power supply DC_5V of the STATUS and NET_STATUS indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

Camera Interface Design

NOTE 3

C1301 100 nF
C1302 2.2 µF
C1303 100 nF
C1304 2.2 µF

CAM_VDDIO

R1310 4.7K
R1311 4.7K

J1301

CAM_VDD
CAM_VDDIO

R1301 0R
R1302 0R

CAM_I2C_SCL [3]
CAM_I2C_SDA [3]

R1303 0R — CAM_SPI_CLK [3]
R1304 0R — CAM_MCLK [3]
R1305 0R — CAM_SPI_DATA0 [3]
R1306 0R — CAM_SPI_DATA1 [3]
R1307 0R — CAM_RST [3]
R1308 0R — CAM_PWDN [3]

NOTE 2

R1312 33R

R1309 0R — VBAT

R1313 33R

Q1301
DTC043ZEBTL

CAM_LIGHT1_MCU [4]

NOTE 1

FH34SRJ-16S-0.5SH

C1305 33 pF
C1306 33 pF
C1307 33 pF
C1308 33 pF
C1309 33 pF
C1310 33 pF

C1311 1 µF

Q1302
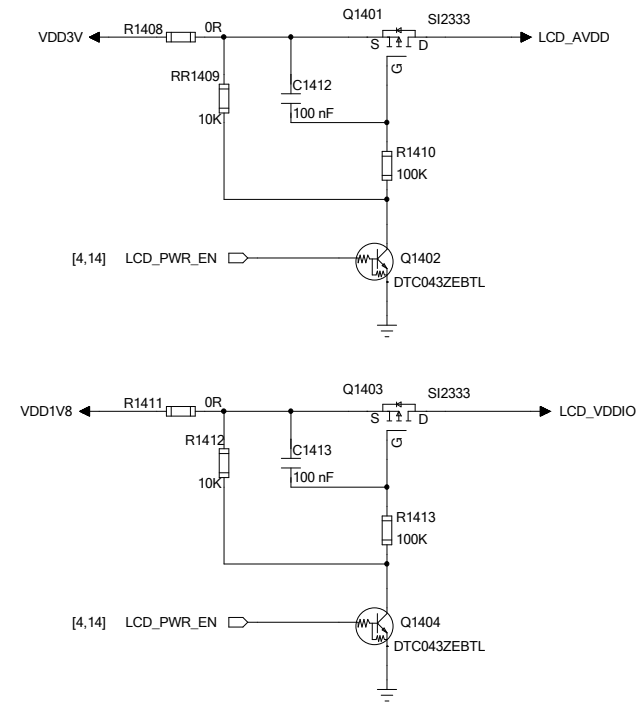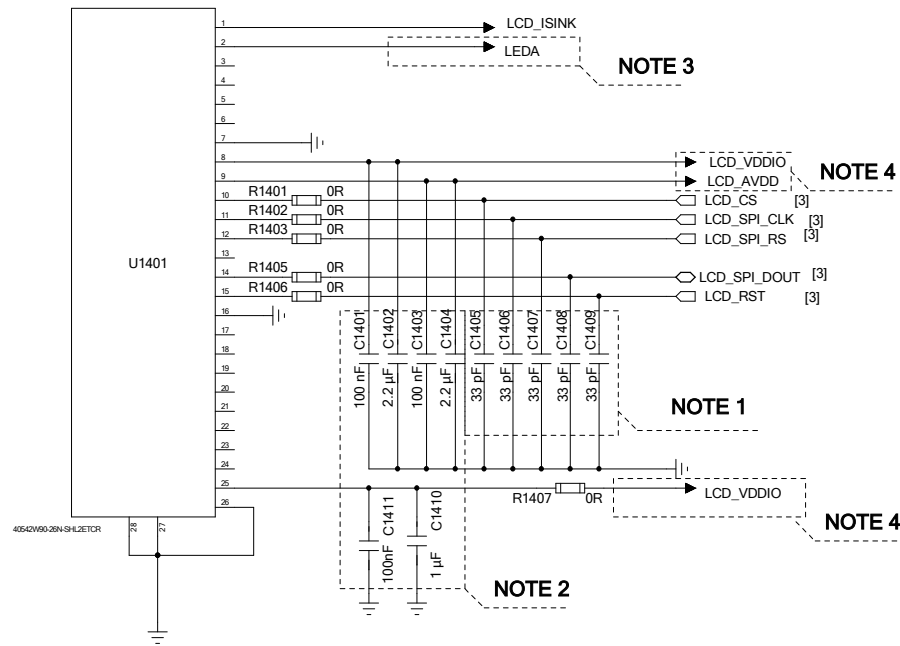DTC043ZEBTL

CAM_LIGHT2_MCU [4]

NOTE 2

NOTE:
1. CAM_LIGHT1_MCU controls the cathode of the position light of the camera by controlling the triode switching circuit;
   CAM_LIGHT2_MCU controls the cathode of the supplement light of the camera by controlling the triode switching circuit;
   Choose GPIO pins with default pull-down status as CAM_LIGHT1_MCU and CAM_LIGHT2_MCU.
2. The 33 pF capacitors of the signal pins are reserved, and they can be used according to the actual debugging situation.
   The values of current limiting resistors of position light and supplement light (R1312 and R1313) should be varied according to desired brightness level.
3. The capacitors of the CAM_VDD power supply should be connected to the GND layer directly, otherwise there may be power noise leading to abnormalities such as white dots on the preview screen.

LCM Interface Design

LCD_ISINK
LEDA
NOTE 3

U1401
40542W90-26N-SHL2ETCR

LCD_VDDIO
LCD_AVDD
NOTE 4

R1401 0R — LCD_CS [3]
R1402 0R — LCD_SPI_CLK [3]
R1403 0R — LCD_SPI_RS [3]
R1405 0R — LCD_SPI_DOUT [3]
R1406 0R — LCD_RST [3]

C1401 100 nF
C1402 2.2 µF
C1403 100 nF
C1404 2.2 µF
C1405 33 pF
C1406 33 pF
C1407 33 pF
C1408 33 pF
C1409 33 pF

NOTE 1

C1411 100nF
C1410 1 µF

R1407 0R — LCD_VDDIO
NOTE 4

NOTE 2

VDD3V — R1408 0R — Q1401 SI2333 — LCD_AVDD
RR1409 10K
C1412 100 nF
R1410 100K
[4,14] LCD_PWR_EN — Q1402 DTC043ZEBTL

VDD1V8 — R1411 0R — Q1403 SI2333 — LCD_VDDIO
R1412 10K
C1413 100 nF
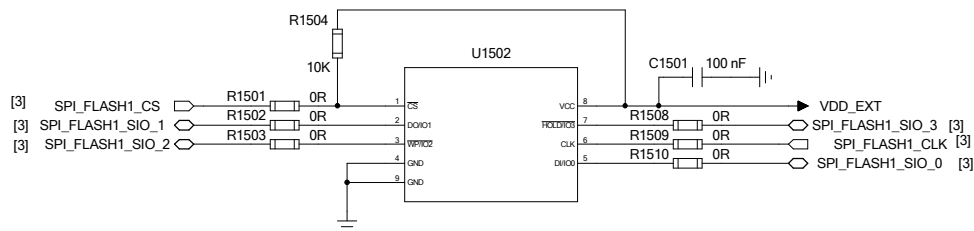R1413 100K
[4,14] LCD_PWR_EN — Q1404 DTC043ZEBTL

NOTE:
1. The 33 pF capacitors of the signal pins are reserved, and can be used as per the actual debugging situation.
2. To avoid abnormal LCD display caused by power fluctuation, the filter capacitors of LCD_AVDD and LCD_VDDIO must be mounted.
3. The power supply pin LEDA of the backlight is provided by an external power supply circuit, and you can design the circuit by yourself.
4. The LCD analog power supply LCD_AVDD and digital power supply LCD_VDDIO are externally provided.
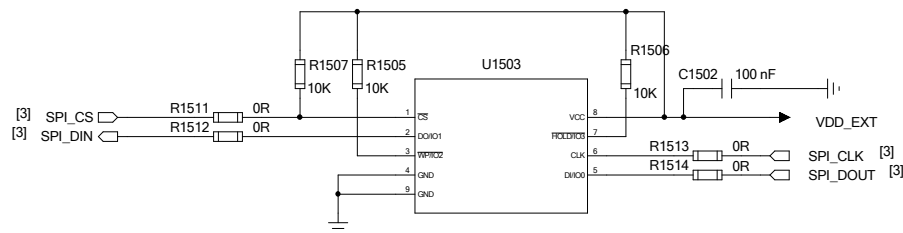   The nominal voltage of LCD_VDDIO is 1.8 V and the nominal voltage of LCD_AVDD is 2.8 V.

External Flash Interface Design

Six-wire NOR Flash Circuit Design

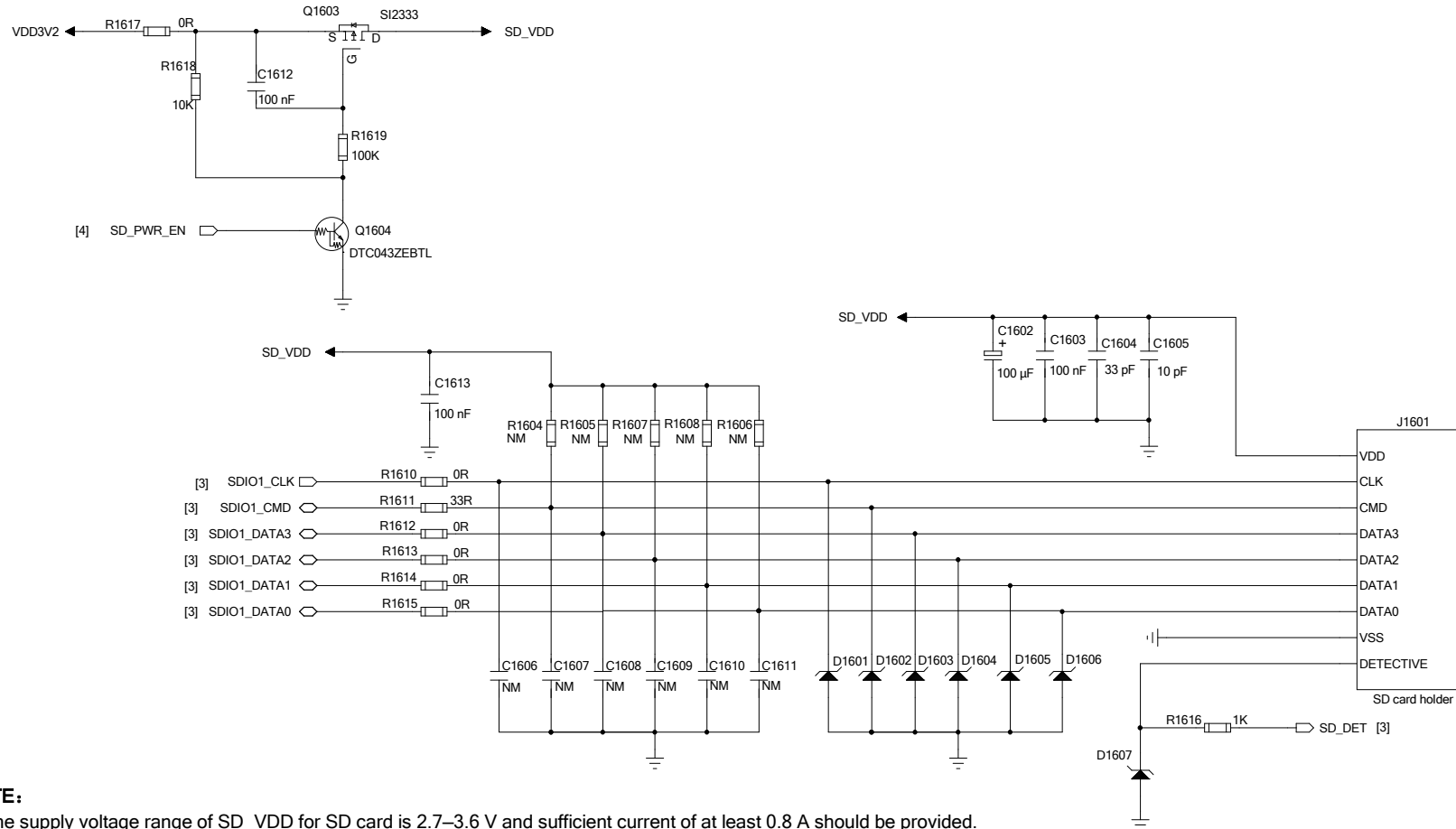## Four-wire NOR Flash Circuit Design

NOTE:

1. The filter capacitors C1501 and C1502 need to be placed close to the power pins of the flash chip to achieve the expected filtering effect.
2. For the four-wire NOR flash circuit, it is recommended that the WP and HOLD pins be connected with pull-up resistors,
   so as to avoid abnormal levels to damage the flash chip, resulting in abnormal transmission or data loss.
3. The SPI of the module only supports master mode, that is, the module can only be a host when communicating with the peripherals through the SPI.
4. There are two design schemes for the flash circuit of the module to be selected according to the design requirements.

SD Card Interface Design

VDD3V2

R1617 0R

Q1603 SI2333

SD_VDD

R1618 10K

C1612 100 nF

R1619 100K

[4] SD_PWR_EN

Q1604 DTC043ZEBTL

SD_VDD

C1602 + 100 µF

C1603 100 nF

C1604 33 pF

C1605 10 pF

C1613 100 nF

R1604 NM

R1605 NM

R1607 NM

R1608 NM

R1606 NM

J1601

VDD

[3] SDIO1_CLK — R1610 0R — CLK

[3] SDIO1_CMD — R1611 33R — CMD

[3] SDIO1_DATA3 — R1612 0R — DATA3

[3] SDIO1_DATA2 — R1613 0R — DATA2

[3] SDIO1_DATA1 — R1614 0R — DATA1

[3] SDIO1_DATA0 — R1615 0R — DATA0

VSS

C1606 NM

C1607 NM

C1608 NM

C1609 NM

C1610 NM

C1611 NM

D1601 D1602 D1603 D1604 D1605 D1606

DETECTIVE

SD card holder

R1616 1K SD_DET [3]

D1607

NOTE：

1. The supply voltage range of SD_VDD for SD card is 2.7–3.6 V and sufficient current of at least 0.8 A should be provided.

2. To avoid the jitter of bus, pull-up resistors R1604–R1608 are recommended to be added to SDIO bus. SDIO bus needs to be connected to a pull-up power supply.
   The values of these resistors are among 10–100 kΩ. The recommended value is 4.7 kΩ and the resistors are not mounted by default. The recommended pull-up power supply is 3.2 V.

3. In order to improve the signal quality, it is recommended to add 0 Ω resistors R1610–R1615 in series between the module and the SD card connector.
   The bypass capacitors C1606–C1611 are reserved and not mounted by default.

4. In order to ensure good ESD performance, it is recommended to add a TVS array and place it as close as possible to the SD card connector,
   and ensure that the junction capacitance of the TVS array is less than 15 pF.

5. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock and DC-DC signals.

6. It is important to route the SDIO signal traces with ground surrounded, and the impedance is controlled at 50 Ω ±10 %.
   The traces of SDIO1_CLK, SDIO1_DATA[0:3] and SDIO1_CMD should be equal in length (the difference is less than 1 mm),
   and the total length should be less than 50 mm.

7. The spacing between SDIO signals and other signals needs to be greater than twice the trace width, and ensure that the bus capacitance is less than 15 pF.