EG915U Series QuecOpen Hardware Design

LTE Standard Module Series

Version: 1.0

Date: 2023-10-09

Status: Released

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-06-30	Len CHEN/ Ailsa WANG	Creation of the document
1.0	2023-10-09	Anla HUANG/ Woping WANG/ Loft XU	First official release

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines the EG915U series module in QuecOpen® solution and describes its air interfaces and hardware interfaces which are connected with your applications.

It can help you quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use this module to design and to set up mobile applications easily.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument, and so on, it indicates that the function, feature, interface, pin, AT command, argument, and so on, are under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SD_SDIO_DATA[0:3] refers to all four SD_SDIO_DATA pins, SD_SDIO_DATA0, SD_SDIO_DATA1, SD_SDIO_DATA2, and SD_SDIO_DATA3.

2 Product Overview

EG915U series is an LTE Cat 1 module, which supports LTE-FDD, LTE-TDD and GPRS network data connection. It provides voice functionality as well as Bluetooth and Wi-Fi Scan functions to meet your specific application demands.

Table 2: Brief Introduction of the Module

Category	
Packaging and Number of Pins	LGA; 126
Dimensions	(23.6 ±0.2) mm × (19.9 ±0.2) mm × (2.4 ±0.2) mm
Weight	2.5 ±0.2 g
Wireless Network Functions	LTE/GSM/Bluetooth [1]/Wi-Fi Scan [1]
Variants	EG915U-CN [2], EG915U-EU, EG915U-LA

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Wireless Network Type	EG915U-CN	EG915U-EU	EG915U-LA
LTE-FDD	B1/B3/B5/B8	B1/B3/B5/B7/B8/B20/ B28	B2/B3/B4/B5/B7/B8 /B28/B66
LTE-TDD	B34/B38/B39/B40/B41	-	-
GSM	900/1800 MHz	850/900/1800/1900 MHz	850/900/1800/ 1900 MHz
Bluetooth and Wi-Fi Scan [1]	2.4 GHz	2.4 GHz	2.4 GHz

[1] EG915U series supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used simultaneously. Pease contact Quectel Technical Support for details about specific models.
[2] Only EG915U-CN supports LTE-TDD. For details, please contact Quectel Technical Support.

2.2. Key Features

Table 4: Key Features

Feature	Description
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	**EG915U-CN:** ● EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800: Class 1 (30 dBm ±2 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB) ● LTE-TDD: Class 3 (23 dBm ±2 dB) **EG915U-EU & EG915U-LA:** ● GSM850/EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800/PCS1900: Class 1 (30 dBm ±2 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB)
LTE Features	**EG915U-CN:** ● Supports up to 3GPP Rel-13 Cat 1 FDD/TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports uplink QPSK and 16QAM ● Supports downlink QPSK, 16QAM, and 64QAM ● Max. transmission data rates: – LTE-FDD: 10 Mbps (DL)/5 Mbps (UL) – LTE-TDD: 8.96 Mbps (DL)/3.1 Mbps (UL) **EG915U-EU & EG915U-LA:** ● Supports up to 3GPP Rel-13 Cat 1 FDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports uplink QPSK and 16QAM ● Supports downlink QPSK, 16QAM, and 64QAM ● Max. transmission data rates: – LTE-FDD: 10 Mbps (DL)/5 Mbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1–4 ● Max. transmission data rates: 85.6 kbps (DL)/85.6 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/ FTPS/SSL/FILE/MQTT/MMS/SMTP/SMTPS protocols ● Supports PAP and CHAP for PPP connections
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast

	• SMS storage: (U)SIM card and ME; ME by default
Audio Features	• Supports one analog audio input and two analog audio output channels • HR/FR/EFR/AMR/AMR-WB • Supports echo cancellation and noise suppression
LCM Interface	Supports LCM interface in SPI mode
Camera Interface	• Provides one camera interface supporting cameras up to 0.3 MP; I/O pins only support 1.8 V • Supports SPI two-data-line data transmission
External Flash Interface	• Supports connection to external flash chip • The interface is multiplexed from other pins
SD Card Interface	• Supports one interface compliant with SD 2.0 specification and can be used for connecting external SD card • Partial pins of the interface are multiplexed from other pin functions
USB Interface	• Compliant with USB 2.0 specification (slave mode only), with maximum transmission rate up to 480 Mbps • Used for data transmission, software debugging and firmware upgrade • Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–6.5, and Android 4.x–13.x
USB_BOOT Interface	• Supports one USB_BOOT interface • Forces the module into emergency download mode
(U)SIM Interfaces	• Supports USIM/SIM card: 1.8/3.0 V • Supports Dual SIM Single Standby
PCM Interface	• Supports one PCM interface (slave mode only) • Used for audio function with external codec connected
I2C Interface	• Supports one I2C interface • Complies with the I2C-bus specification
UART Interfaces	**Main UART:** • Used for data transmission • Baud rates: up to 921600 bps; 115200 bps by default • Supports RTS and CTS hardware flow control **Debug UART:** • Used for log output • Baud rate: 921600 bps • Cannot be used as a general-purpose UART **Auxiliary UART:** • The baud rate is the same as that of the main UART
ADC Interfaces	Supports two ADC Interfaces
SPI	• Supports one SPI (master mode only) • 1.8 V voltage domain • Clock frequency: up to 25 MHz

Indication Signals	● STATUS Indicates the module's operation status ● NET_STATUS indicates the network activity status
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Bluetooth and Wi-Fi Scan antenna interface (ANT_BT/WIFI_SCAN) ● 50 Ω characteristic impedance
Position Fixing	Supports Wi-Fi Scan
Temperature Range	● Operating temperature range [3]: -35 to +75 °C ● Extended temperature range [4]: -40 to +85 °C ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	Via USB interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- Memory
- Radio frequency
- Peripheral interfaces

[3] Within this range, the module's indicators comply with 3GPP specification requirements.
[4] Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

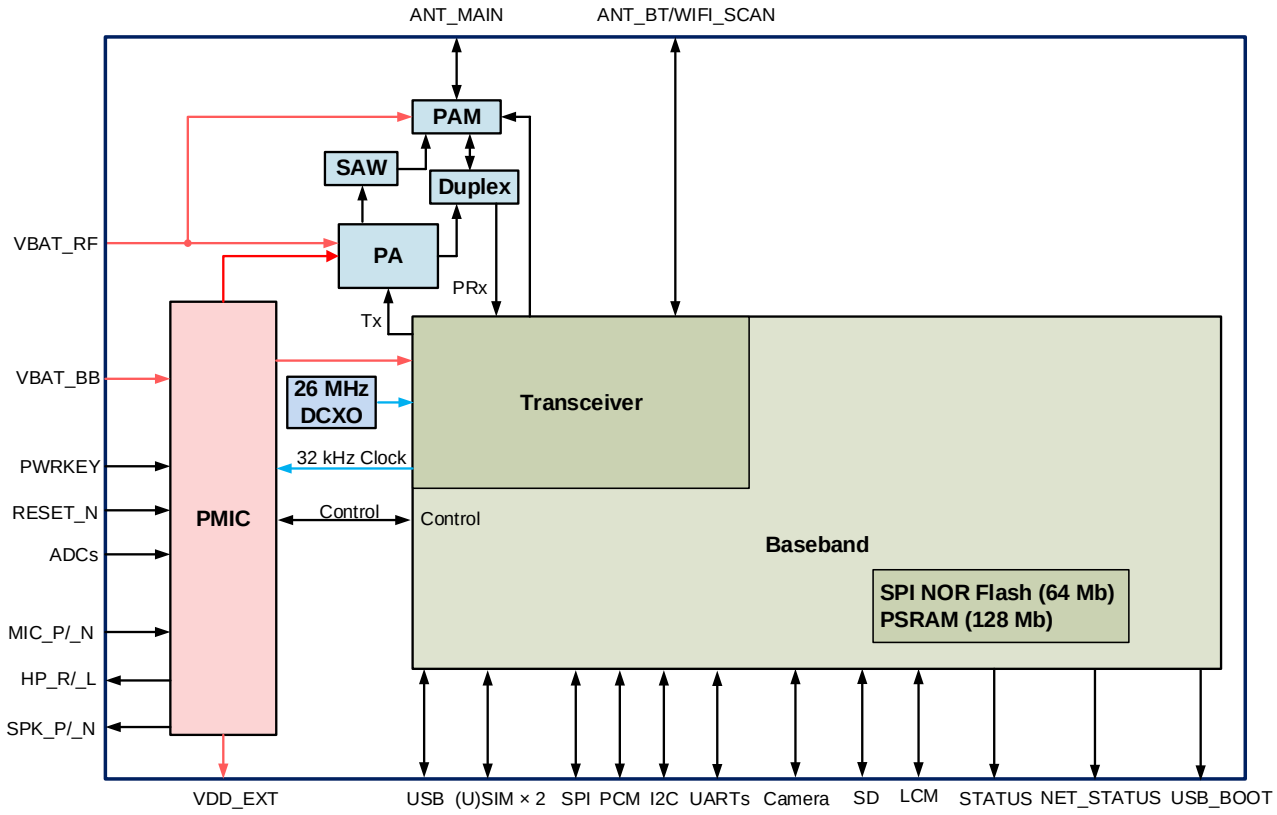


Figure 1: Functional Diagram

2.4. Pin Assignment

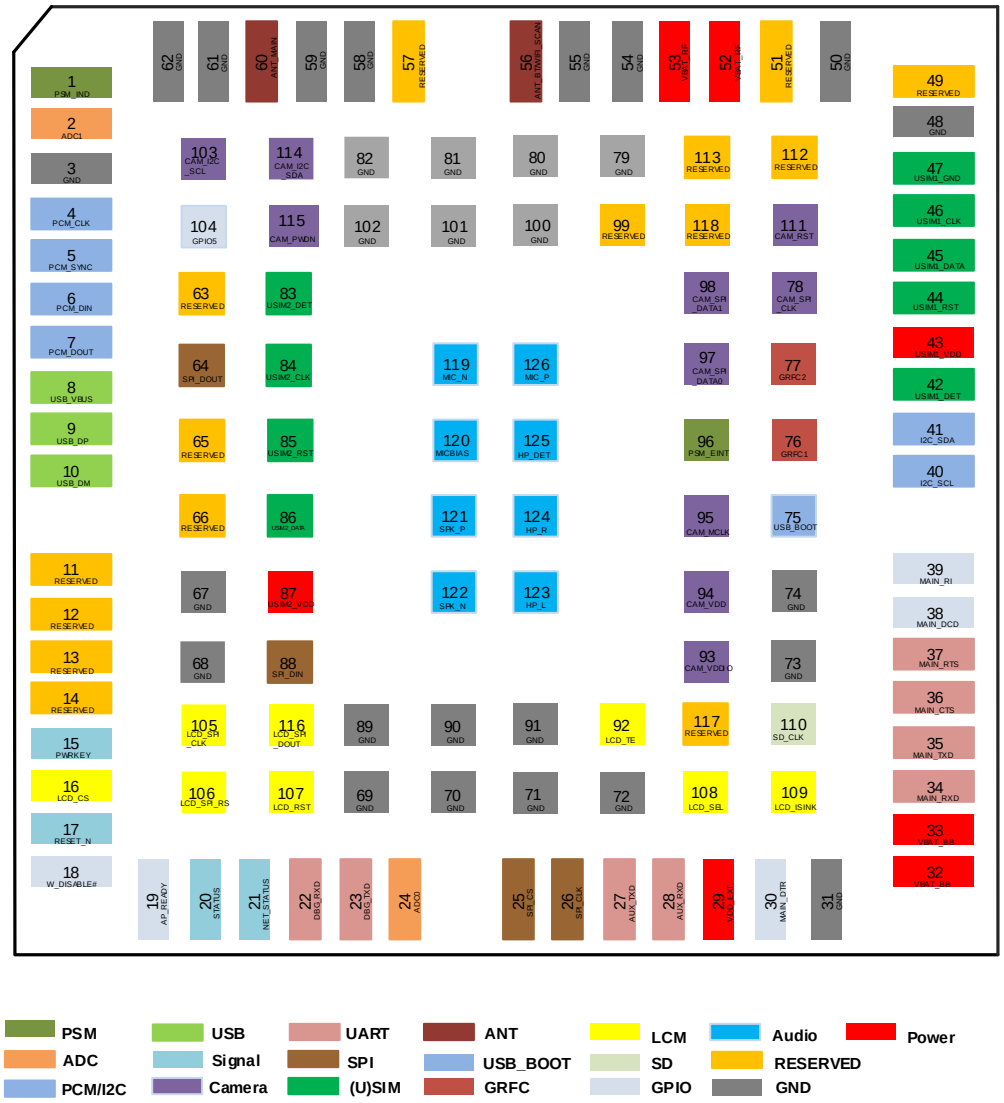


Figure 2: Pin Assignment (Top View)

NOTE

1. When the emergency download mode is not needed, do not pull up USB_BOOT before the module starts up successfully.
2. Keep unused and RESERVED pins unconnected, and all GND pins are connected to the ground network.
3. The module supports Dual SIM Single Standby. For details, please contact Quectel Technical Support.
4. When using pins 18, 19, 30, 38, 39, and 110, please note that these pins will have a period of

variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

2.5. Pin Description

The following tables show the pin definition of the module.

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current of at least 1 A.

					Test points are recommended to be reserved.
VBAT_RF	52, 53	PI	Power supply for the module's RF part		It must be provided with sufficient current of at least 2.5 A. Test points are recommended to be reserved.
VDD_EXT	29	PO	Provides 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Used with a 2.2 μF capacitor and TVS component. A test point is recommended to be reserved.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
Turn On/Off/Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turns on/off the module	V_{IL}max = 0.5 V	VBAT power domain. Active low. A test point is recommended to be reserved.
RESET_N	17	DI	Resets the module		VBAT power domain. Active low. A test point is recommended to be reserved if unused.
Indication Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicates the module's operation status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep them open.
NET_STATUS	21	DO	Indicates the module's network activity status		
USB Interface					
Pin Name	**Pin**	**I/O**	**Description**	**DC**	**Comment**

	No.			Characteristics	
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.5 V Vnom = 5.0 V	A test point must be reserved.
USB_DP	9	AIO	USB 2.0 differential data (+)		USB 2.0 compliant. Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	10	AIO	USB 2.0 differential data (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_CLK	46	DO	(U)SIM1 card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_RST	44	DO	(U)SIM1 card reset		
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM1_GND	47	-	Ground	-	Specified ground for (U)SIM1 card.
USIM2_VDD	87	PO	(U)SIM2 card power supply	Iomax = 50 mA **1.8 V (U)SIM:**	Either 1.8 V or 3.0 V (U)SIM card is

				Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	supported and can be identified automatically by the module.
USIM2_DATA	86	DIO	(U)SIM2 card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_CLK	84	DO	(U)SIM2 card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_RST	85	DO	(U)SIM2 card reset		
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. A test point must be reserved for debugging.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	36	DO	Clear to send signal from the module (Connect to MCU's CTS)	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_RTS	37	DI	Request to send signal to the module (Connect to MCU's RTS)	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
MAIN_RXD	34	DI	Main UART receive		
MAIN_TXD	35	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
Auxiliary UART Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
AUX_TXD	27	DO	Auxiliary UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Test points must be reserved for debugging.
DBG_TXD	23	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PSM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PSM_EINT	96	DI	External interrupt, wakes up the module from PSM		1.8 V power domain. Wakes up the module from PSM when being pulled high externally. If unused, keep it open.
PSM_IND*	1	DO	Indicate the module's power saving mode		1.8 V power domain. If unused, keep it open.
I2C and PCM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	5	DI	PCM data frame sync	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open. Support slave mode only.
PCM_CLK	4	DI	PCM clock		
PCM_DIN	6	DI	PCM data input		
PCM_DOUT	7	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

I2C_SCL	40	OD	I2C serial clock		1.8 V power domain. They need to be pulled up to 1.8 V externally. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data		
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface		50 Ω characteristic impedance.
ANT_BT/ WIFI_SCAN	56	AIO	The shared interface for Bluetooth and Wi-Fi Scan		Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan only supports receiving. 50 Ω characteristic impedance. If unused, keep it open.
Antenna Tuner Control Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	76	DO	Generic RF Controller	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
GRFC2	77	DO			
SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CLK	26	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open. Supports master mode only.
SPI_CS	25	DO	SPI chip select		
SPI_DIN	88	DI	SPI data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SPI_DOUT	64	DO	SPI data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_TE	92	DI	LCD tearing effect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
LCD_RST	107	DO	LCD reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_SEL	108	DO	Reserved		
LCD_CS	16	DO	LCD chip select		
LCD_SPI_CLK	105	DO	LCD SPI clock		
LCD_SPI_RS	106	DO	LCD SPI register select		
LCD_SPI_DOUT	116	DIO	LCD SPI data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_ISINK	109	PI	Sink current input. Backlight adjustment	Imax = 200 mA. Current is configurable.	It is driven by sink current, connected to the cathode of the backlight, and the brightness can be adjusted with current control.
Camera Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CAM_MCLK	95	DO	Camera master clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
CAM_I2C_SCL	103	OD	Camera I2C clock		Pull each of them up to 1.8 V power domain with an external resistor. If unused, keep them open.
CAM_I2C_SDA	114	OD	Camera I2C data		

CAM_SPI_CLK	78	DI	Camera SPI clock	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
CAM_SPI_DATA0	97	DI	Camera SPI data bit 0		
CAM_SPI_DATA1	98	DI	Camera SPI data bit 1		
CAM_PWDN	115	DO	Camera power down	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
CAM_RST	111	DO	Camera reset		
CAM_VDD	94	PO	Camera analog power supply	Vnom = 2.8 V Iomax = 100 mA	Power supply of camera. If unused, keep them open.
CAM_VDDIO	93	PO	Camera digital power supply	Vnom = 1.8 V Iomax = 100 mA	
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO5	104	DIO	General-purpose input/output		Used as GPIO by default. 1.8 V power domain. If unused, keep them open.
MAIN_DCD	38	DIO			
MAIN_RI	39	DIO			
MAIN_DTR	30	DIO			
W_DISABLE#	18	DIO			
AP_READY	19	DIO			
USB_BOOT Interface					
Pin Name	**Pin No**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	75	DI	Force the module into emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Active high. A circuit that can set the module into emergency download mode should be reserved during design. A test point is recommended to be reserved.
ADC Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC0	24	AI	General-purpose ADC interfaces	Voltage range: 0 V to VBAT	It is recommended to reserve a voltage divider circuit. If unused, keep them open.
ADC1	2	AI			
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	110	DO	SD card clock		3.2 V power domain. If unused, keep it open.
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_N	119	AI	Microphone analog input (-)		If unused, keep it open.
MICBIAS	120	PO	Bias voltage output for microphone	Vmax = 3.0 V Vmin = 2.2 V Vnom = 2.2 V	
SPK_P	121	AO	Analog audio differential output (+)		
SPK_N	122	AO	Analog audio differential output (-)		
MIC_P	126	AI	Microphone analog input (+)		
HP_L	123	AO	Headphone left channel output		
HP_R	124	AO	Headphone right channel output		
HP_DET	125	DI	Headphone hot-plug detection		
RESERVED					
Pin Name	**Pin No.**				
RESERVED	11–14, 49, 51, 57, 63, 65, 66, 99, 112, 113, 117, 118				

NOTE

1. MAIN_DCD, MAIN_RI, MAIN_DTR, W_DISABLE#, AP_READY are not defined with functions corresponding to the pin names, but are used as GPIOs by default. For GPIO configuration, see ***document [1]***.
2. When using pins 18, 19, 30, 38, 39 and 110, please note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

2.6. EVB Kit

Quectel supplies an evaluation board (LTE OPEN EVB) with accessories to develop and test the module. For more details, see ***document [2]***.

3 Operating Characteristics

3.1. Operating Modes

The following table briefly outlines the operating modes referred in the following chapters.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module remains registered on the network and is ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	*ql_dev_set_modem_fun()* can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card are invalid.	
Airplane Mode	*ql_dev_set_modem_fun()* can set the module to airplane mode where RF function is invalid.	
Sleep Mode	In this mode, current consumption of the module is reduced to a low level. The module remains the ability to receive paging message, SMS, voice calls and TCP/UDP data from network normally.	
PSM	In this mode, current consumption of the module is reduced to a minimized level. API function cannot be sent to the module, but the module remains the ability to receive paging message from station and be woken up to work.	
Power Down Mode	PMU shuts down the power supply. Software is not active. However, Operating voltage connected to VBAT pins remains applied.	

NOTE

For more details about the API function, see ***document [3]***.

3.2. Sleep Mode

In sleep mode, the module can reduce power consumption to a low level. The following section describes power saving procedures of the module.

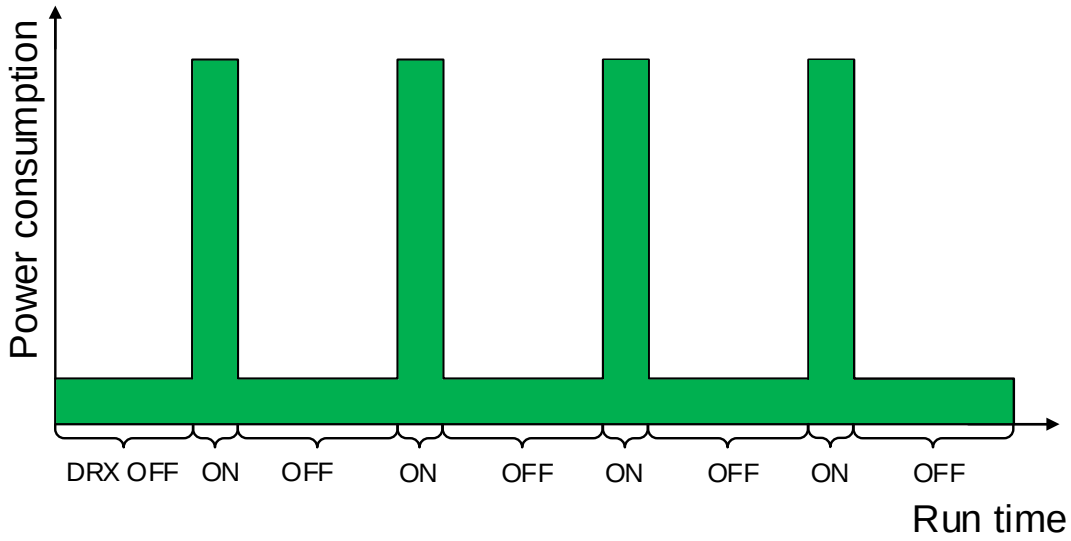


Figure 3: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. USB Application with USB Suspend/Resume Function

For the following two situations:

- The host supports USB suspend/resume and remote wakeup function
- The host supports USB suspend/resume, but does not support remote wake-up function

Three preconditions must be met to set the module to sleep mode:

- Enable sleep function by using *ql_autosleep_enable()*. For more details about the API function, see ***document [4]***.
- Ensure that all wakelocks have been released.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure illustrates the connection between the module and the host.

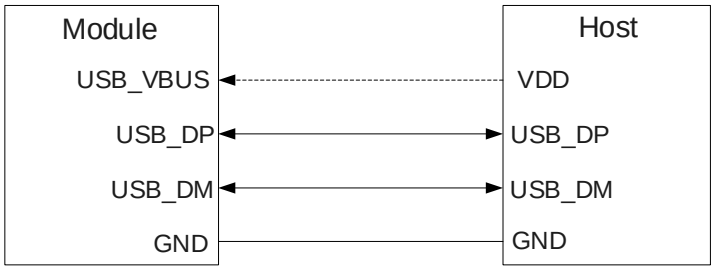


Figure 4: Sleep Mode Application with USB Suspend/Resume Function

You can wake up the module by sending data to it through USB.

3.2.2. USB Application Without USB Suspend Function

If the host does not support USB suspend function, disconnect USB_VBUS with an external control circuit to make the module enter sleep mode.

- Enable sleep function by using *ql_autosleep_enable()*.
- Ensure that all wakelocks have been released.
- Disconnect the USB_VBUS.

The following figure illustrates the connection between the module and the host.

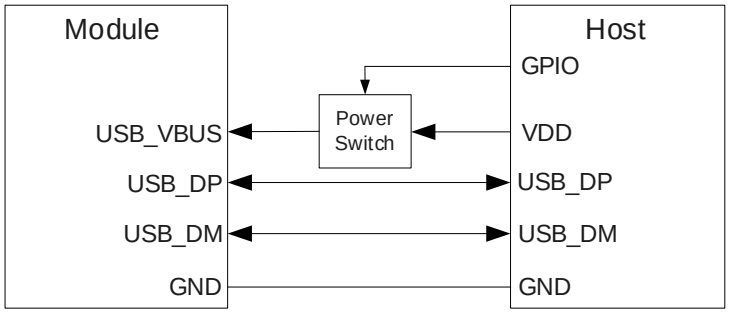


Figure 5: Sleep Mode Application Without USB Suspend Function

You can wake up the module by turning on the power switch to supply power to USB_VBUS.

NOTE

1. Pay attention to the level match shown in the dotted line between the module and the host.
2. USB suspend is supported on Linux system but not on Windows system.

3.3. Airplane Mode

When the module enters airplane mode, the RF function is disabled and all API functions related to it are inaccessible.

ql_dev_set_modem_fun() provides the choice of functionality level through setting parameter *at_dst_cfun* into 0, 1 or 4.

- *at_dst_cfun* is 0: Minimum functionality (Both RF function and (U)SIM functions are disabled).
- *at_dst_cfun* is 1: Full functionality mode (by default).
- *at_dst_cfun* is 4: Airplane mode (RF function is disabled).

3.4. PSM

The module supports power saving mode (PSM).

It enters the PSM through calling *ql_psm_sleep_enable()* and *ql_autosleep_enable()* when working normally. Pulling up PSM_EINT pin externally or setting the timer by software will enable the module to exit PSM.

Table 8: Pin Definition of PSM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PSM_EINT	96	DI	External interrupt, wakes up the module from PSM	Wakes up the module from PSM when being pulled high externally. If unused, keep it open.
PSM_IND*	1	DO	Indicate the module's power saving mode	If unused, keep it open.

NOTE

For more details about *ql_psm_sleep_enable()*, see ***document [5]***.

3.5. Power Supply

3.5.1. Power Supply Pins

The module provides 4 VBAT pins for connection with an external power supply.

- Two VBAT_RF pins for RF part.
- Two VBAT_BB pins for BB part.

Table 9: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	3.3	3.8	4.3	V
VBAT_RF	52, 53	PI	Power supply for the module's RF part				
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102						

3.5.2. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of at least 3.0 A when the GSM or both GSM and LTE are available, and provide sufficient current of at least 2.0 A when only LTE is available. If the voltage drop between input and output is not too high, it is suggested that an LDO should be used. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure illustrates a reference design for 5 V input power source. The typical output voltage of the power supply is about 3.8 V and the maximum load current is 3.0 A.

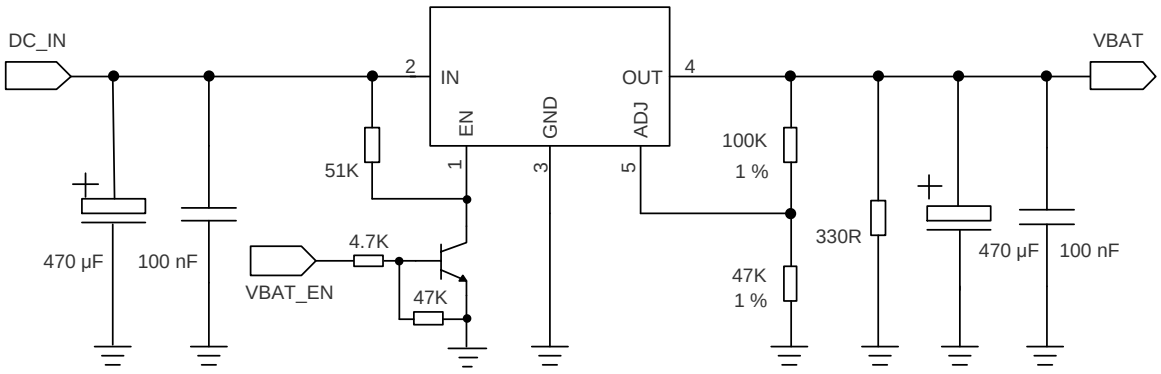


Figure 6: Reference Design of Power Supply

3.5.3. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure the input voltage never drops below 3.3 V.

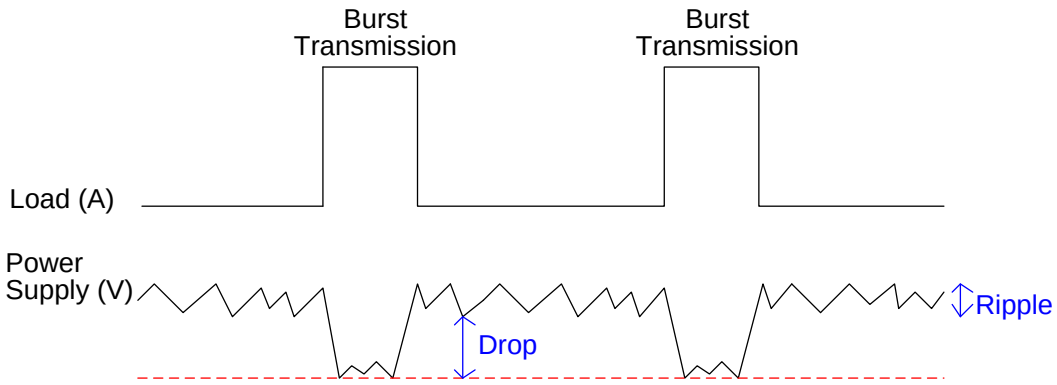


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a filter capacitor of about 100 µF with low ESR (ESR ≤ 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with the star configuration. The width of VBAT_BB trace should be at least 2 mm; and the width of VBAT_RF trace should be at least 2.5 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. The following figure shows the star configuration of the power supply.

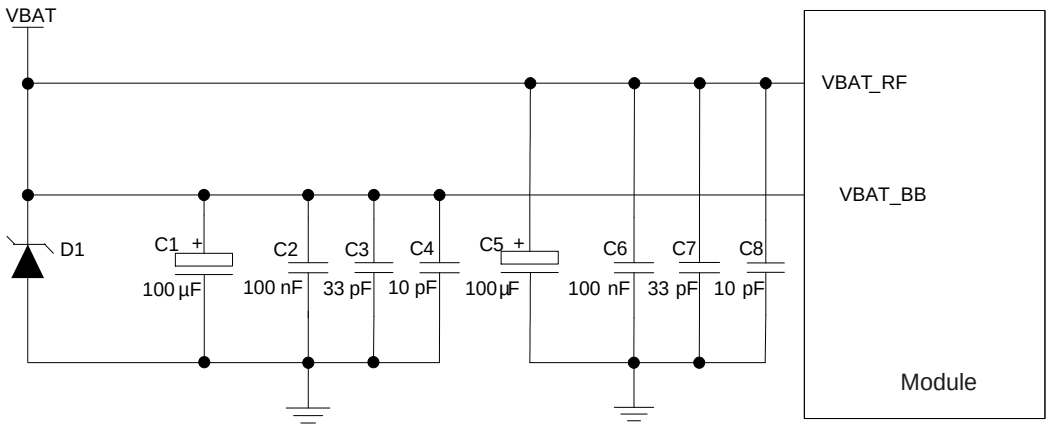


Figure 8: Power Supply in Star Configuration

3.6. Turn On

3.6.1. Turn On with PWPKEY

Table 10: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turns on/off the module	VBAT power domain. Active low. A test point is recommended to be reserved.

When the module is in power down mode, you can turn it on to normal mode by driving the PWRKEY pin low for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

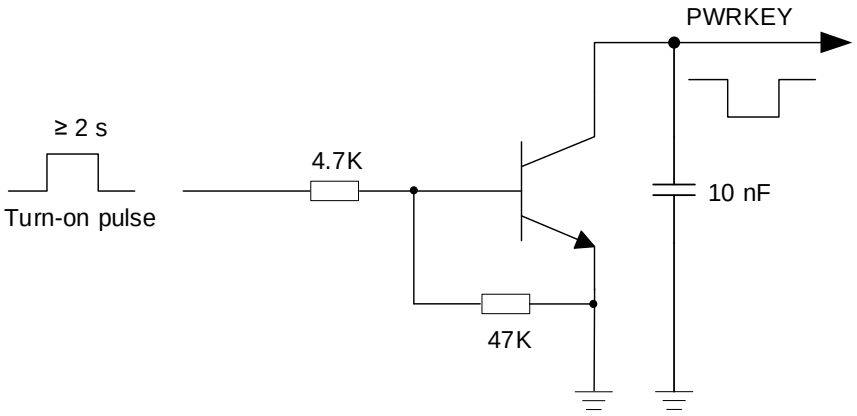


Figure 9: Turning On the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When you are pressing the button, electrostatic strike may be generated from finger. Therefore, you must place a TVS nearby the button for ESD protection. A reference circuit is shown in the following figure.

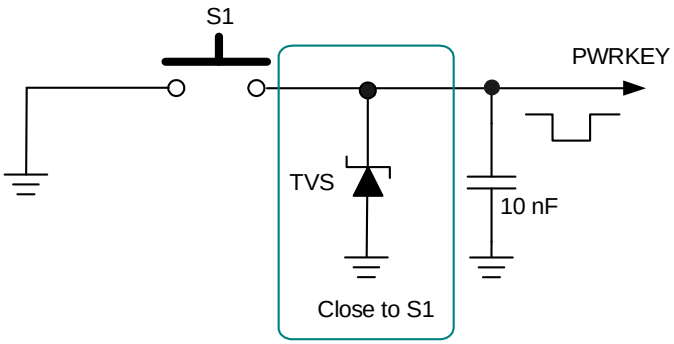


Figure 10: Turning On the Module Using Button

If the module needs to turn on automatically, PWRKEY is connected to GND by connecting a resistor less than 1 kΩ. However, ensure that the voltage of VBAT_BB and VBAT_RF pins is below 0.5 V before power-up.

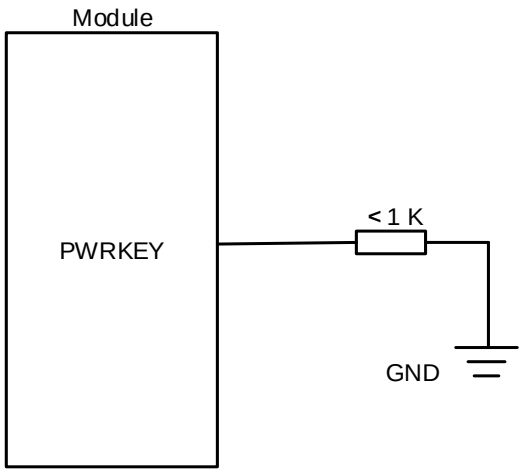


Figure 11: Turning On the Module Automatically

The turn-on timing is illustrated in the following figure.

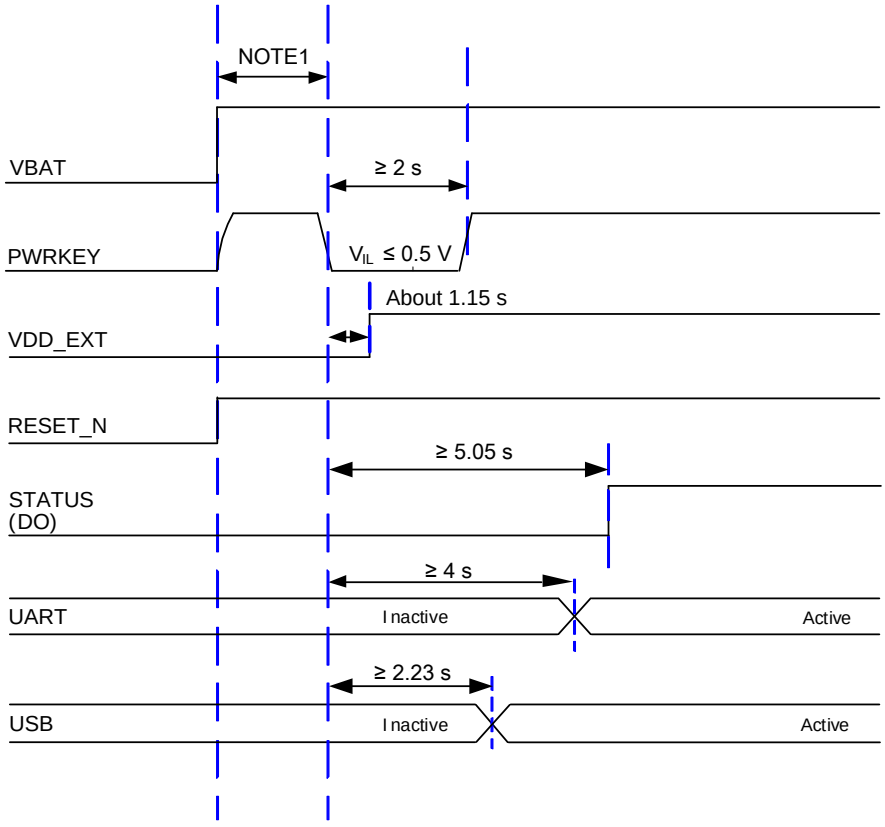


Figure 12: Turn-on Timing

NOTE

1. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. When pulling down PWRKEY to GND by using a resistor, the module will not boot automatically after being turned off with the API function. In this case, it is necessary to forcibly disconnect the VBAT power supply and turn on the module again. Therefore, it is recommended to use a control circuit to control the PWRKEY to turn on/off the module instead of keeping the PWRKEY connected to GND.
3. Pay special attention to the following two power-on scenarios:
   - In the scenario where USB_VBUS is connected first (or has always been connected), VBAT is powered on later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that VBAT is powered on stably for at least 2 s before PERKEY is pulled down;
   - In the scenario where VBAT is powered on first (or has always been powered on), USB_VBUS is connected later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that USB_VBUS is connected for at least 2 s before PWRKEY is pulled down.

3.7. Turn Off

The following methods can be used to turn off the module:

- Use the PWRKEY pin.
- Use *ql_power_down()*. For more details, see ***document [6]***.

3.7.1. Turn Off with PWPKEY

Drive the PWRKEY pin low for at least 3 s and then release PWRKEY, and the module executes power-down procedure. The turn-off timing is illustrated in the following figure.

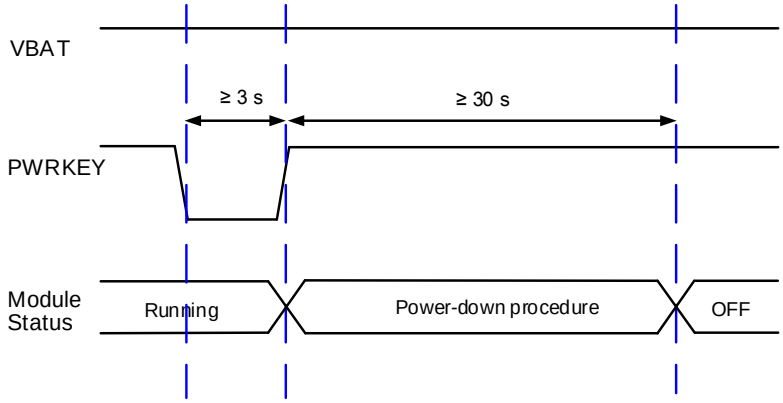


Figure 13: Turn-off Timing

3.7.2. Turn Off with ql_power_down()

It is also a safe way to use *ql_power_down()* to turn off the module, which is similar to turning off the module via the PWRKEY pin.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module with PWRKEY or API function can you cut off the power supply.
2. When being turned off, the module will log out of the network. The time for logging out relates to its network status. Thus, please pay attention to the shutdown time in your design because the actual shutdown time varies according to the network status.

3.8. Reset

The module can be reset by driving the RESET_N pin low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Resets the module	VBAT power domain. Active low. A test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

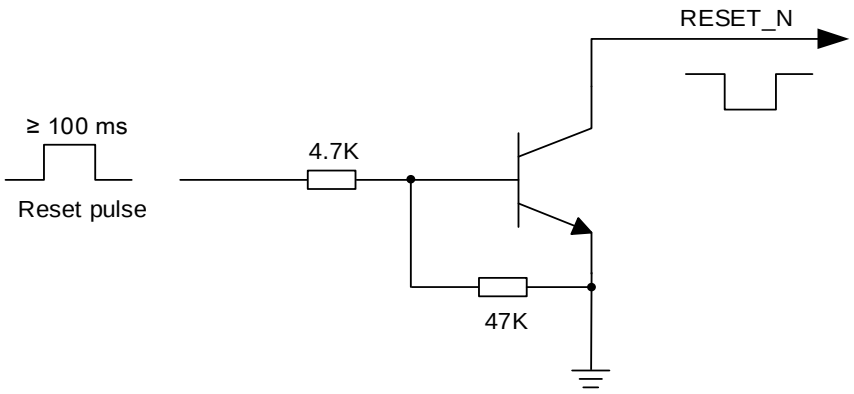


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

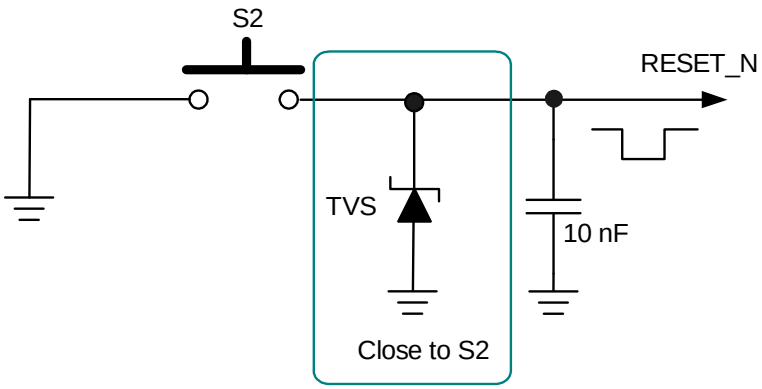


Figure 15: Reference Circuit of RESET_N by Using Button

The reset timing is illustrated in the following figure.

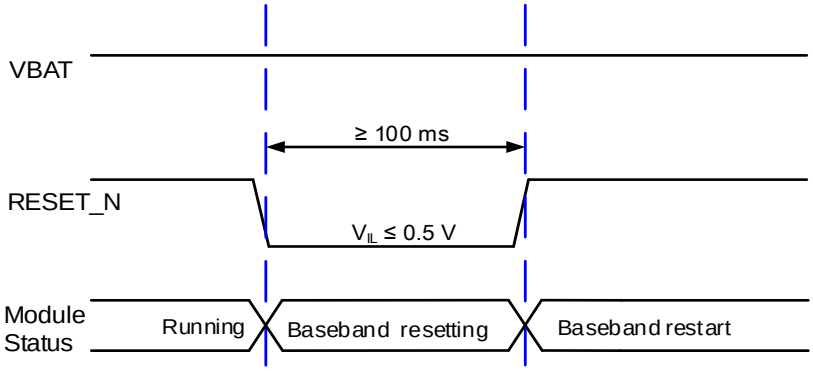


Figure 16: Timing of Resetting the Module

NOTE

1. Ensure that there is no large capacitance exceeding 10 nF on PWRKEY and RESET_N pins.
2. It is recommended to use RESET_N only when you fail to turn off the module with the *ql_power_down()* or PWRKEY pin.

4 Application Interfaces

4.1. Analog Audio Interfaces

The module provides one analog audio input and two analog audio output channels. The pin definition is shown in the following table.

Table 12: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
HP_L	123	AO	Headphone left channel output	If unused, keep them open.
HP_R	124	AO	Headphone right channel output	
HP_DET	125	DI	Headphone hot-plug detection	
SPK_P	121	AO	Analog audio differential output (+)	
SPK_N	122	AO	Analog audio differential output (-)	
MICBIAS	120	PO	Bias voltage output for microphone	
MIC_P	126	AI	Microphone analog input (+)	
MIC_N	119	AI	Microphone analog input (-)	

- AI channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- AO channels are differential output channels. SPK_P/_N can be applied for output of handset, earpiece and loudspeaker. HP_L/_R can be applied for the output of headphone. (The module has no built-in PA, the analog audio output channel SPK_P/_N can be directly used as earpiece, and if connected with an external PA, it can be used as loudspeaker.)

4.1.1. Audio Interface Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required. The filter capacitor on the PCB should be placed near the audio device or audio interface as close as possible, and the trace should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To decrease signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.1.2. Microphone Interface Design

The microphone interface reference circuit is shown in the following figure.

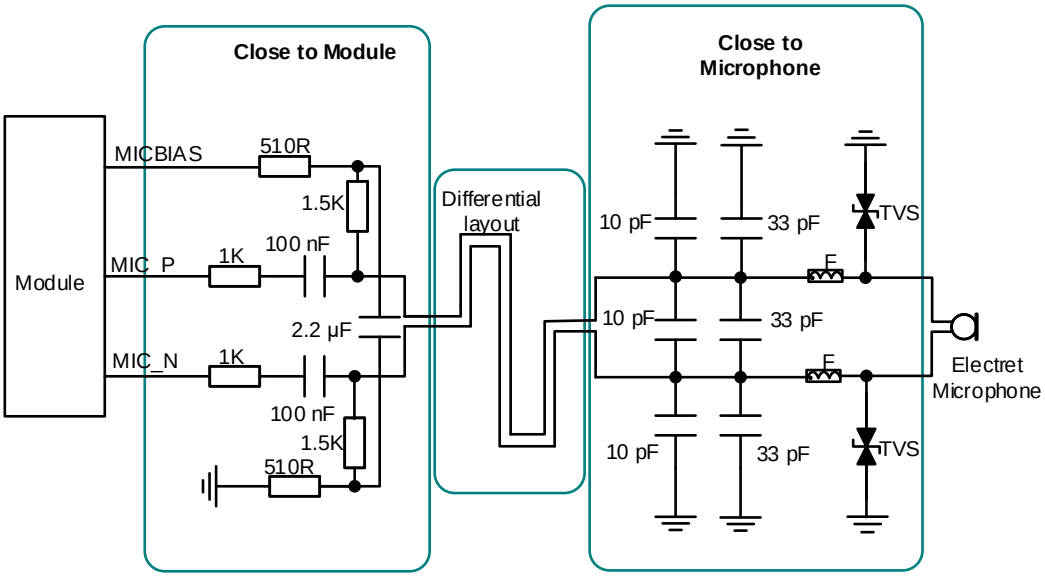


Figure 17: Reference Design for Microphone Interface

NOTE

Microphone channel is sensitive to ESD, so it is not recommended to remove the ESD components.

4.1.3. Earpiece Interface Design

The earpiece interface reference circuit is shown in the following figure:

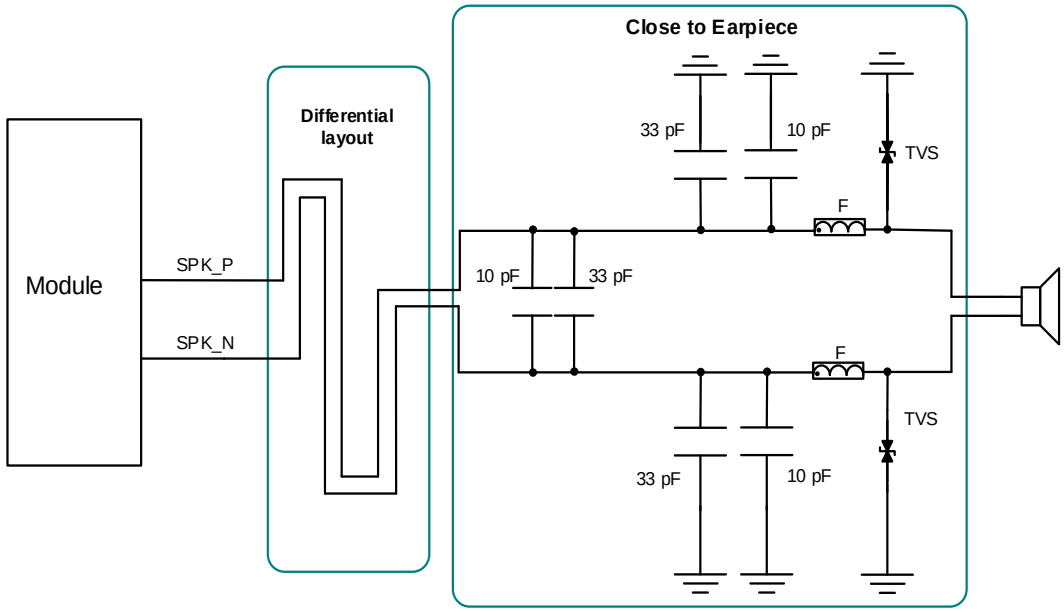


Figure 18: Reference Design for Earpiece Interface

4.1.4. Headphone Interface Design

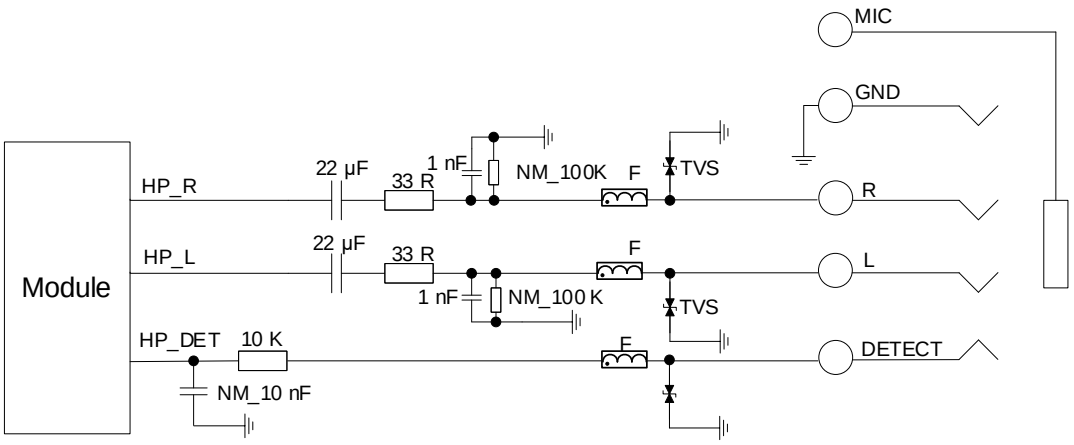


Figure 19: Reference Design for Headphone Interface

4.2. LCM Interface

The LCM interface of the module supports the LCD display with a maximum resolution of 320 × 240 pixel, DMA transmission, as well as 16-bit RGB565 and YUV formats.

Table 13: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_TE	92	DI	LCD tearing effect	1.8 V power domain. If unused, keep them open.
LCD_RST	107	DO	LCD reset	
LCD_SEL	108	DO	Reserved	
LCD_CS	16	DO	LCD SPI chip select	
LCD_SPI_CLK	105	DO	LCD SPI clock	
LCD_SPI_RS	106	DO	LCD SPI register select	
LCD_SPI_DOUT	116	DIO	LCD SPI data	
LCD_ISINK	109	PI	Sink current input. Backlight adjustment	Imax = 200 mA. It is driven by the current sink, connected to the cathode of the backlight, and the brightness can be adjusted with current control.

NOTE

1. The recommended value of LCD digital power LCD_VDDIO should to be designed as Vnom = 1.8 V @ 200 mA.
2. The recommended value of LCD analog power LCD_AVDD should be designed as Vnom = 2.8 V @ 200 mA.

4.3. Camera Interface

The module provides one camera interface supporting cameras up to 0.3 MP and supports SPI two-data-line data transmission.

Table 14: Pin Definition of Camera Interface

Pin Name	Pin No.	I/O	Description	Comment
CAM_I2C_SCL	103	OD	Camera I2C clock	Pull each of them up to 1.8 V power domain with an external resistor. If unused, keep them open.
CAM_I2C_SDA	114	OD	Camera I2C data	
CAM_MCLK	95	DO	Camera master clock	1.8 V power domain. If unused, keep them open.
CAM_SPI_CLK	78	DI	Camera SPI clock	
CAM_SPI_DATA0	97	DI	Camera SPI data bit 0	
CAM_SPI_DATA1	98	DI	Camera SPI data bit 1	
CAM_PWDN	115	DO	Camera power down	
CAM_RST	111	DO	Camera reset	
CAM_VDD	94	PO	Camera analog power supply	Power supply of camera. If unused, keep them open.
CAM_VDDIO	93	PO	Camera digital power supply	

NOTE

If the camera interface is not required, pins 103 and 114 can be used as an I2C interface to connect other peripherals.

4.4. External Flash Interface

The module supports connection to an external flash chip, and the external flash interface is multiplexed from other pins. Pin definition is detailed in the figure below.

Table 15: Pin Definition of the Multiplexed External Flash Interface

Pin Name	Pin No.	Multiplex Function	I/O	DC Characteristics	Description
PCM_SYNC	5	SPI_FLASH1_CS	DO	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	External flash chip select
PCM_CLK	4	SPI_FLASH1_CLK	DO		External flash clock
PCM_DIN	6	SPI_FLASH1_SIO_0	DIO	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	External flash data bit 0
PCM_DOUT	7	SPI_FLASH1_SIO_1	DIO		External flash data bit 1
PSM_IND	1	SPI_FLASH1_SIO_2	DIO		External flash data bit 2
STATUS	20	SPI_FLASH1_SIO_3	DIO		External flash data bit 3

Pins 4–7, 1, 20 can be multiplexed into a set of dedicated SPI for connecting external 6-wire NOR flash or NAND flash. The difference between them is as follows.

- When the dedicated SPI is used for connecting external NOR flash, it supports file system, wear leveling, FOTA upgrade and preset files. It can be used only for storage purpose and cannot be used to run code.
- When the dedicated SPI is used for connecting external NAND flash, it supports basic flash operations such as read, write and erase, file systems and wear leveling. It does not support FOTA upgrade and preset files. It can be used only for storage purpose and cannot be used to run code.

See ***document [7]*** for the design details of the two interface circuits.

NOTE

1. Pins 4–7 can also be multiplexed into a general SPI for connecting external 4-wire flash and other peripherals.
2. For GPIO configuration, see ***document [1]***.

4.5. SD Card Interface

The module provides an SD card interface compliant with SD 2.0 specification. The SD card interface is multiplexed from other pins of the module. Pin definition is detailed in the figure below.

Table 16: Pin Definition of the Multiplexed SD Card Interface

Pin Name	Pin No.	Multiplex Function	I/O	Description	Comment
SD_CLK	110	-	DO	SD card clock	3.2 V power domain. If unused, keep them open.
MAIN_DCD	38	SDIO1_CMD	DIO	SDIO1 command	
MAIN_DTR	30	SDIO1_DATA0	DIO	SDIO1 data bit 0	
MAIN_RI	39	SDIO1_DATA1	DIO	SDIO1 data bit 1	
W_DISABLE#	18	SDIO1_DATA2	DIO	SDIO1 data bit 2	
AP_READY	19	SDIO1_DATA3	DIO	SDIO1 data bit 3	
GPIO5	104	SD_DET	DI	SD card hot-plug detect	1.8 V power domain. If unused, keep it open.

The reference design circuit is shown in the figure below.

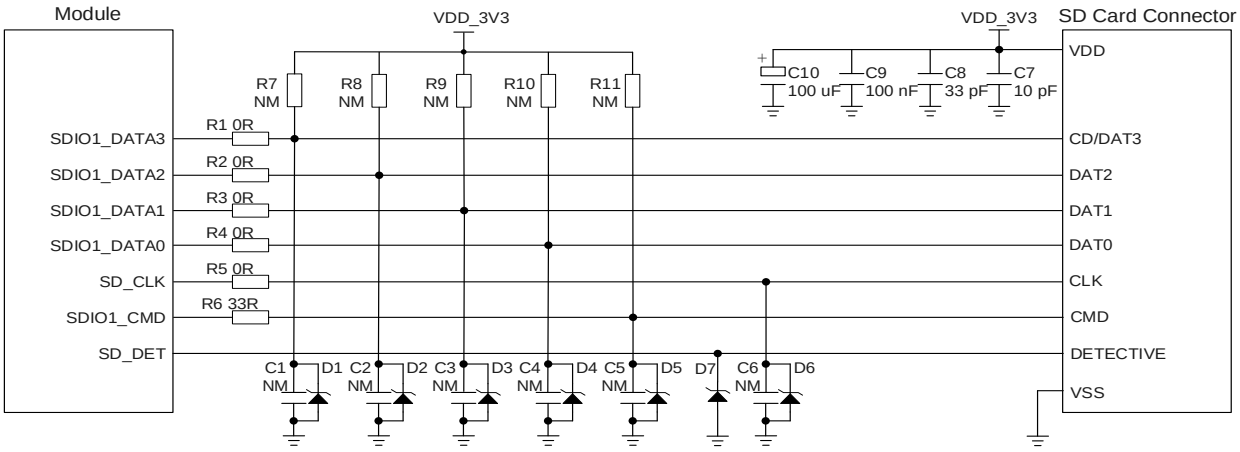


Figure 20: SD Card Interface Reference Design

To ensure good performance and reliability of the SD card, the following principles are recommended in the circuit design of the SD card interface.

- SD card needs to be powered externally. The voltage range of VDD_3V3 is 2.7–3.6 V and it should provide at least 800 mA current. The recommended voltage of VDD_3V3 is 3.2 V.
- To avoid the jitter of bus, it is necessary to reserve pull-up resistors R7–R11 on the SDIO signal traces. The recommended value is 4.7 kΩ and they are not mounted by default. The pull-up power supply can be the external power supply VDD_3V3 whose voltage is 3.2 V.
- To adjust signal quality, it is necessary to add resistors R1–R6 in series between the module and the SD card connector. The recommended value is 0 Ω for R1–R5 and 33 Ω for R6. The bypass capacitors C1–C6 are reserved and not mounted by default. The resistors and capacitors should be placed close to the module when placing the PCB.
- For good ESD protection, it is recommended to add a TVS to each SD card pin, and place them as close to the SD card connector as possible. The parasitic capacitance of TVS should be less than 15 pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noise signals such as clock and DC-DC signals.
- Route SDIO signals with ground surrounded. The impedance of SDIO data trace should be kept at 50 Ω ±10 %.
- Keep the space between SDIO signal traces and other signal traces greater than twice the trace width and ensure that the bus capacitance is less than 15 pF.
- Keep the trace length difference among SDIO1_CLK, SDIO1_DATA[0:3] and SDIO1_CMD less than 1 mm and the total routing length should be less than 50 mm.

NOTE

1. When using pins 18, 19, 30, 38, 39, and 110, please note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.
2. For GPIO configuration, see ***document [1]***.

4.6. USB Interface

The module provides an integrated Universal Serial Bus (USB) interface compliant with the USB 2.0 specification and supporting full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve as a slave device.

Table 17: Functions of USB Interface

Function	
Data transmission	√
Software debugging	√
Firmware upgrade	√

The following table shows the pin definition of USB interface.

Table 18: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	3.5 V–5.25 V. A test point must be reserved.
USB_DP	9	AIO	USB 2.0 differential data (+)	USB 2.0 compliant. Requires 90 Ω differential impedance. Test points must be reserved.
USB_DM	10	AIO	USB 2.0 differential data (-)	

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

Reserve test points for debugging and firmware upgrade in your designs. The following figure shows a reference circuit of USB interface.

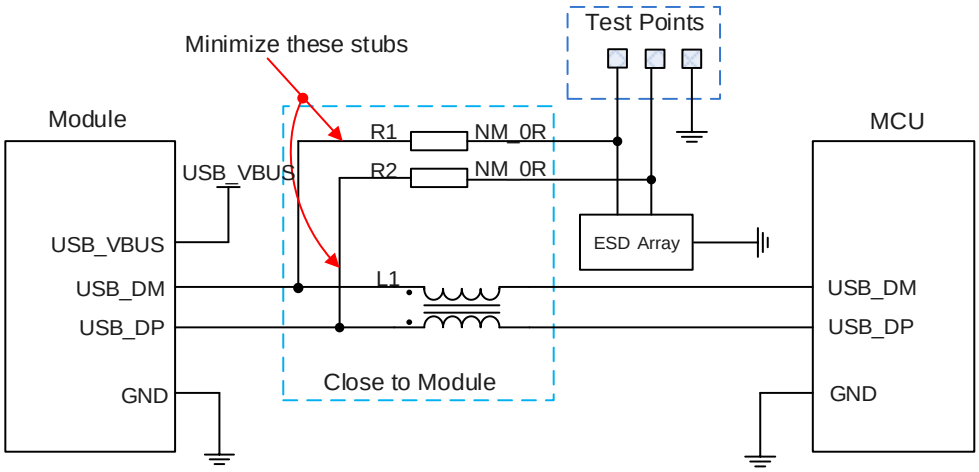


Figure 21: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. To ensure the signal integrity of USB data lines, L1, R1, and R2 must be placed close to the module, and resistors R1 and R2 should be placed close to each other. The extra stubs of trace must be as short as possible.

When designing the USB interface, you should follow the following principles to meet USB 2.0 specification.

- Route the USB signal traces as differential pairs in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under or near crystals, oscillators, magnetic devices, and RF signal traces.
- Pay attention to the selection of the ESD component on the USB data line. Its stray capacitance should not exceed 2 pF and should be placed as close as possible to the USB connector.

4.7. USB_BOOT Interface

The module provides a USB_BOOT interface. You can pull up USB_BOOT to VDD_EXT before power-up and the module will enter download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 19: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module into emergency download mode	1.8 V power domain. Active high. A circuit that can set the module into emergency download mode should be reserved during design. A test point is recommended to be reserved.

The following figure shows a reference circuit of USB_BOOT interface.

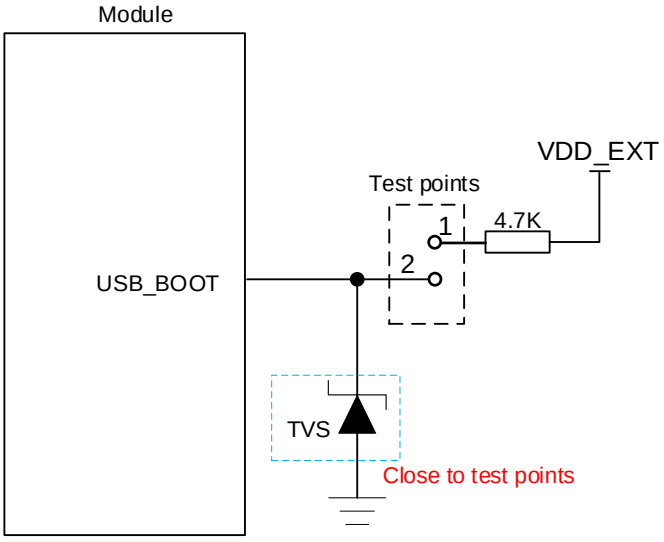


Figure 22: Reference Circuit of USB_BOOT Interface

4.8. (U)SIM Interfaces

The module provides two (U)SIM interfaces that supports Dual SIM Single Standby. The (U)SIM interfaces circuitry meets ETSI requirement and IMT-2000 specification. Either 1.8 V or 3.0 V (U)SIM card is supported.

Table 20: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM1_GND	47	-	Ground	Specified ground for (U)SIM1 card.
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified

				automatically by the module.
USIM2_DATA	86	DIO	(U)SIM2 card data	
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. A test point must be reserved for debugging.

The module supports (U)SIM card hot-plug via the USIM1_DET and USIM2_DET pins and both high- and low-level detections are supported. See ***document [8]*** for details on configuring the hot-plug detection function.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

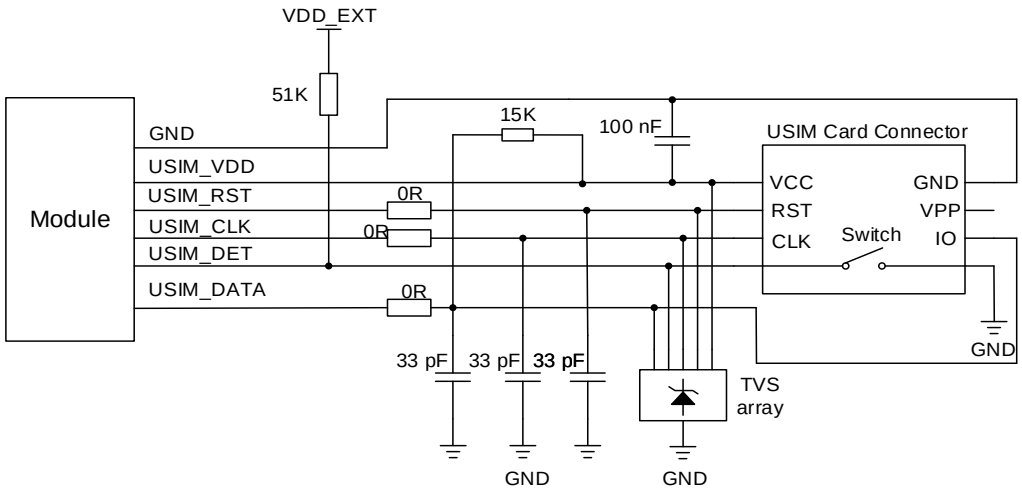


Figure 23: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

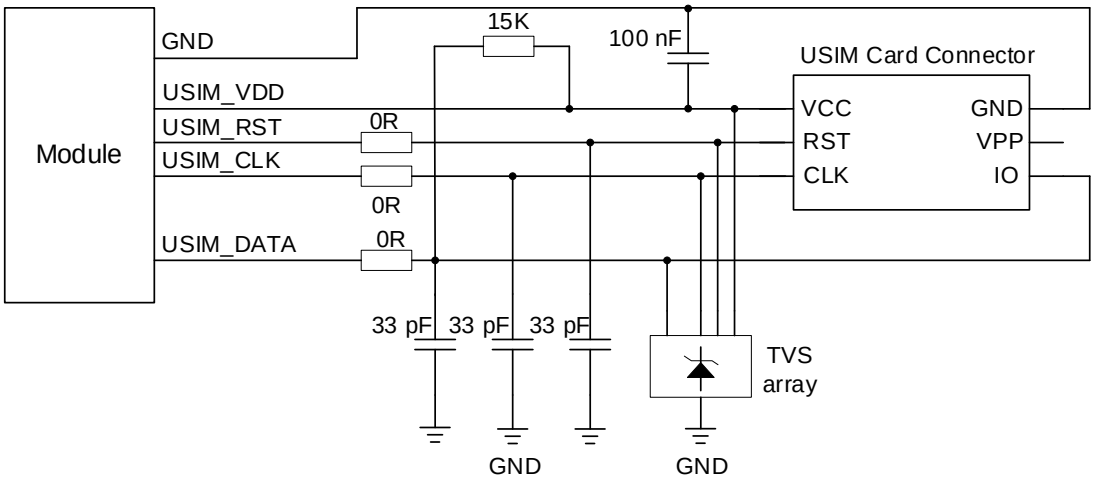


Figure 24: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Place (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM signals away from RF and VBAT traces.
- Ensure the bypass capacitor between USIM_VDD and GND does not exceed 1 µF, and the capacitor should be close to the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

4.9. PCM and I2C Interfaces

The module provides one pulse code modulation (PCM) interface and one I2C interface. The PCM interface only supports slave mode; therefore, the clock signal of the codec IC needs to be provided externally.

PCM interface supports the short frame mode. In short frame mode, PCM_CLK = the number of channels × PCM_SYNC × 16 bit, where the number of channels supports 1–4 channels, but the module will only take the data on the first channel; PCM_SYNC is equal to the audio sampling rate, which supports 8–44.1 kHz.

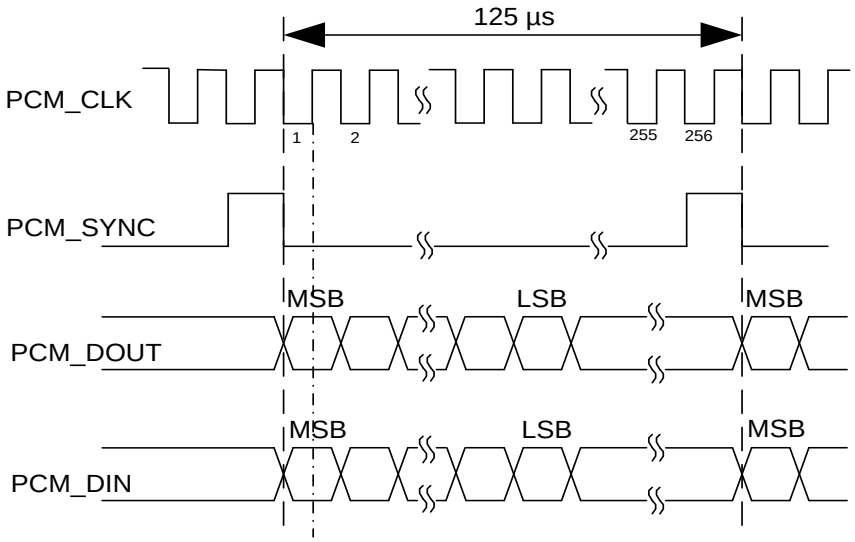


Figure 23: Timing of PCM Mode

NOTE

The clocks of PCM_SYNC and PCM_CLK are provided by the external codec IC, but the provided PCM_SYNC frequency must be equal to the sampling frequency of the audio file played by the module.

Table 21: Pin Definition of I2C and PCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	40	OD	I2C serial clock	1.8 V power domain. They need to be pulled up to 1.8 V externally. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data	
PCM_DIN	6	DI	PCM data input	1.8 V power domain. If unused, keep them open. Supports slave mode only.
PCM_DOUT	7	DO	PCM data output	
PCM_SYNC	5	DI	PCM data frame sync	
PCM_CLK	4	DI	PCM clock	

The following figure shows a reference design of I2C and PCM interfaces with an external codec IC.

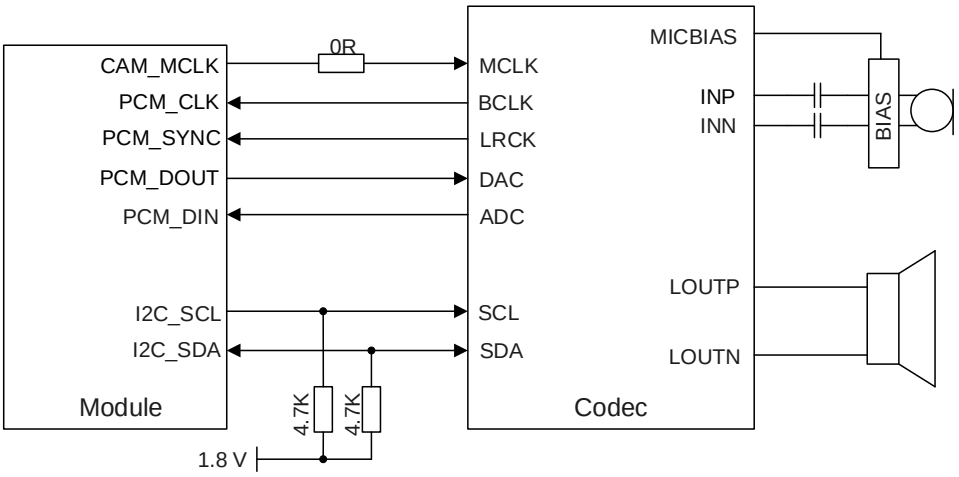


Figure 25: Reference Circuit of I2C and PCM Application with Audio Codec

NOTE

1. It is recommended to reserve a termination resistor and a filter capacitor on the PCM traces (especially on CAM_MCLK and PCM_CLK traces).
2. The I2C interface supports simultaneous connection of multiple peripherals except for codec IC. In other words, if a codec IC has been mounted on the I2C bus, no other peripherals can be mounted; if there is no codec IC on the bus, multiple peripherals can be mounted.

4.10. UART Interfaces

The module provides three UART interfaces: main UART, debug UART, and auxiliary UART.

- Main UART interface supports baud rates 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, and 921600 bps, and the default is 115200 bps. It supports RTS and CTS hardware flow control. This interface is used for data transmission.
- Debug UART interface supports 921600 bps baud rate. It is used for log output. It cannot be used as a general-purpose UART.
- Auxiliary UART interface supports the same baud rates as the main UART interface.

Table 22: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	36	DO	Clear to send signal from the module	Connect to MCU's CTS. 1.8 V power domain. If unused, keep it open.
MAIN_RTS	37	DI	Request to send signal to the module	Connect to MCU's RTS. 1.8 V power domain. If unused, keep it open.
MAIN_RXD	34	DI	Main UART receive	1.8 V power domain. If unused, keep them open.
MAIN_TXD	35	DO	Main UART transmit	

Table 23: Pin Definition of Auxiliary UART Interface

Pin Name	Pin No.	I/O	Description	Comment
AUX_TXD	27	DO	Auxiliary UART transmit	1.8 V power domain. If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive	

Table 24: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain. Test points must be reserved for debugging.
DBG_TXD	23	DO	Debug UART transmit	

The module provides a 1.8 V UART interface. A level-shifting circuit should be used if the application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0104EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

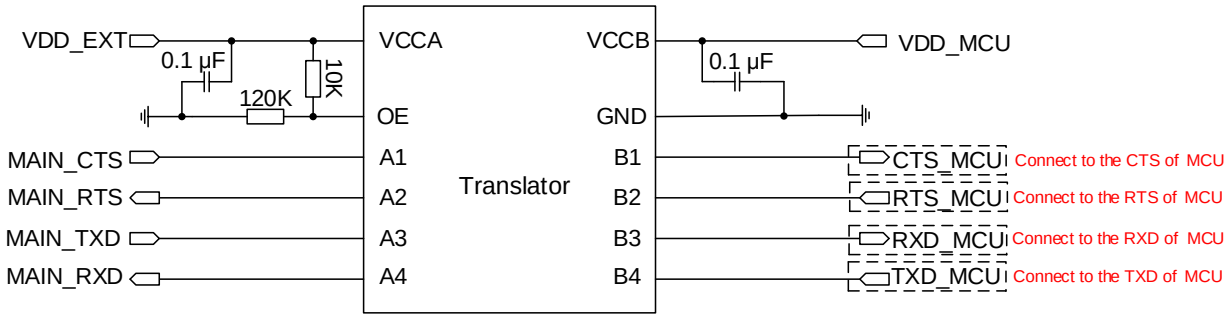


Figure 26: Reference Circuit with Voltage-level Translator

Please visit http://www.ti.com for more information.

Another example with transistor circuit is shown as follows. For the design of circuits in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

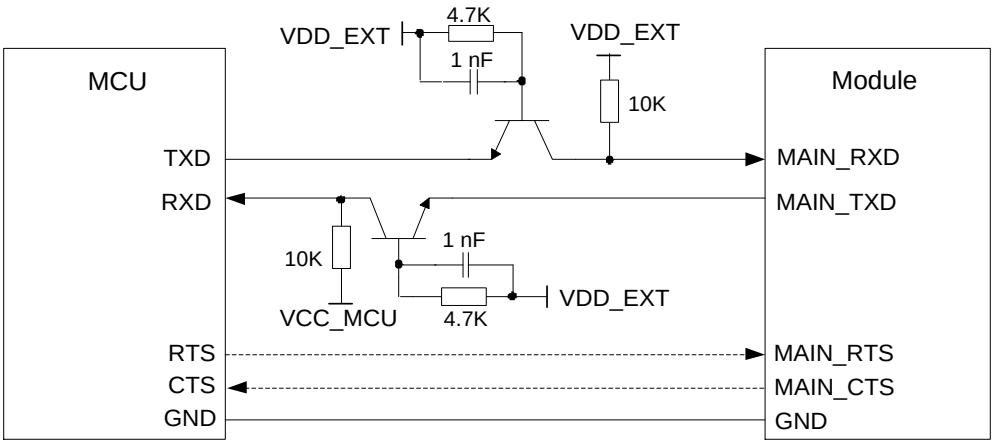


Figure 27: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.

4.11. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. To improve the measurement accuracy of ADC, surround the traces of ADC with ground.

Table 25: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interfaces	If unused, keep them open.
ADC1	2	AI		

Table 26: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	VBAT	V
ADC1 Voltage Range	0	-	VBAT	V
ADC Resolution	-	12	-	bits

You can call *ql_adc_get_volt()* to read the voltage of an ADC interface. The mapping between *ql_adc_channel_id* and an ADC channel is as follows. For more details, see ***document [9]***.

Table 27: Mapping between *q_adc_channel_id* and ADC Channel

ql_adc_channel_id	ADC Channel
QL_ADC0_CHANNEL	ADC0
QL_ADC1_CHANNEL	ADC1

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. Do not supply any voltage to ADC pins when VBAT is removed.
3. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins, it is strongly recommended to reserve the voltage divider circuit for better compatibility with other Quectel modules. The resistance of the divider must be less than 100 kΩ,

otherwise the measurement accuracy of the ADC will be significantly reduced. When the divider circuit is not used, the ADC pins require 1 kΩ resistors in series.

4.12. SPI

The module provides an SPI that only supports master mode. It has a working voltage of 1.8 V and a maximum clock frequency of 25 MHz.

Table 28: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	1.8 V power domain. If unused, keep them open. Supports master mode only.
SPI_CS	25	DO	SPI chip select	
SPI_DIN	88	DI	SPI data input	
SPI_DOUT	64	DO	SPI data output	

NOTE

1. When the general 4-wire SPI is used for connecting external NOR flash, it supports basic flash operations such as read, write and erase, file systems, wear leveling, FOTA upgrade and preset files. It can be used only for storage purpose and cannot be used to run code.
2. When the general 4-wire SPI is used for connecting external NAND flash, it supports basic flash operations such as read, write and erase, file systems and wear leveling. It does not support FOTA upgrade and preset files. It can be used only for storage purpose and cannot be used to run code.

4.13. Indication Signals

The module provides two indication pins STATUS and NET_STATUS, which are mainly used for driving external indicators. The following tables describe pin definition and working states in different network status. See *led_cfg-demo.c* in the CSDK for details.

Table 29: Pin Definition of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicates the module's operation status	1.8 V power domain. If unused, keep them open.
NET_STATUS	21	DO	Indicates the module's network activity status	

Table 30: Working States of Indication Pins

Pin Name	State	Network Status
STATUS	Always high	Power on
	Always low	Power off
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker quickly (234 ms high/266 ms low)	Registered on network and idle
	Flicker rapidly (63 ms high /62 ms low)	Data transfer is ongoing
	Always high	Voice calling

The reference circuits are shown as follows.

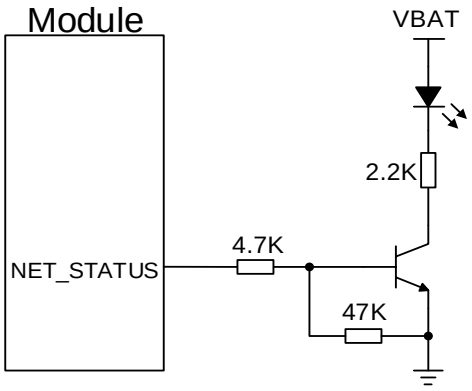


Figure 28: Reference Circuit of NET_STATUS

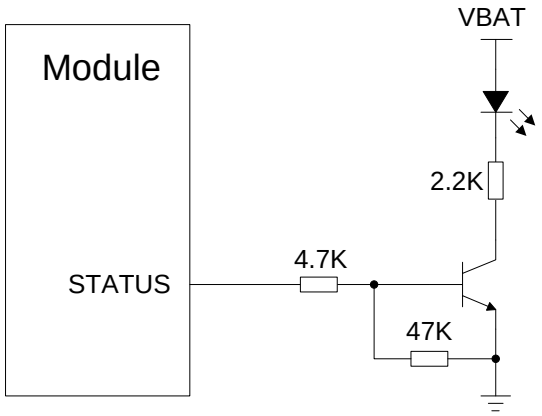


Figure 29: Reference Circuit of STATUS

5 Antenna Interfaces

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module provides a main antenna interface and a Bluetooth/Wi-Fi Scan antenna interface.

5.1. Main Antenna and Bluetooth/Wi-Fi Scan Antenna Interfaces

5.1.1. Pin Definition

Table 31: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω characteristic impedance.
ANT_BT/WIFI_SCAN	56	AIO	The shared interface for Bluetooth and Wi-Fi Scan	Bluetooth and Wi-Fi Scan cannot be used simultaneously. Wi-Fi Scan only supports receiving. 50 Ω characteristic impedance. If unused, keep it open.

5.1.2. Operating Frequency

Table 32: Operating Frequency of EG915U-CN (Unit: MHz)

Operating Frequency	Transmit	Receive
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B8	880–915	925–960
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

Table 33: Operating Frequency of EG915U-EU (Unit: MHz)

Operating Frequency	Transmit	Receive
GSM850	824–849	869–894
PCS1900	1850–1910	1930–1990
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894

LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803

Table 34: Operating Frequency of EG915U-LA (Unit: MHz)

Operating Frequency	Transmit	Receive
GSM850	824–849	869–894
PCS1900	1850–1910	1930–1990
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710–1780	2110–2180

NOTE

Only EG915U-CN supports LTE-TDD.

5.1.3. Reference Design of Antenna Interfaces

A reference design of ANT_MAIN pin and ANT_BT/WIFI_SACN pin are shown as below. A π-type matching circuit and ESD protection device should be reserved for better RF performance. The capacitors are not mounted by default.

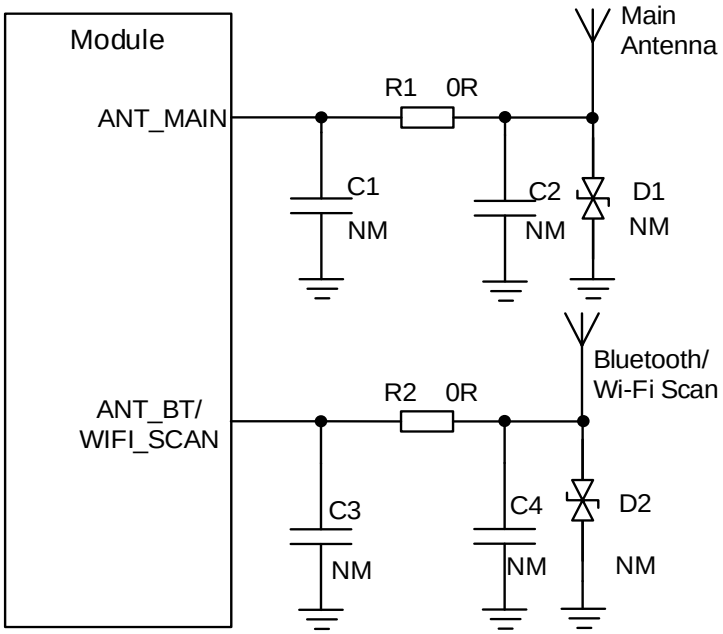


Figure 30: Reference Circuit of RF Antennas

NOTE

1. To improve receiver sensitivity, ensure that the clearance among antennas is appropriate.
2. Place the π-type matching components (R1, C1, C2 and R2, C3, C4) to antennas as close as possible.

5.1.4. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between the RF traces and the ground (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

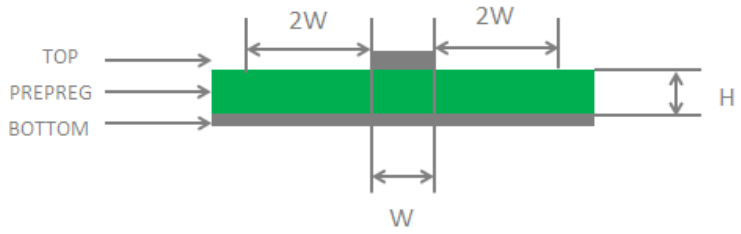


Figure 31: Microstrip Design on a 2-layer PCB

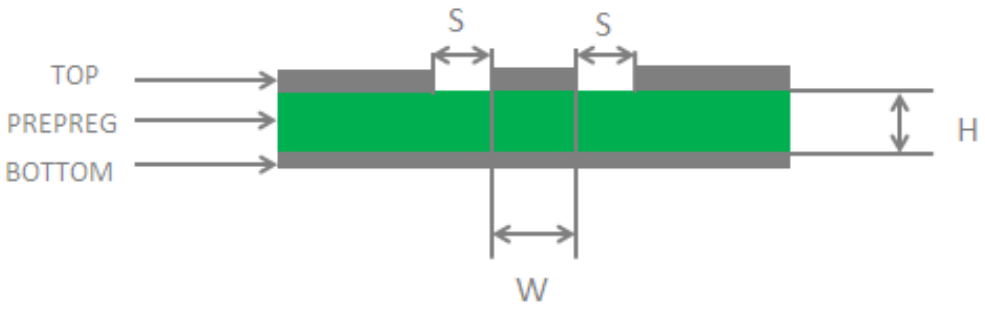


Figure 32: Coplanar Waveguide Design on a 2-layer PCB

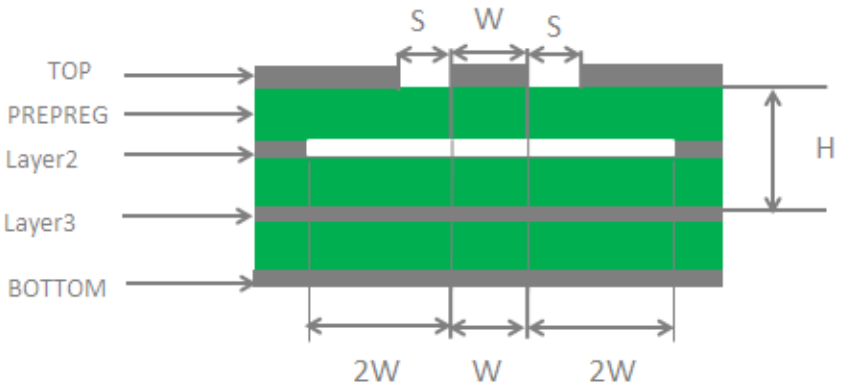


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

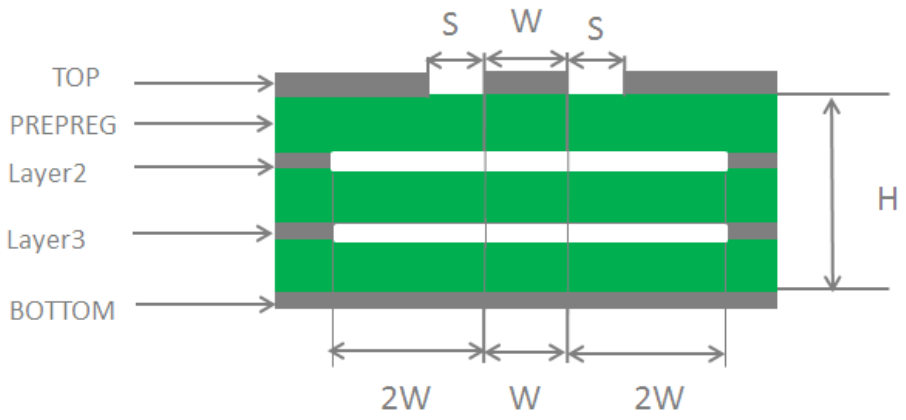


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [10]***.

5.2. Antenna Installation

5.2.1. Antenna Design Requirements

Table 35: Antenna Design Requirements

Type	Requirement
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max. input power: 50 W Input impedance: 50 Ω Cable insertion loss: < **1 dB:** LB (< 1 GHz) < **1.5 dB:** MB (1–2.3 GHz) < **2 dB:** HB (> 2.3 GHz)

5.2.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

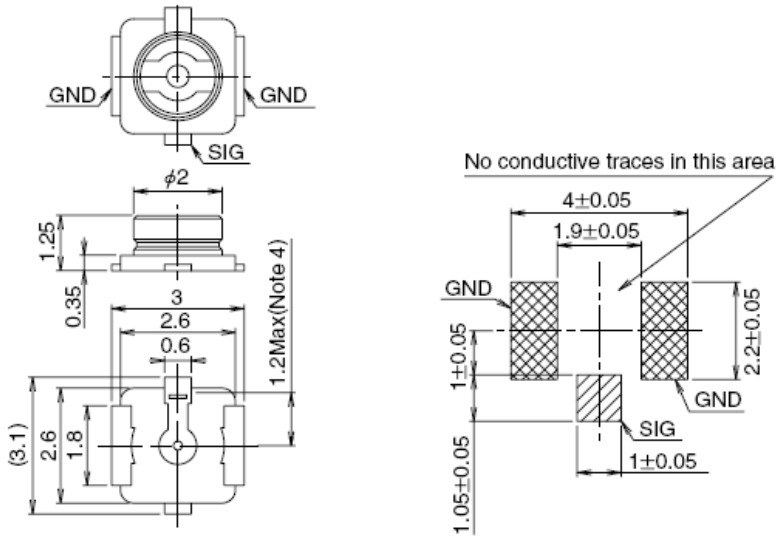


Figure 35: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

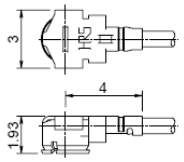
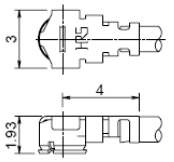
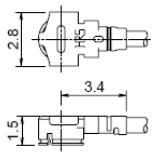
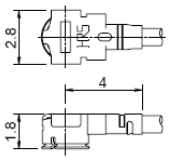
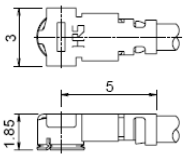
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 36: Specifications of Mated Plugs

The following figure describes the space factor of mated connector.

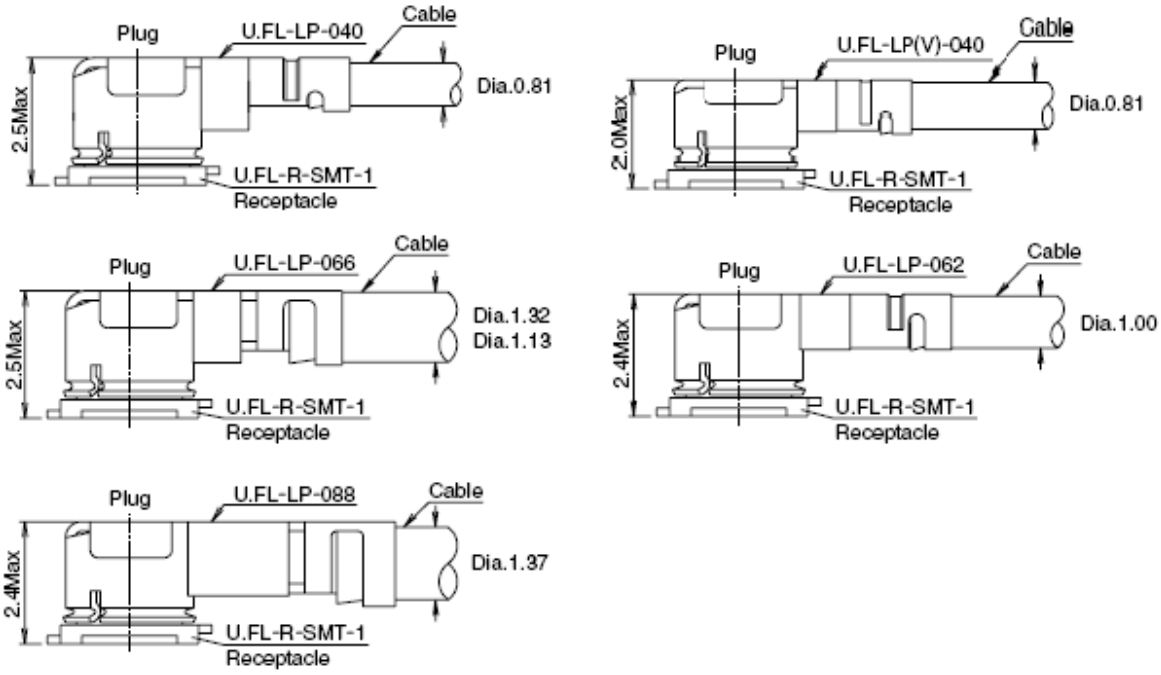


Figure 37: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Table 36: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	1	A
Peak Current of VBAT_RF	-	2.5	A
Voltage on Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT	V
Voltage at ADC1	0	VBAT	V

6.2. Power Supply Ratings

Table 37: Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during transmitting burst	Maximum power control level	-	-	400	mV
I_{VBAT}	Peak supply current	Maximum power control level	-	1.7	2.5	A

USB_VBUS	USB connection detection	-	3.5	5.0	5.25	V

6.3. Power Consumption

Table 38: EG915U-CN Current Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	32	μA
Sleep state	Minimum Functionality Mode (USB disconnected)	1.0	mA
	Minimum Functionality Mode (USB connected)	2.2	
	Airplane Mode (USB disconnected)	1.0	
	Airplane Mode (USB connected)	2.3	
	EGSM900 @ DRX = 2 (USB disconnected)	2.0	
	EGSM900 @ DRX = 5 (USB disconnected)	1.5	
	EGSM900 @ DRX = 5 (USB connected)	2.7	
	EGSM900 @ DRX = 9 (USB disconnected)	1.3	
	DCS1800 @ DRX = 2 (USB disconnected)	2.0	
	DCS1800 @ DRX = 5 (USB disconnected)	1.5	
	DCS1800 @ DRX = 5 (USB connected)	2.7	
	DCS1800 @ DRX = 9 (USB disconnected)	1.3	
	LTE-FDD @ PF = 32 (USB disconnected)	2.5	
	LTE-FDD @ PF = 64 (USB disconnected)	1.8	
	LTE-FDD @ PF = 64 (USB connected)	3.0	
	LTE-FDD @ PF = 128 (USB disconnected)	1.4	
	LTE-FDD @ PF = 256 (USB disconnected)	1.2	
	LTE-TDD @ PF = 32 (USB disconnected)	2.5	

	LTE-TDD @ PF = 64 (USB disconnected)	1.8	
	LTE-TDD @ PF = 64 (USB connected)	3.1	
	LTE-TDD @ PF = 128 (USB disconnected)	1.4	
	LTE-TDD @ PF = 256 (USB disconnected)	1.2	
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	12.6	mA
	EGSM900 @ DRX = 5 (USB connected)	28.6	
	LTE-FDD @ PF = 64 (USB disconnected)	13.0	
	LTE-FDD @ PF = 64 (USB connected)	29.0	
	LTE-TDD @ PF = 64 (USB disconnected)	13.0	
	LTE-TDD @ PF = 64 (USB connected)	29.0	
LTE data transfer	LTE-FDD B1 @ 22.94 dBm	587	mA
	LTE-FDD B3 @ 23.01 dBm	615	
	LTE-FDD B5 @ 23.54 dBm	527	
	LTE-FDD B8 @ 22.83 dBm	564	
	LTE-TDD B34 @ 23.14 dBm	280	
	LTE-TDD B38 @ 23.34 dBm	326	
	LTE-TDD B39 @ 23.25 dBm	247	
	LTE-TDD B40 @ 23.81 dBm	297	
	LTE-TDD B41 @ 23.06 dBm	311	
GPRS data transfer	EGSM900 4DL/1UL @ 32.87 dBm	234	mA
	EGSM900 3DL/2UL @ 30.86 dBm	348	
	EGSM900 2DL/3UL @ 28.90 dBm	401	
	EGSM900 1DL/4UL @ 26.74 dBm	415	
	DCS1800 4DL/1UL @ 30.13 dBm	160	
	DCS1800 3DL/2UL @ 28.12 dBm	221	
	DCS1800 2DL/3UL @ 26.01 dBm	249	

	DCS1800 1DL/4UL @ 23.94 dBm	258	
GSM voice call	EGSM900 PCL = 5 @ 32.89 dBm	256	mA
	EGSM900 PCL = 12 @ 19.41 dBm	101	
	EGSM900 PCL = 19 @ 6.33 dBm	72	
	DCS1800 PCL = 0 @ 29.99 dBm	178	
	DCS1800 PCL = 7 @ 16.09 dBm	84	
	DCS1800 PCL = 15 @ 1.26 dBm	67	
GSM voice call (Max. Current)	EGSM900 PCL = 5 @ 32.83 dBm	1.78	A
	EGSM900 PCL = 12 @ 18.94 dBm	0.45	
	EGSM900 PCL = 19 @ 6.18 dBm	0.19	
	DCS1800 PCL = 0 @ 30.12 dBm	1.11	
	DCS1800 PCL = 7 @ 15.97 dBm	0.30	
	DCS1800 PCL = 15 @ 0.28 dBm	0.15	

Table 39: EG915U-EU Current Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	32	μA
Sleep state	Minimum Functionality Mode (USB disconnected)	1.1	mA
	Minimum Functionality Mode (USB connected)	2.3	
	Airplane Mode (USB disconnected)	1.2	
	Airplane Mode (USB connected)	2.4	
	EGSM900 @ DRX = 2 (USB disconnected)	2.1	
	EGSM900 @ DRX = 5 (USB disconnected)	1.8	
	EGSM900 @ DRX = 5 (USB connected)	2.8	
	EGSM900 @ DRX = 9 (USB disconnected)	1.5	
	DCS1800 @ DRX = 2 (USB disconnected)	2.1	

	DCS1800 @ DRX = 5 (USB disconnected)	1.8	
	DCS1800 @ DRX = 5 (USB connected)	2.7	
	DCS1800 @ DRX = 9 (USB disconnected)	1.5	
	LTE-FDD @ PF = 32 (USB disconnected)	2.7	
	LTE-FDD @ PF = 64 (USB disconnected)	2.1	
	LTE-FDD @ PF = 64 (USB connected)	3.3	
	LTE-FDD @ PF = 128 (USB disconnected)	1.6	
	LTE-FDD @ PF = 256 (USB disconnected)	1.5	
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	12.5	mA
	EGSM900 @ DRX = 5 (USB connected)	28.1	
	LTE-FDD @ PF = 64 (USB disconnected)	12.5	
	LTE-FDD @ PF = 64 (USB connected)	28.1	
LTE data transfer	LTE-FDD B1 @ 22.44 dBm	595	mA
	LTE-FDD B3 @ 22.74 dBm	657	
	LTE-FDD B5 @ 22.17 dBm	567	
	LTE-FDD B7 @ 22.01 dBm	774	
	LTE-FDD B8 @ 22.01 dBm	533	
	LTE-FDD B20 @ 22.92 dBm	522	
	LTE-FDD B28 @ 22.56 dBm	526	
GPRS data transfer	GSM850 4DL/1UL @ 32.57 dBm	247	mA
	GSM850 3DL/2UL @ 30.53 dBm	365	
	GSM850 2DL/3UL @ 28.32 dBm	414	
	GSM850 1DL/4UL @ 26.07 dBm	430	
	EGSM900 4DL/1UL @ 32.13 dBm	234	
	EGSM900 3DL/2UL @ 30.45 dBm	355	

	EGSM900 2DL/3UL @ 28.37 dBm	408	
	EGSM900 1DL/4UL @ 26.33 dBm	427	
	DCS1800 4DL/1UL @ 29.42 dBm	155	
	DCS1800 3DL/2UL @ 27.95 dBm	227	
	DCS1800 2DL/3UL @ 25.89 dBm	253	
	DCS1800 1DL/4UL @ 23.79 dBm	259	
	PCS1900 4DL/1UL @ 29.89 dBm	163	
	PCS1900 3DL/2UL @ 27.78 dBm	230	
	PCS1900 2DL/3UL @ 25.86 dBm	260	
	PCS1900 1DL/4UL @ 23.70 dBm	271	
GSM voice call	GSM850 PCL = 5 @ 32.62 dBm	256	mA
	GSM850 PCL = 12 @ 18.71 dBm	91	
	GSM850 PCL = 19 @ 5.04 dBm	60	
	EGSM900 PCL = 5 @ 32.11 dBm	249	
	EGSM900 PCL = 12 @ 18.76 dBm	100	
	EGSM900 PCL = 19 @ 5.30 dBm	69	
	DCS1800 PCL = 0 @ 29.43 dBm	171	
	DCS1800 PCL = 7 @ 15.91 dBm	81	
	DCS1800 PCL = 15 @ 0.21 dBm	63	
	PCS1900 PCL = 0 @ 29.88 dBm	179	
	PCS1900 PCL = 7 @ 16.03 dBm	83	
	PCS1900 PCL = 15 @ 0.72 dBm	64	
GSM voice call (Max. Current)	GSM850 PCL = 5 @ 32.82 dBm	1.88	A
	GSM850 PCL = 12 @ 19.08 dBm	0.46	
	GSM850 PCL = 19 @ 6.12 dBm	0.19	

	EGSM900 PCL = 5 @ 32.34 dBm	1.72
	EGSM900 PCL = 12 @ 19.06 dBm	0.44
	EGSM900 PCL = 19 @ 5.39 dBm	0.19
	DCS1800 PCL = 0 @ 29.89 dBm	1.13
	DCS1800 PCL = 7 @ 15.96 dBm	0.30
	DCS1800 PCL = 15 @ 0.95 dBm	0.16
	PCS1900 PCL = 0 @ 29.66 dBm	1.10
	PCS1900 PCL = 7 @ 15.59 dBm	0.33
	PCS1900 PCL = 15 @ 0.58 dBm	0.15

Table 40: EG915U-LA Current Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	32	μA
Sleep state	Minimum Functionality Mode (USB disconnected)	0.94	mA
	Minimum Functionality Mode (USB connected)	2.39	
	Airplane Mode (USB disconnected)	1.02	
	Airplane Mode (USB connected)	2.45	
	EGSM900 @ DRX = 2 (USB disconnected)	1.98	
	EGSM900 @ DRX = 5 (USB disconnected)	1.41	
	EGSM900 @ DRX = 5 (USB connected)	2.86	
	EGSM900 @ DRX = 9 (USB disconnected)	1.28	
	DCS1800 @ DRX = 2 (USB disconnected)	1.95	
	DCS1800 @ DRX = 5 (USB disconnected)	1.44	
	DCS1800 @ DRX = 5 (USB connected)	2.85	
	DCS1800 @ DRX = 9 (USB disconnected)	1.25	
	LTE-FDD @ PF = 32 (USB disconnected)	2.55	

	LTE-FDD @ PF = 64 (USB disconnected)	1.80	
	LTE-FDD @ PF = 64 (USB connected)	3.24	
	LTE-FDD @ PF = 128 (USB disconnected)	1.41	
	LTE-FDD @ PF = 256 (USB disconnected)	1.23	
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	12.11	mA
	EGSM900 @ DRX = 5 (USB connected)	27.26	
	LTE-FDD @ PF = 64 (USB disconnected)	12.33	
	LTE-FDD @ PF = 64 (USB connected)	27.65	
LTE data transfer	LTE-FDD B2 @ 22.93 dBm	610	mA
	LTE-FDD B3 @ 23.27 dBm	641	
	LTE-FDD B4 @ 23.27 dBm	766	
	LTE-FDD B5 @ 22.84 dBm	608	
	LTE-FDD B7 @ 22.65 dBm	747	
	LTE-FDD B8 @ 23.58 dBm	609	
	LTE-FDD B28 @ 23.75 dBm	587	
	LTE-FDD B66 @ 23.48 dBm	667	
GPRS data transfer	GSM850 4DL/1UL @ 32.47 dBm	241	mA
	GSM850 3DL/2UL @ 30.60 dBm	366	
	GSM850 2DL/3UL @ 28.53 dBm	422	
	GSM850 1DL/4UL @ 26.35 dBm	438	
	EGSM900 4DL/1UL @ 32.17 dBm	231	
	EGSM900 3DL/2UL @ 30.60 dBm	359	
	EGSM900 2DL/3UL @ 28.44 dBm	437	
	EGSM900 1DL/4UL @ 26.44 dBm	437	
	DCS1800 4DL/1UL @ 29.56 dBm	146	
	DCS1800 3DL/2UL @ 28.80 dBm	233	

	DCS1800 2DL/3UL @ 26.79 dBm	267	
	DCS1800 1DL/4UL @ 24.79 dBm	276	
	PCS1900 4DL/1UL @ 29.51 dBm	144	
	PCS1900 3DL/2UL @ 28.36 dBm	230	
	PCS1900 2DL/3UL @ 26.30 dBm	260	
	PCS1900 1DL/4UL @ 24.22 dBm	271	
GSM voice call	GSM850 PCL = 5 @ 32.82 dBm	288	mA
	GSM850 PCL = 12 @ 19.08 dBm	113	
	GSM850 PCL = 19 @ 6.12 dBm	80	
	EGSM900 PCL = 5 @ 32.34 dBm	261	
	EGSM900 PCL = 12 @ 19.06 dBm	112	
	EGSM900 PCL = 19 @ 5.39 dBm	79	
	DCS1800 PCL = 0 @ 29.89 dBm	187	
	DCS1800 PCL = 7 @ 15.96 dBm	91	
	DCS1800 PCL = 15 @ 0.95 dBm	72	
	PCS1900 PCL = 0 @ 29.66 dBm	196	
	PCS1900 PCL = 7 @ 15.59 dBm	94	
	PCS1900 PCL = 15 @ 0.58 dBm	72	

6.4. Tx Power

Table 41: EG915U-CN RF Output Power

Frequency Band	Max. RF Output Power	Min. RF Output Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm

LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 42: EG915U-EU RF Output Power

Frequency Band	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm

Table 43: EG915U-LA RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B2/B3/B4/B5/B7/B8/B28/B66	23 dBm ±2 dB	< -39 dBm

6.5. Rx Sensitivity

Table 44: EG915U-CN Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)	3GPP (SIMO)
	Primary	
EGSM900	-108.0	-102
DCS1800	-107.5	-102
LTE-FDD B1 (10 MHz)	-97.3	-96.3
LTE-FDD B3 (10 MHz)	-98	-93.3
LTE-FDD B5 (10 MHz)	-99	-94.3
LTE-FDD B8 (10 MHz)	-99	-93.3

LTE-TDD B34 (10 MHz)	-98	-96.3
LTE-TDD B38 (10 MHz)	-97.6	-96.3
LTE-TDD B39 (10 MHz)	-98.4	-96.3
LTE-TDD B40 (10 MHz)	-98.3	-96.3
LTE-TDD B41 (10 MHz)	-97	-94.3

Table 45: EG915U-EU Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)	3GPP (SIMO)
	Primary	
GSM850	-108	-102
EGSM900	-106.5	-102
DCS1800	-107.5	-102
PCS1900	-107	-102
LTE-FDD B1 (10 MHz)	-97	-96.3
LTE-FDD B3 (10 MHz)	-98.3	-93.3
LTE-FDD B5 (10 MHz)	-97.4	-94.3
LTE-FDD B7 (10 MHz)	-96.1	-94.3
LTE-FDD B8 (10 MHz)	-97	-93.3
LTE-FDD B20 (10 MHz)	-98.3	-93.3
LTE-FDD B28 (10 MHz)	-98.6	-94.8

Table 46: EG915U-LA Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency	Receiving Sensitivity (Typ.)	3GPP (SIMO)
	Primary	
GSM850	-108	-102

EGSM900	-106.8	-102
DCS1800	-107.5	-102
PCS1900	-107.2	-102
LTE-FDD B2 (10 MHz)	-98.1	-94.3
LTE-FDD B3 (10 MHz)	-98.2	-93.3
LTE-FDD B4 (10 MHz)	-97.5	-96.3
LTE-FDD B5 (10 MHz)	-97.4	-94.3
LTE-FDD B7 (10 MHz)	-96.1	-94.3
LTE-FDD B8 (10 MHz)	-97.5	-93.3
LTE-FDD B28 (10 MHz)	-99.4	-93.3
LTE-FDD B66 (10 MHz)	-97.9	-95.8

6.6. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the electrostatics discharge characteristics of the module.

Table 47: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interface	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.7. Operating and Storage Temperatures

Table 48: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [5]	-35	+25	+75	ºC
Extended Temperature Range [6]	-40	+25	+85	ºC
Storage Temperature Range	-40	+25	+90	ºC

[5] Within this range, the module's indicators comply with 3GPP specification requirements.
[6] Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

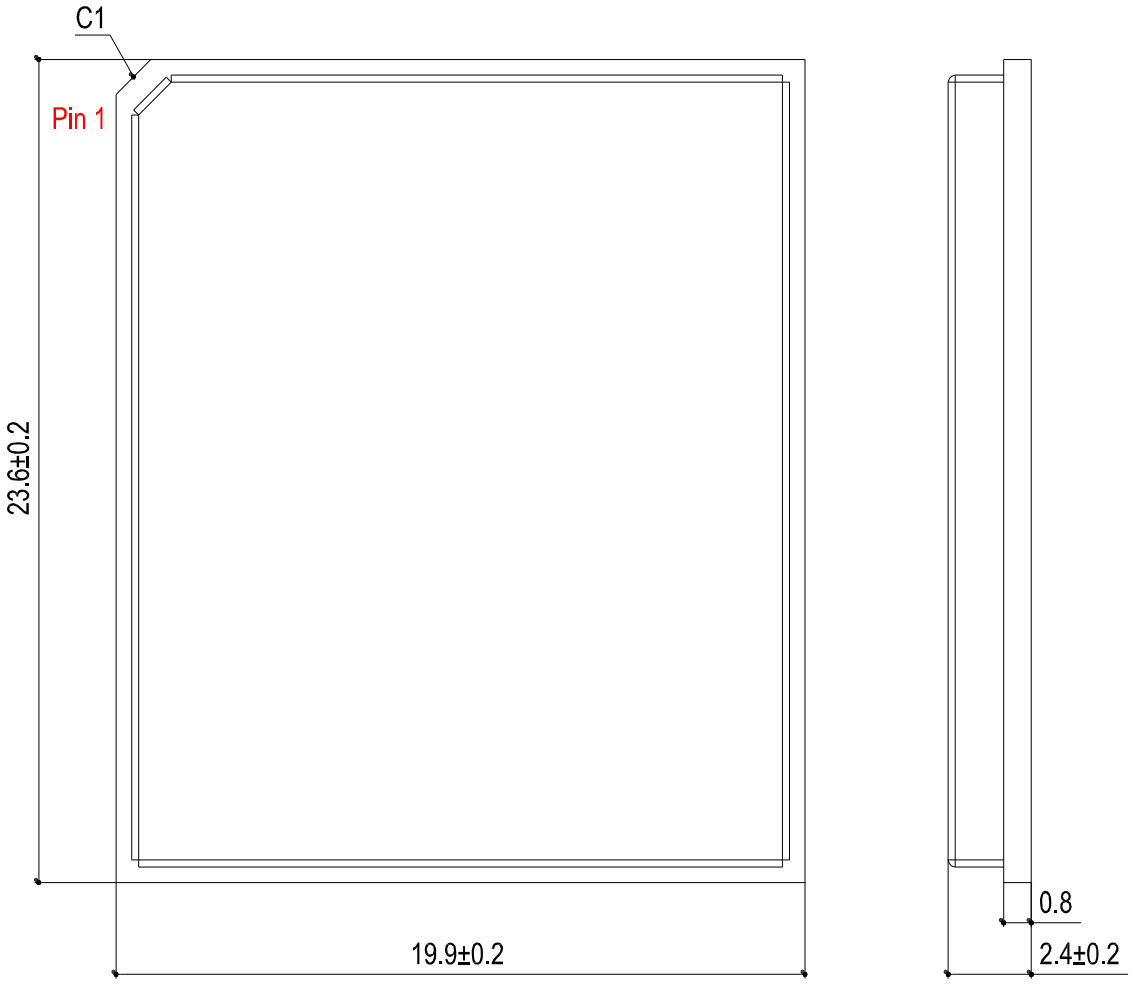


Figure 38: Module Top and Side Dimensions (Unit: mm)

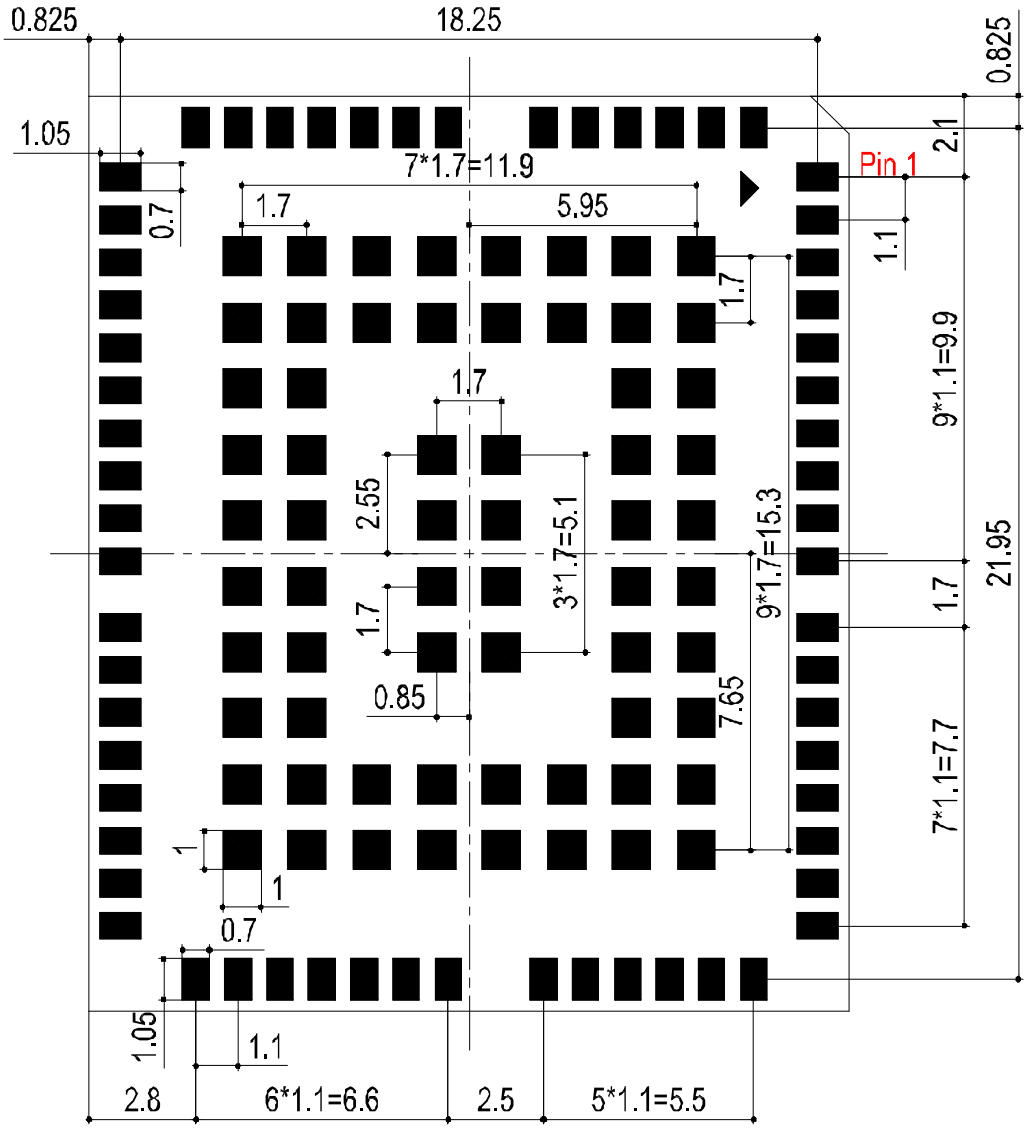


Figure 39: Module Bottom Dimensions

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

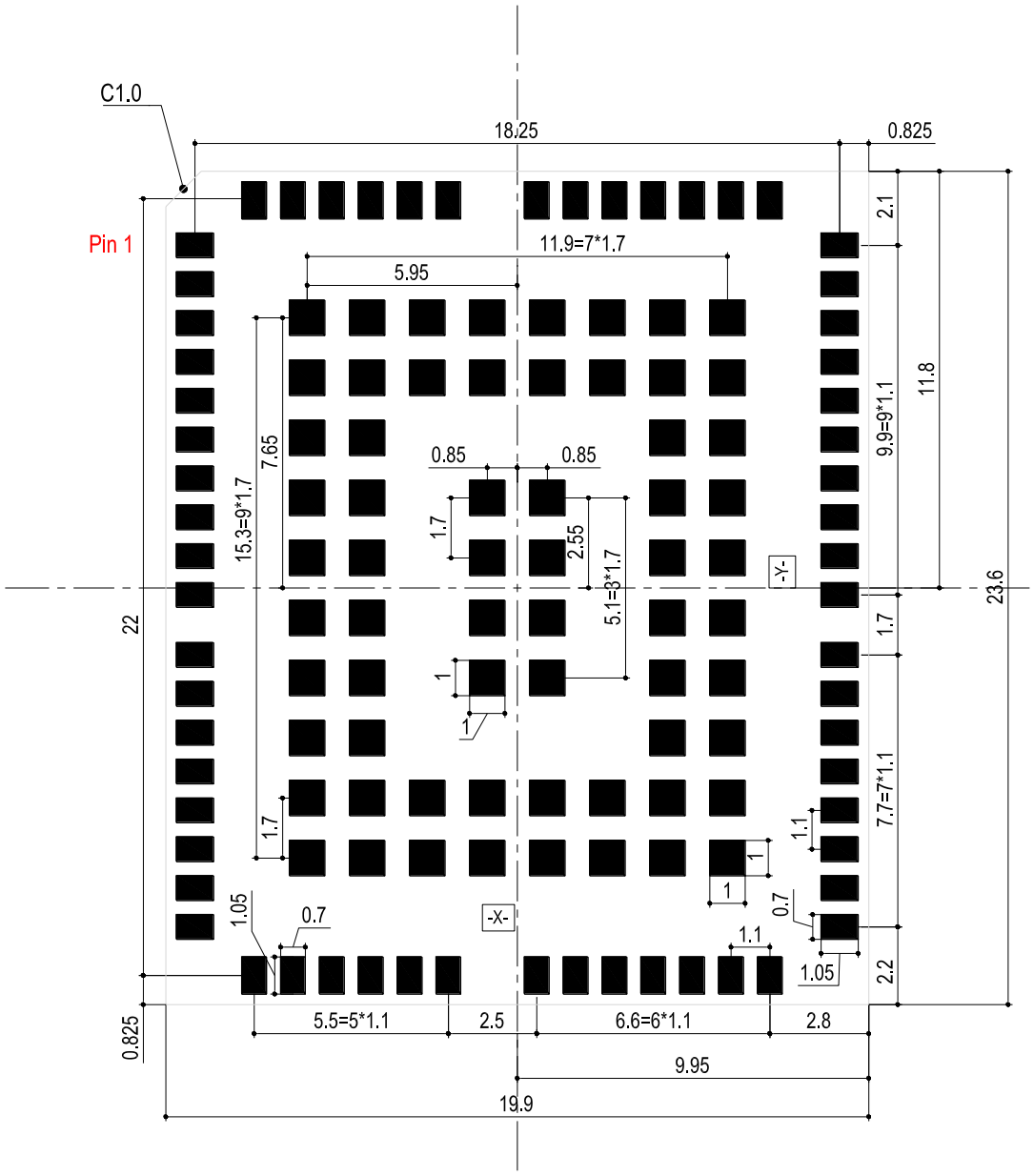


Figure 40: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

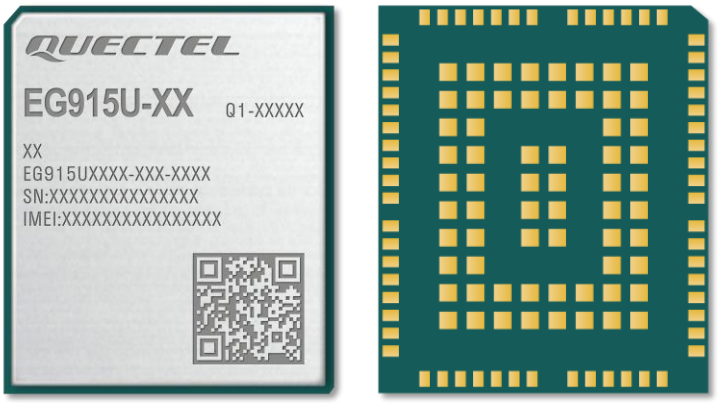


Figure 41: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

Module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [7] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[7] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [11]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

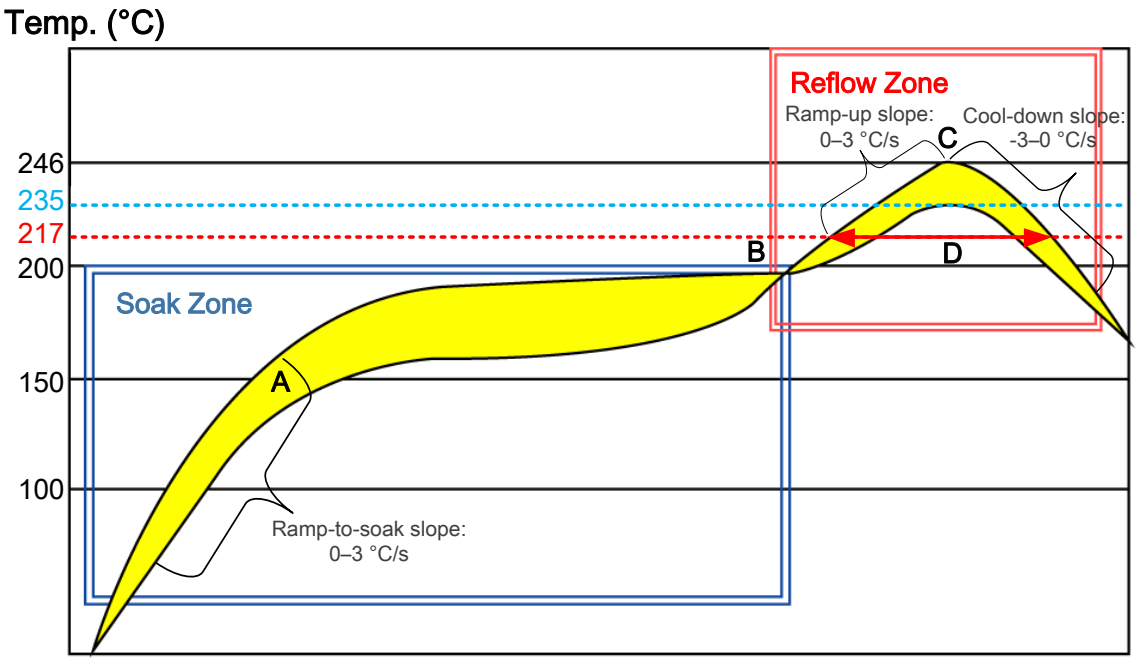


Figure 42: Recommended Reflow Soldering Thermal Profile

Table 49: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [11]***.

8.3. Packaging Specification

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

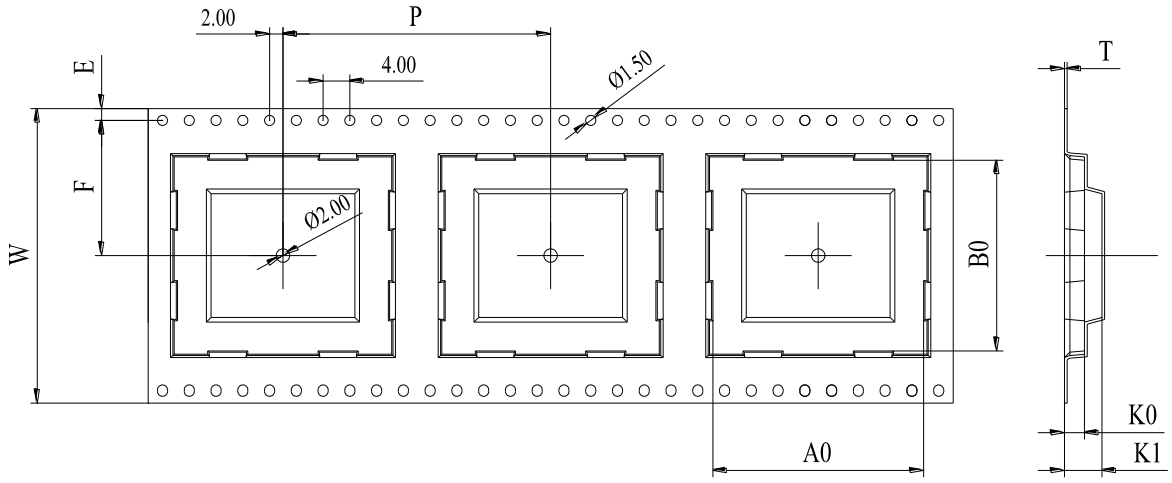


Figure 43: Carrier Tape Dimension Drawing

Table 50: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	20.2	24	3.15	6.65	20.2	1.75

8.3.2. Plastic Reel

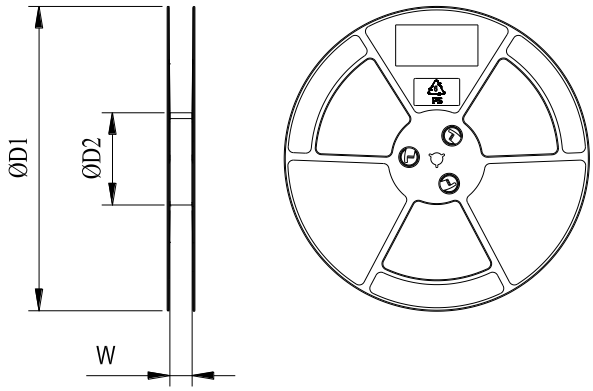


Figure 44: Plastic Reel Dimension Drawing

Table 51: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

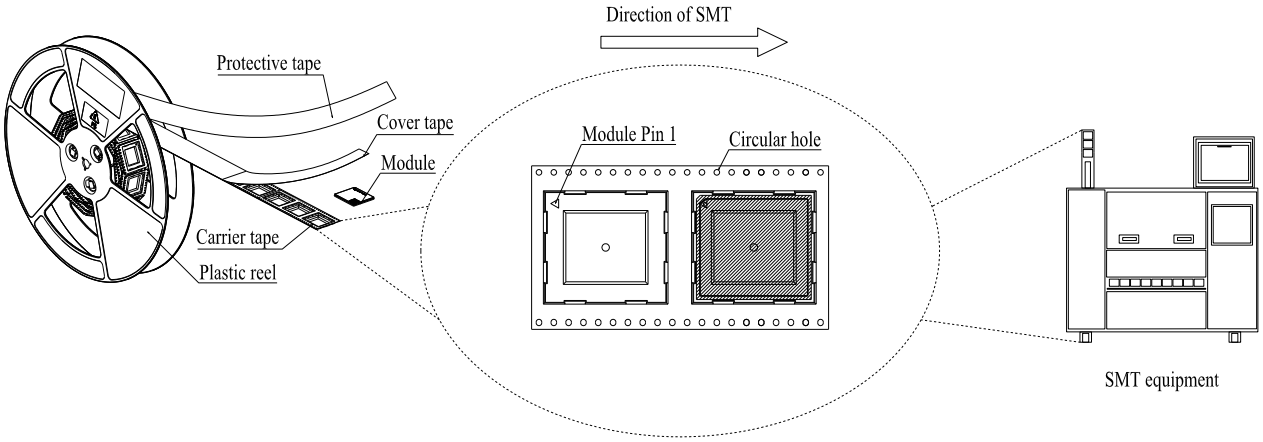
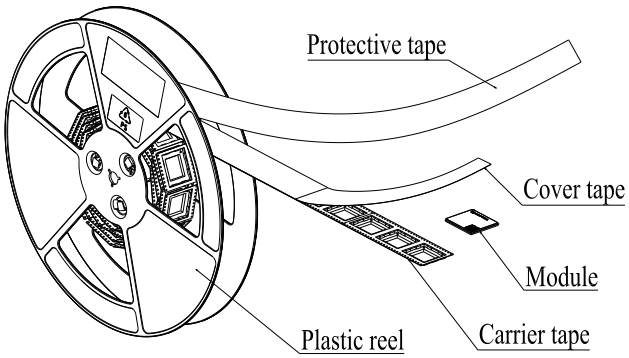


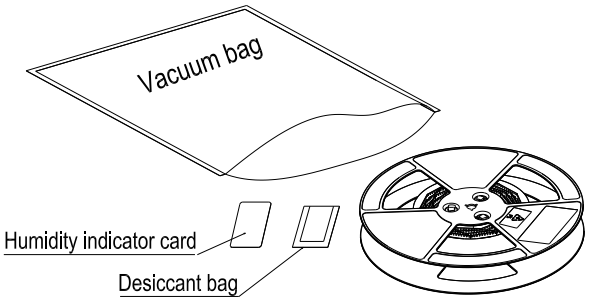
Figure 45: Mounting Direction

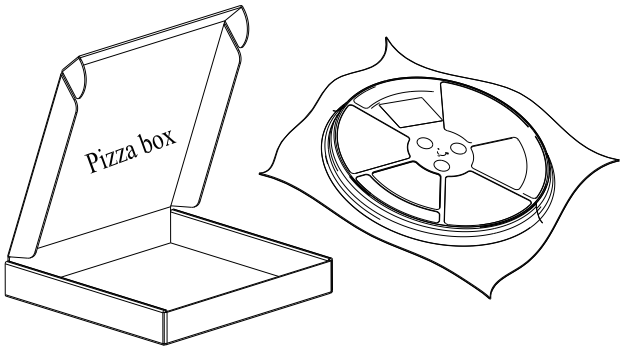
8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

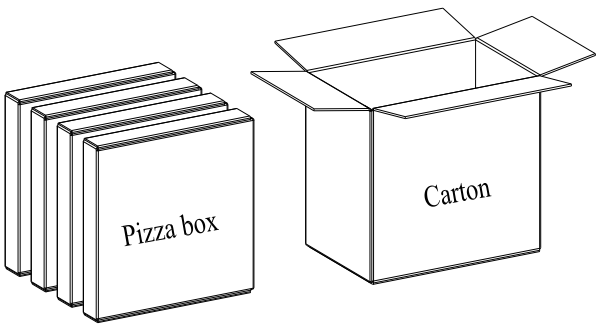


Figure 46: Packaging Process

9 Appendix References

Table 52: Related Documents

Document Name	
[1]	Quectel_EG915U_Series_QuecOpen_GPIO_Configuration
[2]	Quectel_LTE_OPEN_EVB_User_Guide
[3]	Quectel_EC200U&EG91xU_Series_QuecOpen(SDK)_Device_Management_API_Reference_Manual
[4]	Quectel_EC200U&EG91xU_Series_QuecOpen(SDK)_Low_Power_Consumption_API_Reference_Manual
[5]	Quectel_EC200U&EG91xU_Series_QuecOpen(SDK)_PSM_Application_Note
[6]	Quectel_EC200U&EG91xU_Series_QuecOpen(SDK)_Booting&Shutdown_Development_Guide
[7]	Quectel_EG915U_Series_QuecOpen_Reference_Design
[8]	Quectel_EC200U&EG91xU_Series_QuecOpen(SDK)_(U)SIM_API_Reference_Manual
[9]	Quectel_EC200U&EG91xU_Series_QuecOpen(SDK)_ADC_Development_Guide
[10]	Quectel_RF_Layout_Application_Note
[11]	Quectel_Module_SMT_User_Guide

Table 53: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-WB	Adaptive Multi-Rate Wideband
AP	Application Processor
bps	bit(s) per second
CHAP	Challenge Handshake Authentication Protocol

CS	Coding Scheme
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DMA	Direct Memory Access
DRX	Discontinuous Reception
DRX	Diversity Receive
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
GRFC	General RF Control
HB	High Band
HR	Half Rate
I/O	Input/Output
LB	Low Band
LGA	Land Grid Array
LTE	Long Term Evolution
MB	Middle Band
MCU	Microcontroller Unit
MT	Mobile Terminated
OTA	Over-the-air Programming
PA	Power Amplifier
PAP	Password Authentication Protocol
PC	Personal Computer

PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
R&D	Research and Development
RI	Ring Indicator
RF	Radio Frequency
Rx	Receive
SIMO	Single Input Multiple Output
SMS	Short Message Service
SPI	Serial Peripheral Interface
TDD	Time Division Duplexing
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UL	Uplink
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage

V_{IL}min	Minimum Low-level Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio