EG915N Series QuecOpen Reference Design

LTE Standard Module Series

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About the Document

Revision History

Version	Date	Author	Description
-	2022-02-15	Tik HUANG	Creation of the document
1.0	2023-05-25	Shihao HUANG/ Jeff SHEN	First official release

Contents

1 Reference Design

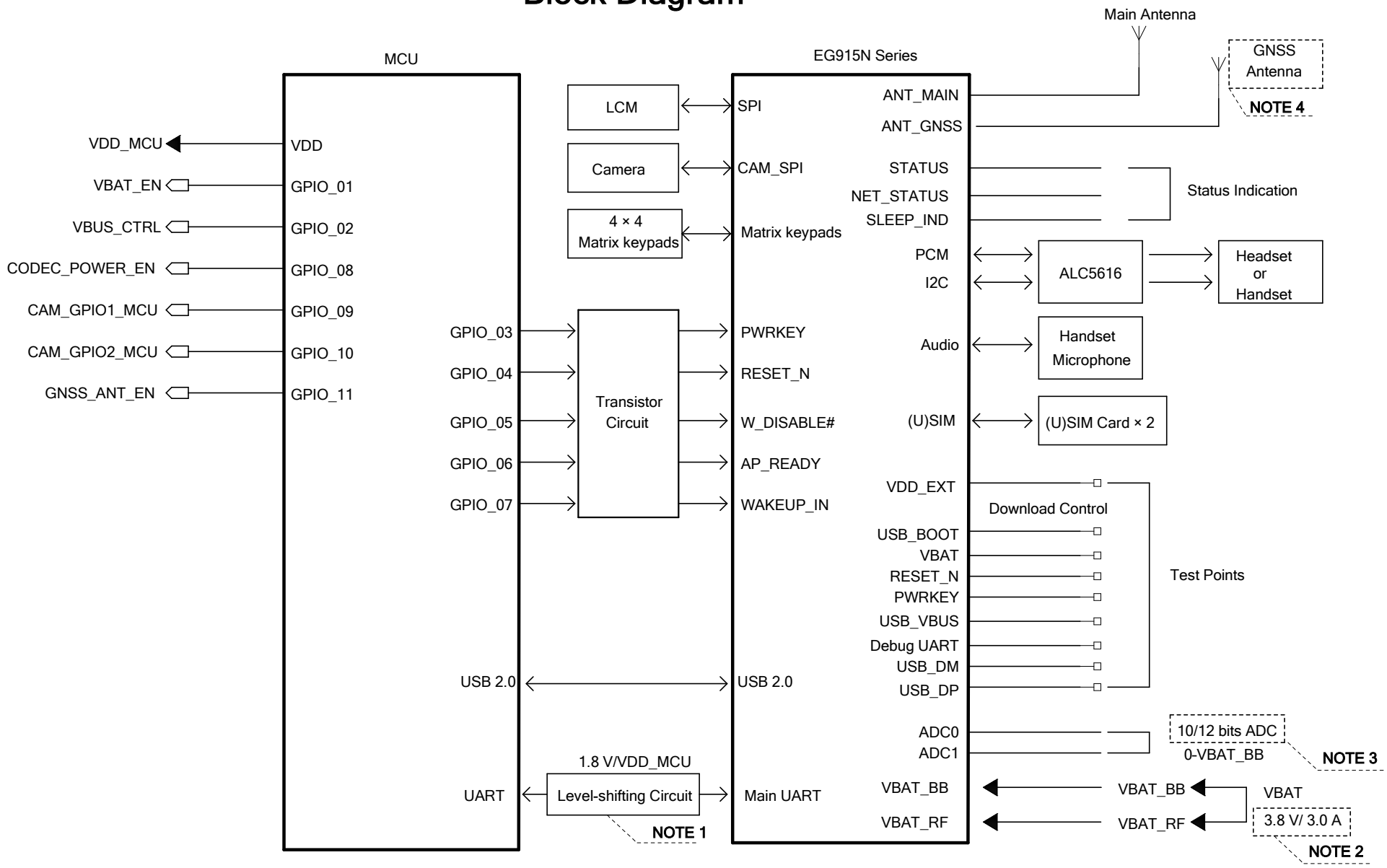
1.1. Introduction

This document provides the reference design for Quectel EG915N series QuecOpen® module.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



NOTE:

1. A level-shifting circuit or a voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.
2. The power supply should be able to provide at least 3.0 A for the module.
3. EG915N-LA/-EA: 10 bits resolution, provide one analog-to-digital converter (ADC) interface.
   EG915N-EU: 12 bits resolution, provides two analog-to-digital converter (ADC) interfaces.
4. GNSS function is optional for the module. Only the module with built-in GNSS function can support GNSS function.

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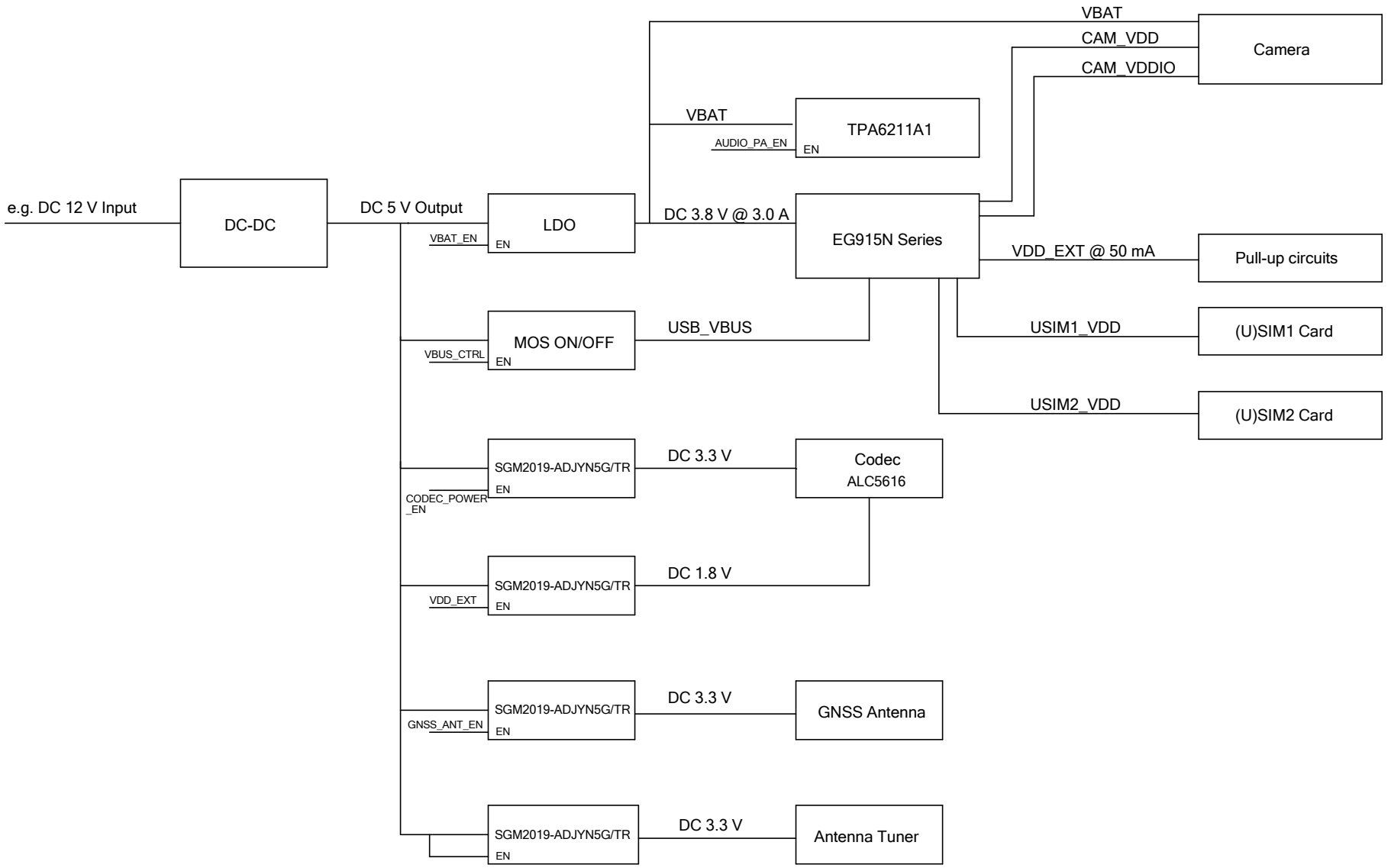
Power System Block Diagram



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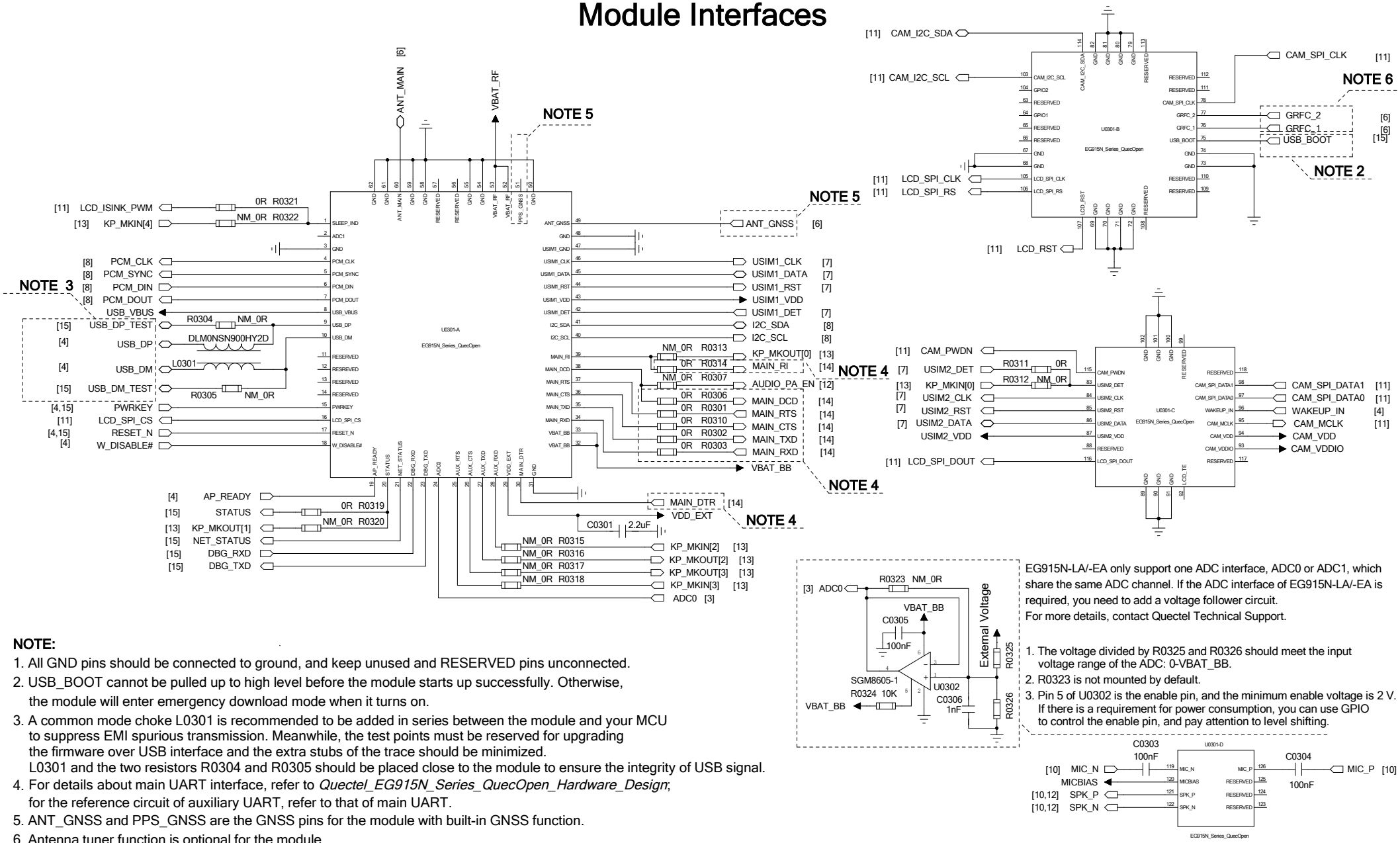
Module Interfaces



EG915N-LA/-EA only support one ADC interface, ADC0 or ADC1, which share the same ADC channel. If the ADC interface of EG915N-LA/-EA is required, you need to add a voltage follower circuit.
For more details, contact Quectel Technical Support.

1. The voltage divided by R0325 and R0326 should meet the input voltage range of the ADC: 0-VBAT_BB.
2. R0323 is not mounted by default.
3. Pin 5 of U0302 is the enable pin, and the minimum enable voltage is 2 V. If there is a requirement for power consumption, you can use GPIO to control the enable pin, and pay attention to level shifting.

NOTE:

1. All GND pins should be connected to ground, and keep unused and RESERVED pins unconnected.
2. USB_BOOT cannot be pulled up to high level before the module starts up successfully. Otherwise, the module will enter emergency download mode when it turns on.
3. A common mode choke L0301 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the test points must be reserved for upgrading the firmware over USB interface and the extra stubs of the trace should be minimized. L0301 and the two resistors R0304 and R0305 should be placed close to the module to ensure the integrity of USB signal.
4. For details about main UART interface, refer to *Quectel_EG915N_Series_QuecOpen_Hardware_Design*; for the reference circuit of auxiliary UART, refer to that of main UART.
5. ANT_GNSS and PPS_GNSS are the GNSS pins for the module with built-in GNSS function.
6. Antenna tuner function is optional for the module.

Note for Circuit Layout Design:

Ensure that there is a complete reference ground plane below the module, and the ground plane should be placed as close to the module layer as possible. Other traces cannot be routed on the first layer below the module. At least a 4-layer board design is recommended.

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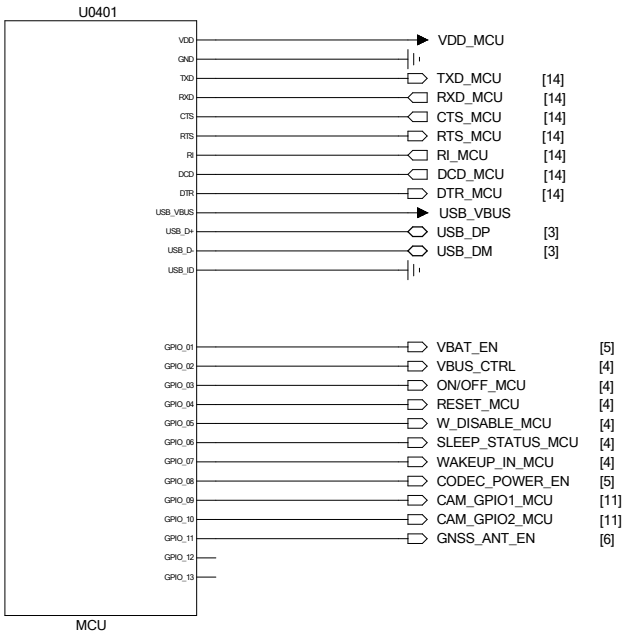
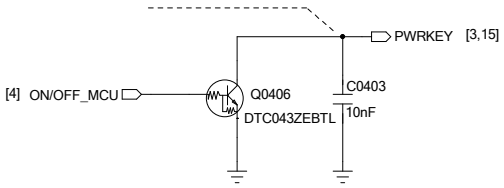
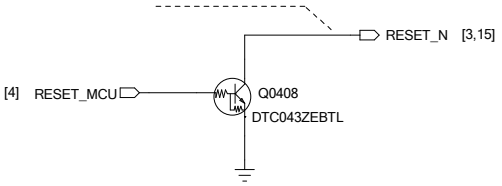
MCU Interfaces



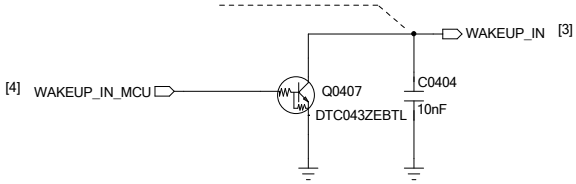
It is used to turn on/off the module.



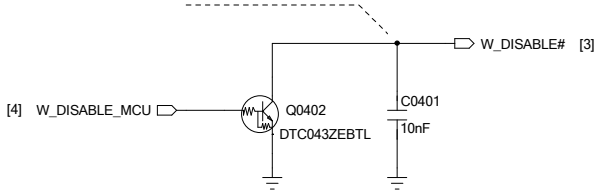
It is used to reset the module.



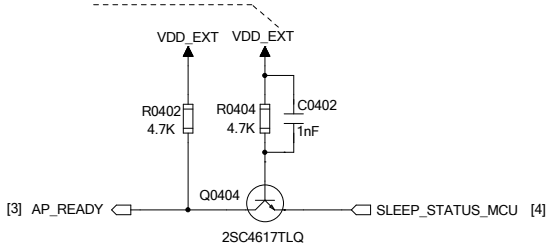
It is used to wake up the module.



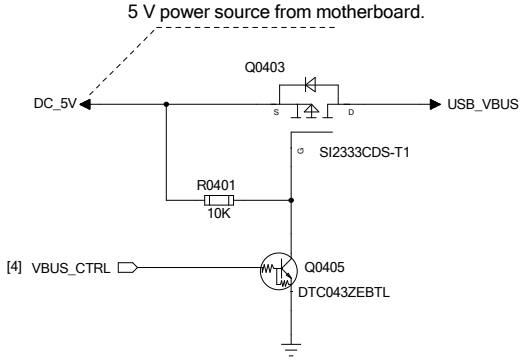
It is used to set the module into the airplane mode.



it is used to detect the sleep status of MCU.



5 V power source from motherboard.



NOTE:

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V.
   If the power domain of GPIO interfaces of U0401 is also 1.8 V, then the related level-shifting circuit is not needed.
2. The USB 2.0 interface of the module only serves as a slave device and supports full-speed and high-speed modes.
   To communicate with the USB interface, MCU needs to support USB host mode or OTG function. The USB_VBUS of the module should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the GPIO pins of MCU which are at low level by default as the control pins for PWRKEY and RESET_N of the module.
   Ensure that the load capacitance on PWRKEY and RESET_N pins does not exceed 10 nF.

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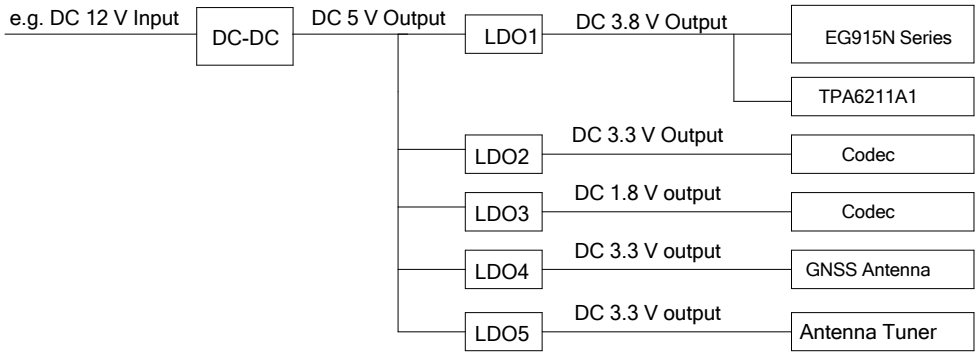
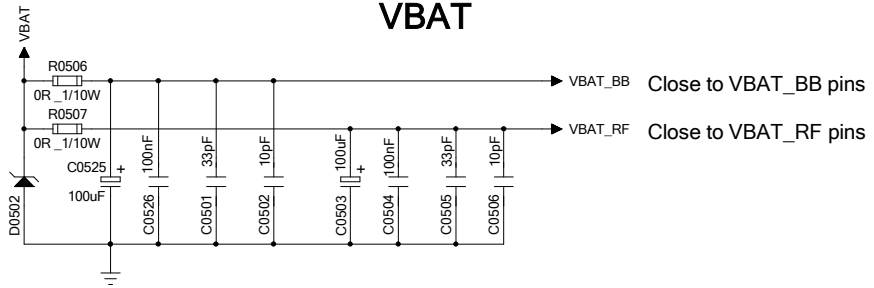
Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to 5.0 V, and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V to power the module, GNSS antenna, antenna tuner, PA and Codec.



VBAT

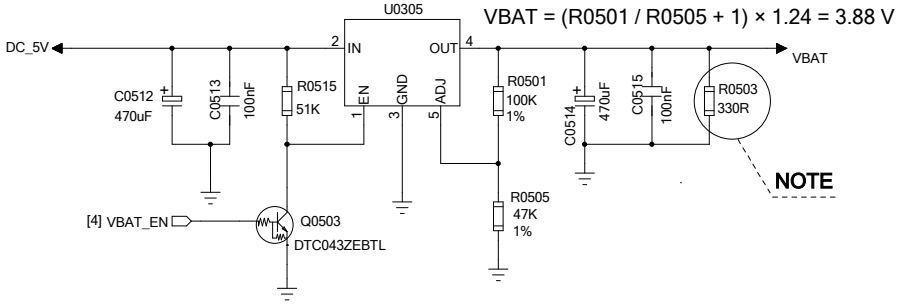


NOTE:

1. The power supply should be able to provide sufficient current of at least 3 A for the module.
2. The VBAT trace should be connected to pins VBAT_BB and VBAT_RF in a star configuration.
3. The width of VBAT_BB trace should not be less than 1 mm; and the width of VBAT_RF trace should not be less than 2 mm.
4. The recommended operating voltage of VBAT is 3.4-4.5 V; the typical operating voltage of VBAT is 3.8 V.

LDO Application

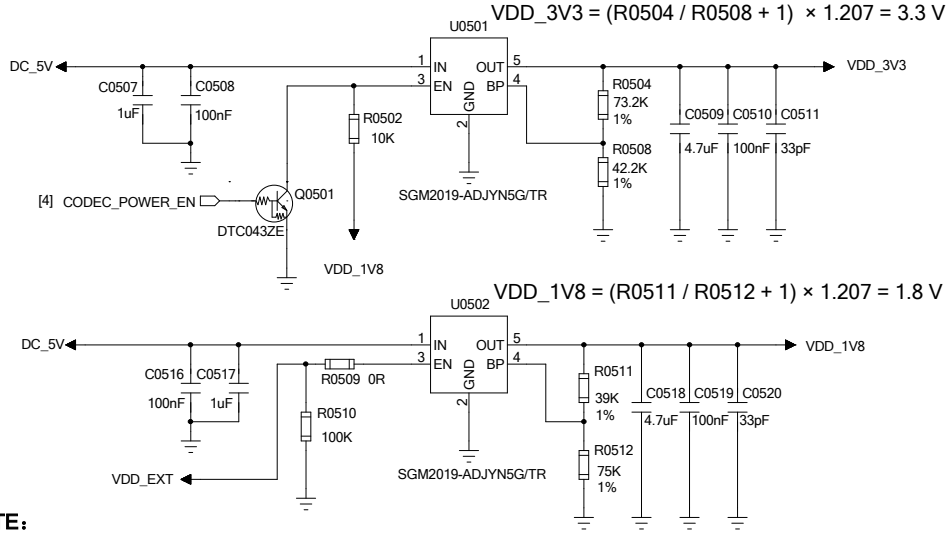
When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



NOTE:

The recommended load current is greater than 10 mA.

Power Supply for PCM Codec



NOTE：

1. VDD_EXT and CODEC_POWER_EN are used to turn on/off VDD_1V8 and VDD_3V3 respectively.
2. The following power-up/down sequences should be followed to ensure the audio codec works normally.
   Power-up sequence: power up VDD_1V8 first, and then VDD_3V3.
   Power-down sequence: power down VDD_3V3 first, and then VDD_1V8.

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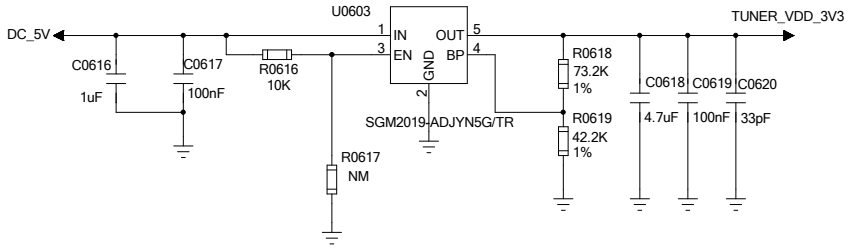
Antenna Interface Design

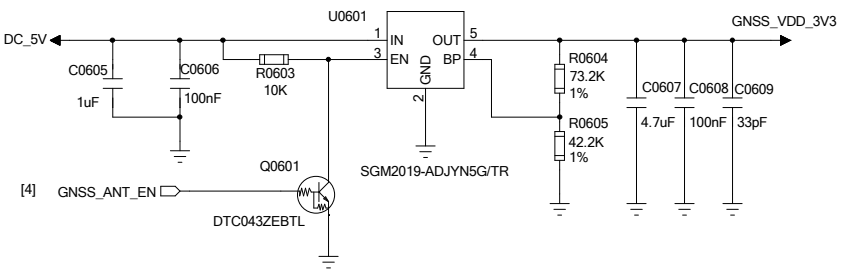
Antenna Tuner Power Supply

TUNER_VDD_3V3 = (R0618 / R0619 + 1) × 1.207 = 3.3 V

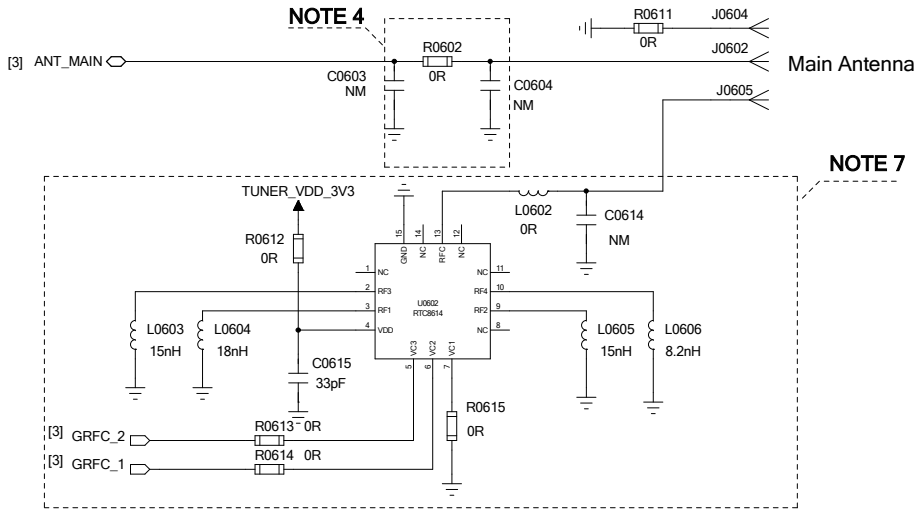


GNSS Active Antenna Power Supply

GNSS_VDD_3V3 = (R0604 / R0605 + 1) × 1.207 = 3.3 V

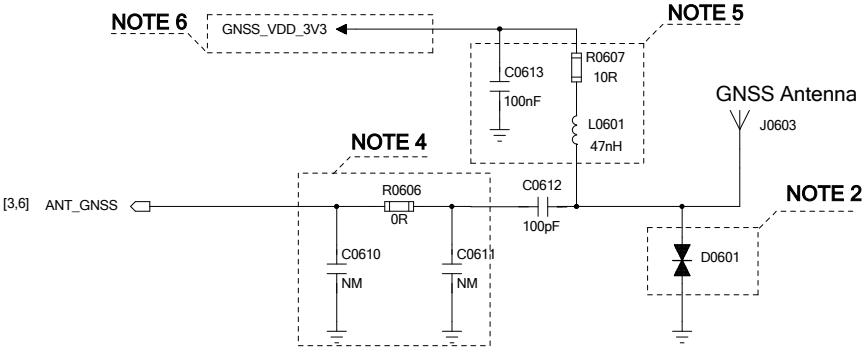


Main Antenna

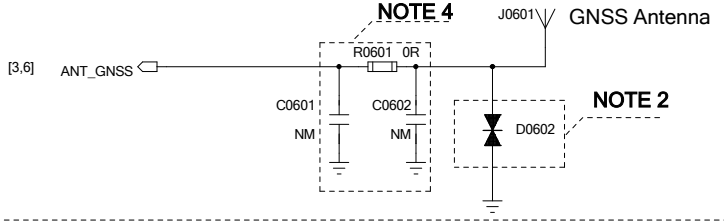


Tuner	GRFC_1	GRFC_2	RF	EG915N-EU	EG915N-LA	EG915N-EA
Status	0	0	RF1	NM	LTE B28	LTE B28
	0	1	RF2	LTE B20	LTE B5/GSM850	LTE B20
	1	0	RF3	LTE B8/EGSM900	LTE B8/EGSM900	LTE B8/EGSM900
	1	1	RF4	LTE B1/3/7/DCS1800	LTE B2/3/4/7/66/DCS1800/PCS1900	LTE B1/3/7/DCS1800

GNSS Active Antenna



GNSS Passive Antenna Design



NOTE:

1. GNSS function is optional for the module. Thus, GNSS antenna design is only suitable for the module with built-in GNSS funtion.
2. The junction capacitance of the antenna ESD protection component should be less than 0.05 pF.
3. The single-ended impedance of the RF antenna is 50 Ω.
4. The reserved Π-type circuit is used to match the impedence of the antenna.
5. R0607, L0601 and C0613 are recommended to be placed close to the RF trace during the layout.
6. The external active antenna power supply voltage range is from 2.8 V to 4.3 V, and the typical value is 3.3 V.
   The power supply voltage can be designed according to the power supply requirements of the selected active antenna.
7. Antenna tuner function is optional, and antenna tuner should be placed close to J0605.

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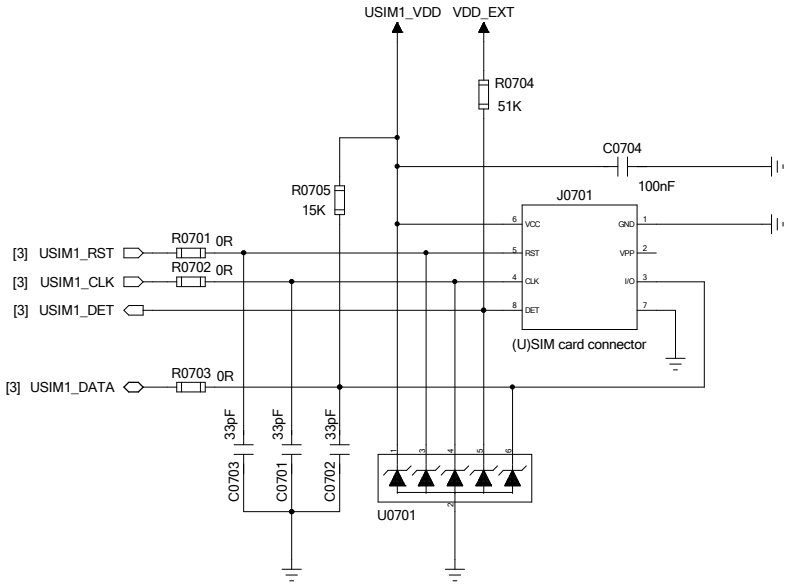
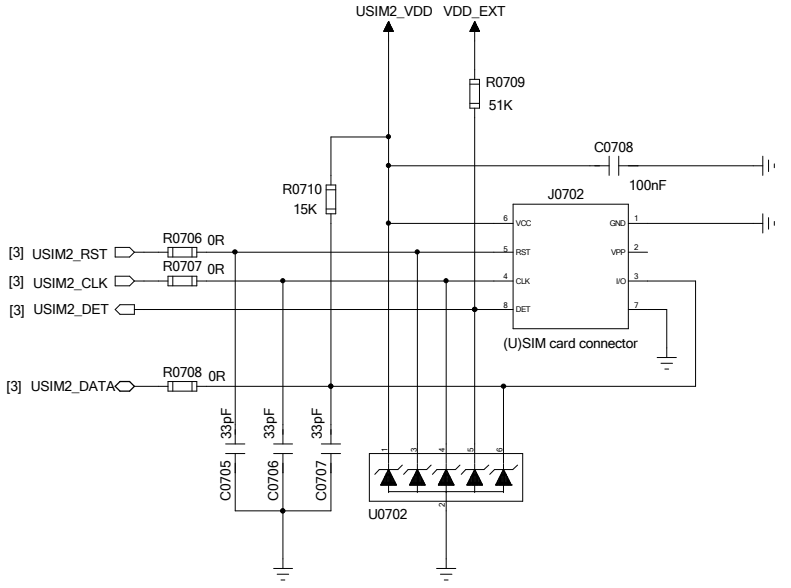
(U)SIM Interface Design

(U)SIM1



(U)SIM 2



NOTE:

1. U0701 and U0702 are recommended to be used to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.
2. The pull-up resistors R0705 and R0710 can improve anti-jamming capability, and should be placed close to the (U)SIM card connectors.
3. R0701-R0703 and R0706-R0708 are used for debugging, and C0701-C0703 and C0705-C0707 are used for filtering out RF interference.
4. The capacitance of C0704 and C0708 should be less than 1 μF and they should be placed close to the (U)SIM card connectors.
5. The GND of the (U)SIM card connector is recommended to be connected to the GND layer directly.
6. For more information about the layout of (U)SIM interfaces, refer to *Quectel_EG915N_Series_QuecOpen_Hardware_Design*.

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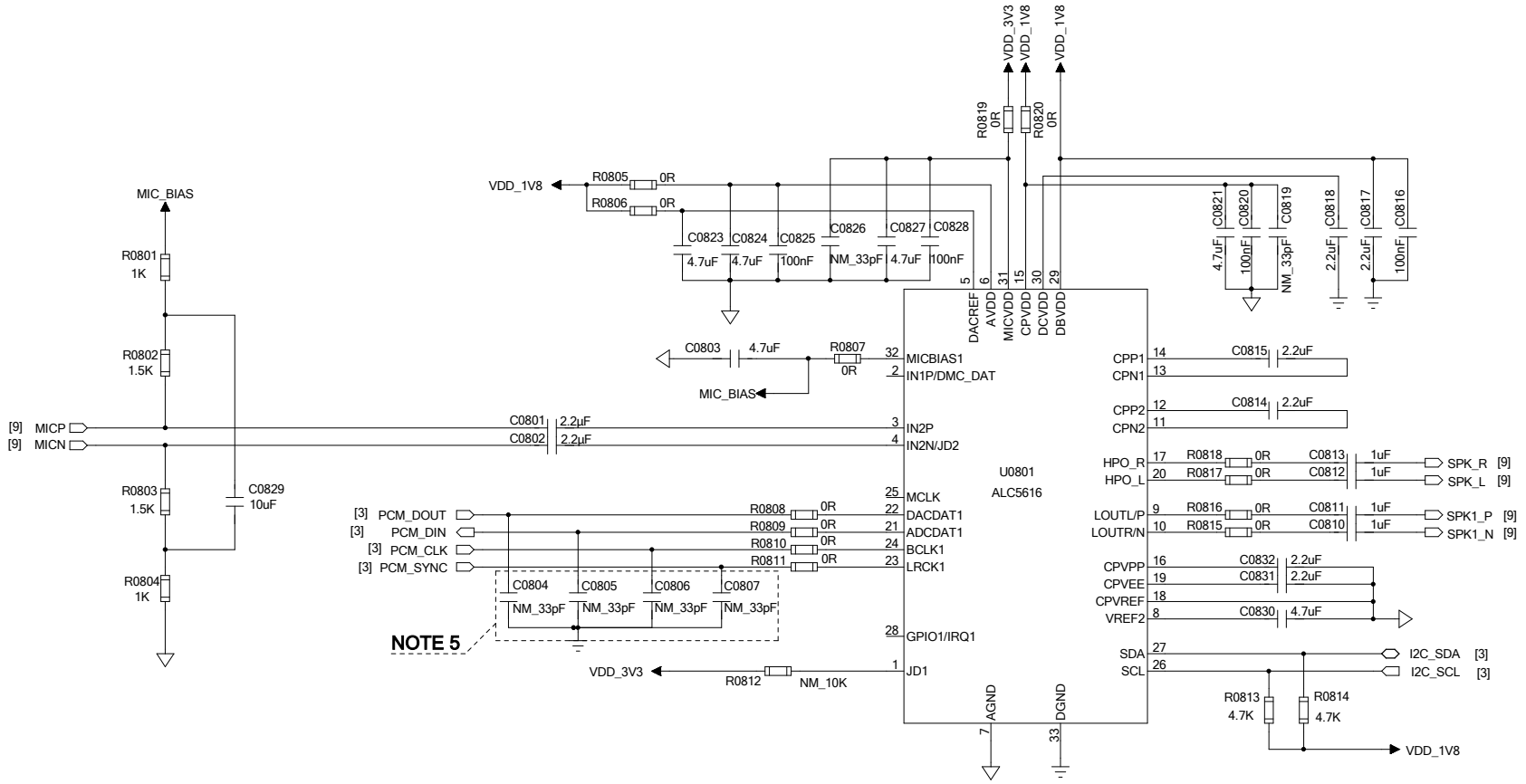
Analog Audio Design (ALC5616)



NOTE:

1. ALC5616 power-up sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD → MICVDD → software initialization.
2. ALC5616 power-down sequence: disable Codec function by software → MICVDD → DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.
3. The module will automatically initialize the Codec via I2C interface after it is turned on successfully, so all power supplies for the Codec need to be powered up before that.
4. Pay attention to the distinction between analog ground and digital ground, both of which need to be connected with a 0 Ω resistor packaged as R-0805. For more details, refer to Sheet "Audio Codec Interface Design".
5. The 33 pF capacitors of the signal pins should be reserved, and be used according to the actual debugging situation.
6. For more details, refer to the datasheet of ALC5616.

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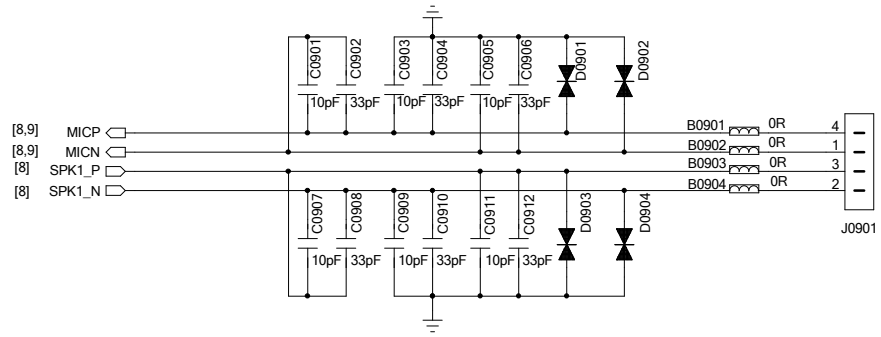
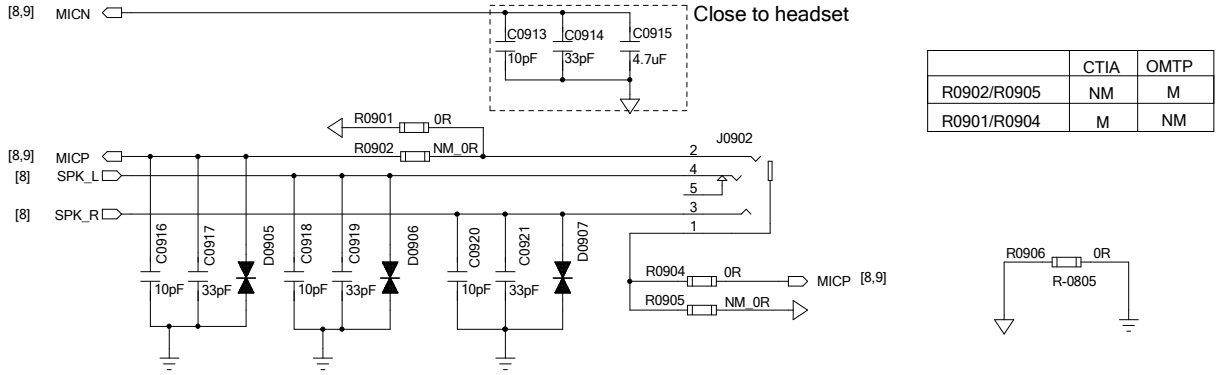
Audio Codec Interface Design

Handset Application



Headset Application



	CTIA	OMTP
R0902/R0905	NM	M
R0901/R0904	M	NM

NOTE:

1. The Codec analog output can drive handset and headset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.
2. In handset application, route the MIC and SPK signal traces as differential pairs respectively.
3. In headset application, route the MIC signal trace as a differential pair.
4. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noises such as clock and DC-DC signals.
5. Pay attention to the distinction between analog ground and digital ground, both of which need to be connected with a o Ω resistor packaged as R-0805.

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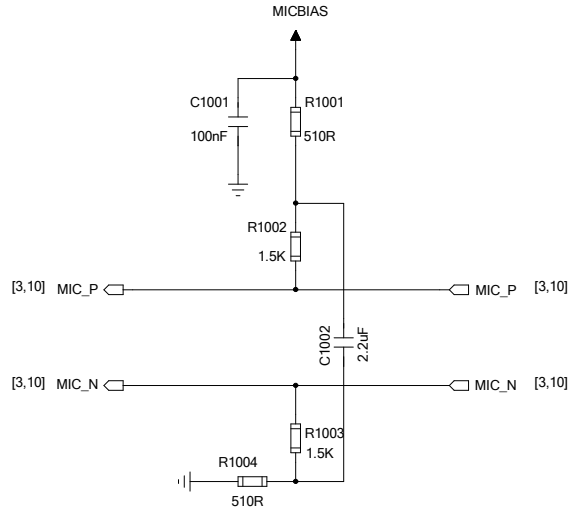
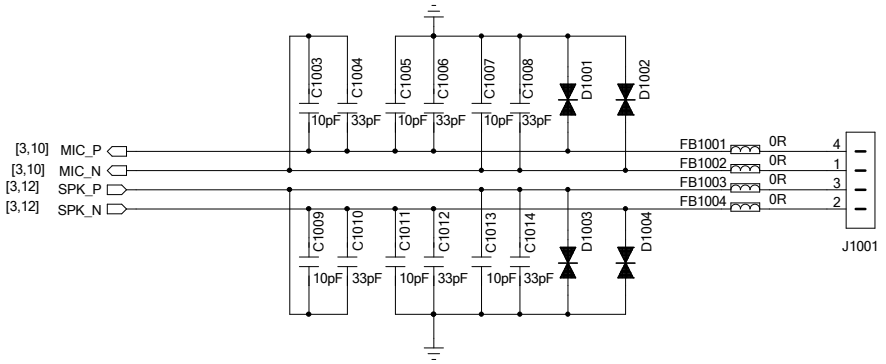
Analog Audio Design

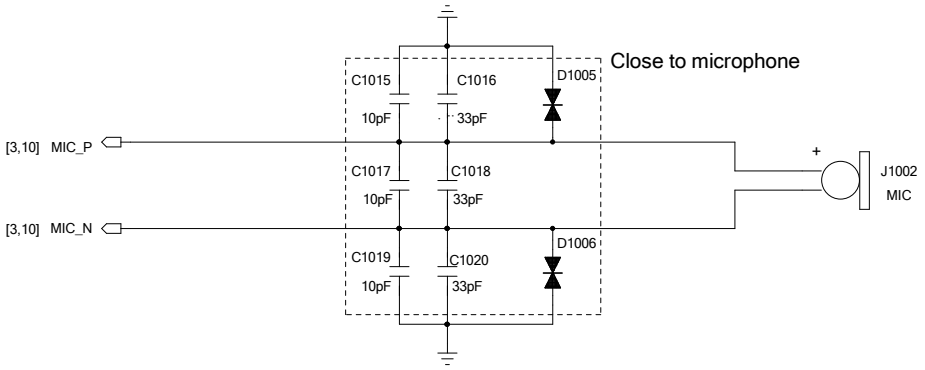
Microphone Bias Circuit



Handset Application



Microphone Application



NOTE:

1. Both the MIC and SPK signal traces need to be routed as differential pairs.
2. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noises.
3. D1001-D1004, D1005-D1006 are used for ESD protection, and they should be placed close to the handset and microphone.
4. The 10 pF capacitors and 33 pF capacitors are used to filter out the TDD noise, and they should be placed close to the handset and microphone.
5. The analog output can drive handset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.

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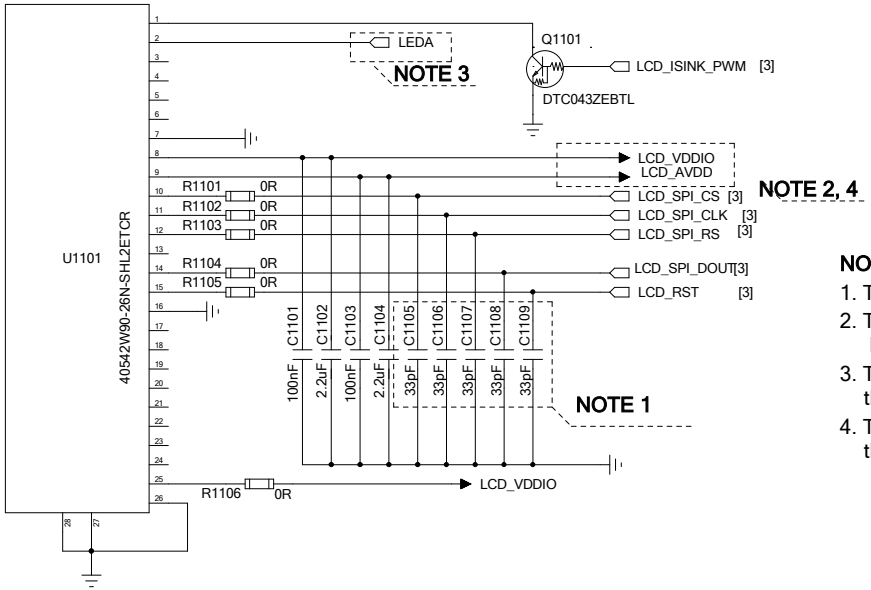
LCM & Camera Interface Design

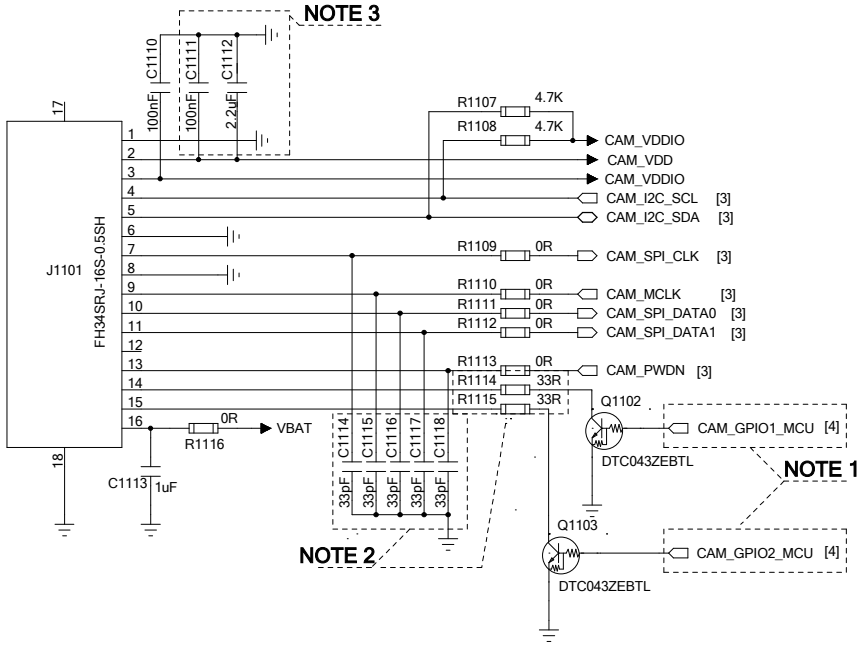
LCM Interface



NOTE:

1. The 33 pF capacitors of the signal pins are reserved, and can be used according to the actual debugging situation.
2. To avoid abnormal LCM display caused by power fluctuation, the filter capacitors of the LCM power supply pins LCD_AVDD and LCD_VDDIO must be mounted.
3. The power supply pin LEDA of the backlight is provided by an external power supply circuit, and you can design the circuit by yourself.
4. The LCD_VDDIO and LCD_AVDD are provided by external power supply, and you can design the circuit by yourself.

Camera Interface



NOTE:

1. CAM_GPIO1_MCU controls the cathode of the positioning light of the camera by controlling the triode switching circuit; CAM_GPIO2_MCU controls the cathode of the supplement light of the camera by controlling the triode switching circuit; It is recommended to select GPIO pins which are in pull-down status by default as the two control pins.
2. The 33 pF capacitors of the signal pins are reserved, and they are used according to the actual debugging situation. The values of current limiting resistors (R1114 and R1115) of positioning light and supplement light should be varied according to brightness requirements.
3. The capacitors of the CAM_VDD power supply should be connected to the GND layer directly, otherwise there may be power noise resulting in abnormalities such as white dots on the preview screen.
4. If the camera interface is not required, CAM_I2C_SCL and CAM_I2C_SDA can be used as general I2C interfaces for connecting with other peripherals.

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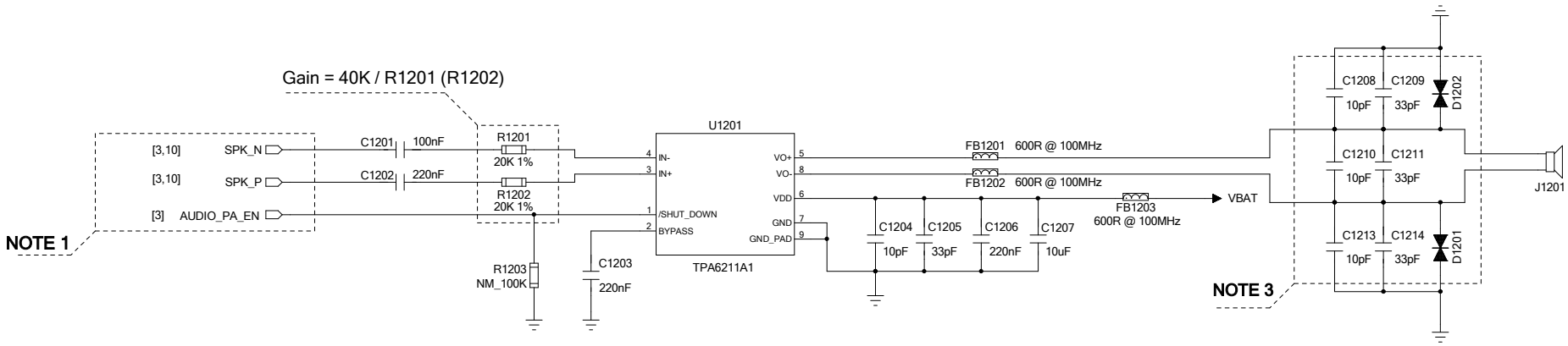
Analog Audio Design (Audio Power Amplifier)



NOTE:

1. SPK_P and SPK_N are differential output channels that can be used for external audio amplifier.
   It is recommended to use GPIO pins of the module to control the enable pin of the audio power amplifier to eliminate POP noise, and the selected GPIO pin should be at low level by default, such as pin 38 (MAIN_DCD).
   For more information about AUDIO_PA_EN, contact Quectel Technical Support.
2. The model of power amplifier in this design is for reference only. Select the appropriate audio power amplifier according to actual needs.
3. Place filter capacitors and ESD protection components close to the loudspeaker.
4. The selection of ESD protection component is related to the selection of audio power amplifier. Ensure that the output voltage of audio power amplifier is within the maximum reverse working voltage range of ESD protection components under normal working condition, so as to avoid damage to ESD protection components.

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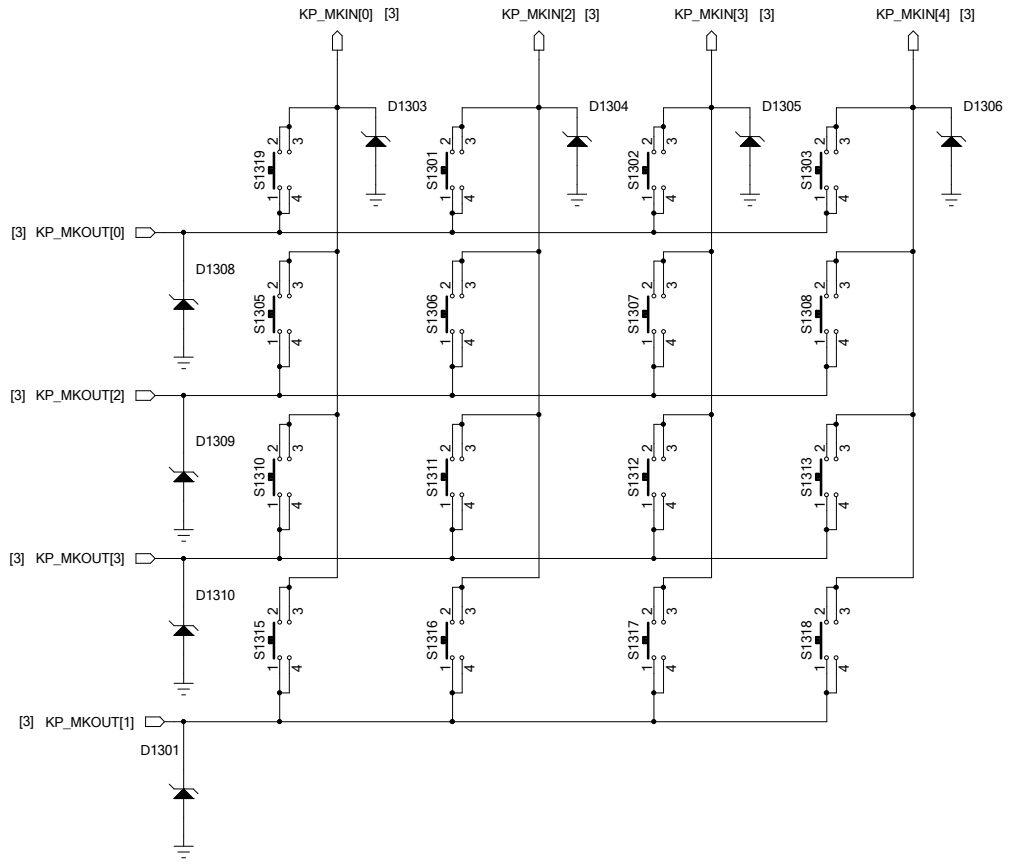
Matrix Keypad Interface Design



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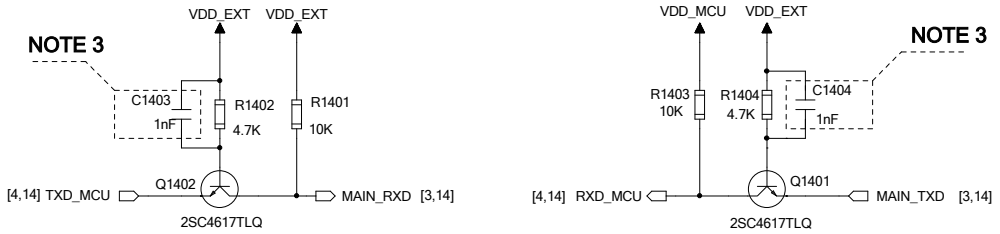
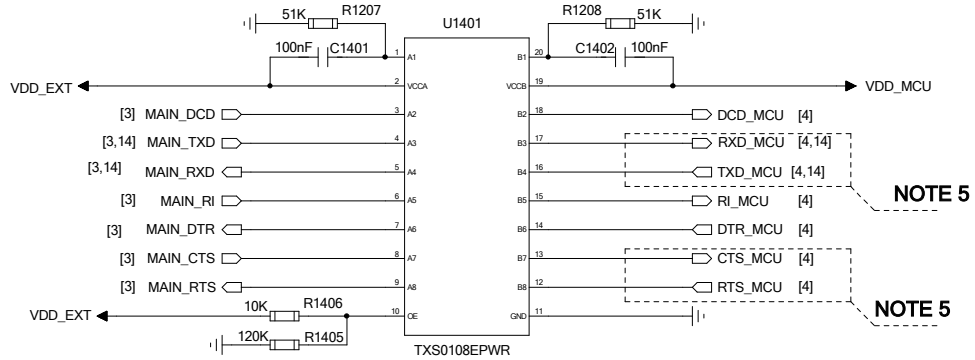
UART Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, refer to the datasheet of TXS0108EPWR.
3. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C1403 and C1404 of 1 nF can improve the signal quality.
4. MAIN_RTS and MAIN_DTR level-shifting circuits are similar to that of the MAIN_RXD.
   MAIN_CTS, MAIN_RI and MAIN_DCD level-shifting circuits are similar to that of the MAIN_TXD.
5. The UART hardware flow control pins MAIN_CTS and MAIN_RTS adopt the direct mode, that is, the RTS of the module is connected to the RTS of the MCU, and the CTS of the module is connected to the CTS of the MCU. Pay attention to the direction of signal input and output.
   MAIN_TXD and MAIN_RXD adopt a cross connection mode, that is, the TXD and RXD of the module are respectively connected to the RXD and TXD of the MCU.

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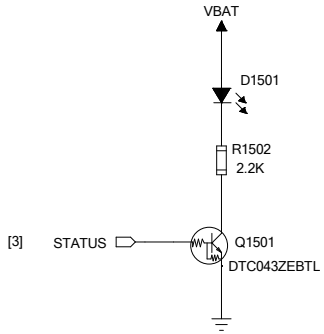
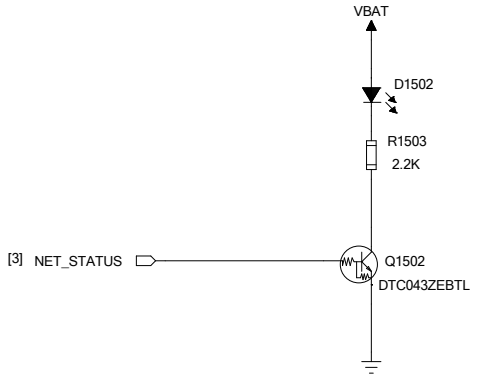
Other Designs

Indicators

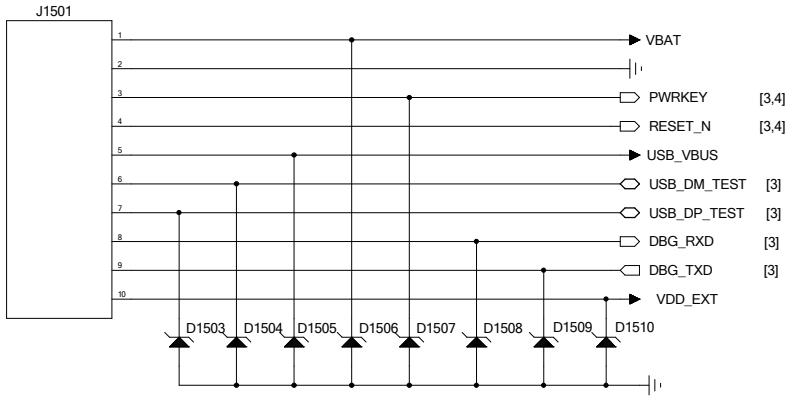




NOTE:

1. For more details about STATUS and NET_STATUS, refer to *Quectel_EG915N_Series_QuecOpen_Hardware_Design*.
2. If the low current consumption is required when your device is in sleep mode, replace the power supply VBAT of the STATUS and NET_STATUS indicators with external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

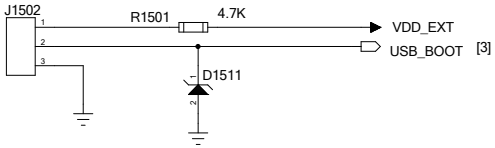
Reserved Test Points



NOTE:

1. Test points for both USB and debug UART interfaces are reserved for capturing logs.
2. Test points for USB interface can also be reserved for firmware upgrade.
3. The junction capacitance of the ESD protection components on USB data lines should be less than 2 pF.
4. The debug UART interface supports 1.8 V power domain, and a voltage-level translator should be used if the power domain of your application is 3.3 V.

USB_BOOT Interface



NOTE:

1. Ensure to reserve the USB_BOOT interface design and test points.
2. You can pull up USB_BOOT to 1.8 V or short-circuit VDD_EXT and USB_BOOT before module's startup, and the module will enter emergency download mode. In this mode, the module supports firmware upgrade over USB interface.

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