EG915N Series QuecOpen Hardware Design

LTE Standard Module Series

Version: 1.1

Date: 2023-11-24

Status: Released

At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
http://www.quectel.com/support/sales.htm.

For technical support, or to report documentation errors, please visit:
http://www.quectel.com/support/technical.htm.
Or email us at: support@quectel.com.

Legal Notices

We offer information as a service to you. The provided information is based on your requirements and we make every effort to ensure its quality. You agree that you are responsible for using independent analysis and evaluation in designing intended products, and we provide reference designs for illustrative purposes only. Before using any hardware, software or service guided by this document, please read this notice carefully. Even though we employ commercially reasonable efforts to provide the best possible experience, you hereby acknowledge and agree that this document and related services hereunder are provided to you on an “as available” basis. We may revise or restate this document from time to time at our sole discretion without any prior notice to you.

Use and Disclosure Restrictions

License Agreements

Documents and information provided by us shall be kept confidential, unless specific permission is granted. They shall not be accessed or used for any purpose except as expressly provided herein.

Copyright

Our and third-party products hereunder may contain copyrighted material. Such copyrighted material shall not be copied, reproduced, distributed, merged, published, translated, or modified without prior written consent. We and the third party have exclusive rights over copyrighted material. No license shall be granted or conveyed under any patents, copyrights, trademarks, or service mark rights. To avoid ambiguities, purchasing in any form cannot be deemed as granting a license other than the normal non-exclusive, royalty-free license to use the material. We reserve the right to take legal action for noncompliance with abovementioned requirements, unauthorized use, or other illegal or malicious use of the material.

Trademarks

Except as otherwise set forth herein, nothing in this document shall be construed as conferring any rights to use any trademark, trade name or name, abbreviation, or counterfeit product thereof owned by Quectel or any third party in advertising, publicity, or other aspects.

Third-Party Rights

This document may refer to hardware, software and/or documentation owned by one or more third parties ("third-party materials"). Use of such third-party materials shall be governed by all restrictions and obligations applicable thereto.

We make no warranty or representation, either express or implied, regarding the third-party materials, including but not limited to any implied or statutory, warranties of merchantability or fitness for a particular purpose, quiet enjoyment, system integration, information accuracy, and non-infringement of any third-party intellectual property rights with regard to the licensed technology or use thereof. Nothing herein constitutes a representation or warranty by us to either develop, enhance, modify, distribute, market, sell, offer for sale, or otherwise maintain production of any our products or any other hardware, software, device, tool, information, or product. We moreover disclaim any and all warranties arising from the course of dealing or usage of trade.

Privacy Policy

To implement module functionality, certain device data are uploaded to Quectel's or third-party's servers, including carriers, chipset suppliers or customer-designated servers. Quectel, strictly abiding by the relevant laws and regulations, shall retain, use, disclose or otherwise process relevant data for the purpose of performing the service only or as permitted by applicable laws. Before data interaction with third parties, please be informed of their privacy and data security policy.

Disclaimer

a) We acknowledge no liability for any injury or damage arising from the reliance upon the information.
b) We shall bear no liability resulting from any inaccuracies or omissions, or from the use of the information contained herein.
c) While we have made every effort to ensure that the functions and features under development are free from errors, it is possible that they could contain errors, inaccuracies, and omissions. Unless otherwise provided by valid agreement, we make no warranties of any kind, either implied or express, and exclude all liability for any loss or damage suffered in connection with the use of features and functions under development, to the maximum extent permitted by law, regardless of whether such loss or damage may have been foreseeable.
d) We are not responsible for the accessibility, safety, accuracy, availability, legality, or completeness of information, advertising, commercial offers, products, services, and materials on third-party websites and third-party resources.

Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-02-11	Shiye ZHU/ Jeff SHEN	Creation of the document
1.0	2023-09-19	Shihao HUANG/ Jeff SHEN/ Jerry LIN	First official release
1.1	2023-11-24	Shihao HUANG/ Jeff SHEN/ Jerry LIN	1. Updated GNSS performance (Table 46). 2. Updated recommended footprint (Figure 44).

Contents

Table Index

Figure Index

1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and cost-effectiveness

This document defines the EG915N series module in QuecOpen® solution and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up wireless applications with the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument, and so on, it indicates that the function, feature, interface, pin, AT command, argument, and so on, is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

The module is an SMD type module which is engineered to meet most of the requirements for M2M applications such as:

- Automation
- Metering
- Tracking system
- Smart safety
- Router
- Wireless POS
- Mobile computing device
- PDA phone
- Tablet PC

Table 2: Brief Introduction

EG915N Series	
Packaging	LGA
Pins count	126
Dimensions	(23.6 ±0.2) mm × (19.9 ±0.2) mm × (2.4 ±0.2) mm
Weight	Approx. 2.46 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

	EG915N-EU	EG915N-LA	EG915N-EA
LTE-FDD	B1/B3/B7/B8/B20	B2/B3/B4/B5/B7/B8/B28/B66	B1/B3/B7/B8/B20/B28
GSM	EGSM900/DCS1800	GSM850/EGSM900/	EGSM900/DCS1800

		DCS1800/PCS1900	
GNSS (optional)	GPS/GLONASS/Galileo/ BDS/QZSS	GPS/GLONASS/Galileo/ BDS/QZSS	GPS/GLONASS/Galileo/ BDS/QZSS

2.2. Key Features

Table 4: Key Features

Features	Description
Power Supply	● Supply voltage: 3.4–4.5 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM card and ME; ME by default
(U)SIM Interfaces	● Supports (U)SIM card: 1.8/3.0 V ● Supports Dual SIM Single Standby
USB Interface	● Compliant with USB 2.0 specification (slave mode only), with data transmission rates up to 480 Mbps ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial drivers for: Windows 7/8/8.1/10/11, Linux 2.6–6.5, Android 4.x–13.x, etc.
UART	**Main UART:** ● Used for data transmission and AT command communication ● Baud rate: 115200 bps by default ● Supports RTS and CTS hardware flow control **Auxiliary UART:** ● Used for communication with peripheral ● Baud rate: 115200 bps ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for the output of partial logs and GNSS NMEA message ● Baud rate:115200 bps
SPI	● Supports slave mode* and master mode with a maximum clock frequency of 26 MHz ● Multiplexed from auxiliary UART
PCM Interface	● Used for audio function with an external codec ● Short frame mode: module can only be used as a master device

I2C Interface	● One I2C interface ● Complies with I2C bus specification version
Audio Features	● Supports one digital audio interface: PCM interface ● Supports one analog audio input and one analog audio output ● HR/FR/EFR/AMR/AMR-WB ● Supports echo cancellation and noise suppression
ADC Interfaces	● EG915N-EU supports two Analog-to-Digital Converter (ADC) interfaces ● EG915N-LA/-EA support one Analog-to-Digital Converter (ADC) interfaces
USB_BOOT	Supports one download control interface
Camera Interface	● Provides one camera interface ● Supports up to 0.3 MP ● Supports the single data trace or dual data trace transmission of SPI
LCM Interface	● Supports an LCD display module with a maximum resolution of 240 × 320 ● Supports SPI four-wire single data trace transmission ● Supports RGB565 format output
Matrix Keypad Interfaces	Supports 4 × 4 matrix keypad interfaces
Transmitting Power	● Class 4 (33 dBm ±2 dB) for GSM850 ● Class 4 (33 dBm ±2 dB) for EGSM900 ● Class 1 (30 dBm ±2 dB) for DCS1800 ● Class 1 (30 dBm ±2 dB) for PCS1900 ● Class E2 (27 dBm ±3 dB) for GSM850 8-PSK ● Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK ● Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK ● Class E2 (26 dBm ±3 dB) for PCS1900 8-PSK ● Class 3 (23 dBm ±2 dB) for LTE-FDD bands
LTE Features	● Supports up to 3GPP Rel-9 non-CA Cat 1 FDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● LTE-FDD: Max. 10 Mbps (DL), Max. 5 Mbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1–4 ● Max. 85.6 kbps (DL), Max. 85.6 kbps (UL) **EDGE:** ● Supports EDGE multi-slot class 12 ● Supports GMSK and 8-PSK for different MCS ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 236.8 kbps (DL), Max. 236.8 kbps (UL)

Internet Protocol Features	Supports TCP/UDP/NTP/NITZ/FTP/HTTP/PING/HTTPS/FTPS/SSL/FILE /MQTT/MMS protocols
AT Commands	Compliant with *3GPP TS 27.007, 3GPP TS 27.005* and Quectel enhanced AT commands
Network Indication	NET_STATUS to indicate the network connectivity status
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● GNSS antenna interface (ANT_GNSS) [1] ● 50 Ω characteristic impedance
Position Fixing	● Supports Wi-Fi scan and shares the main antenna ● Supports GNSS positioning [1]
Temperature Range	● Operating temperature range: -35 to +75 °C [2] ● Extended temperature range: -40 to +85 °C [3] ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	Via USB interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS Directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- Memory
- Radio frequency
- Peripheral interfaces

[1] GNSS function is optional for the module. Only the module with built-in GNSS function can support GNSS positioning function.
[2] Within operating temperature range, the module is 3GPP compliant.
[3] Within extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

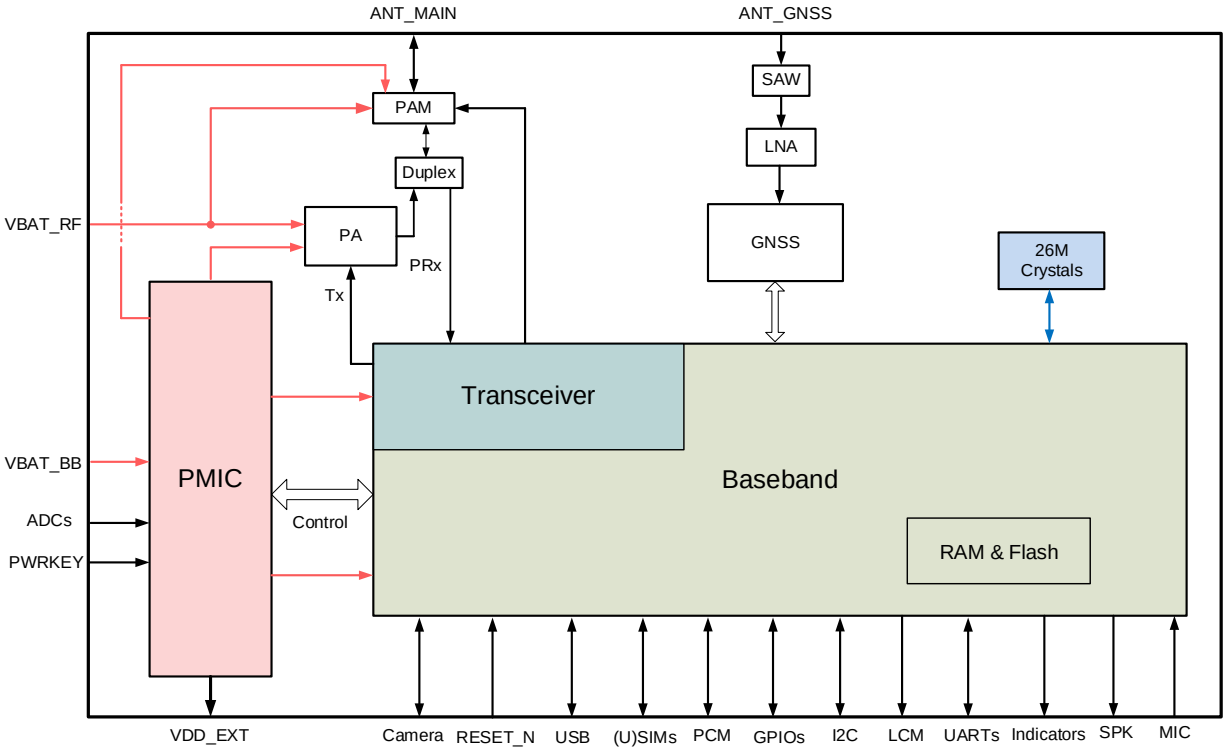


Figure 1: Functional Diagram of EG915N-EU

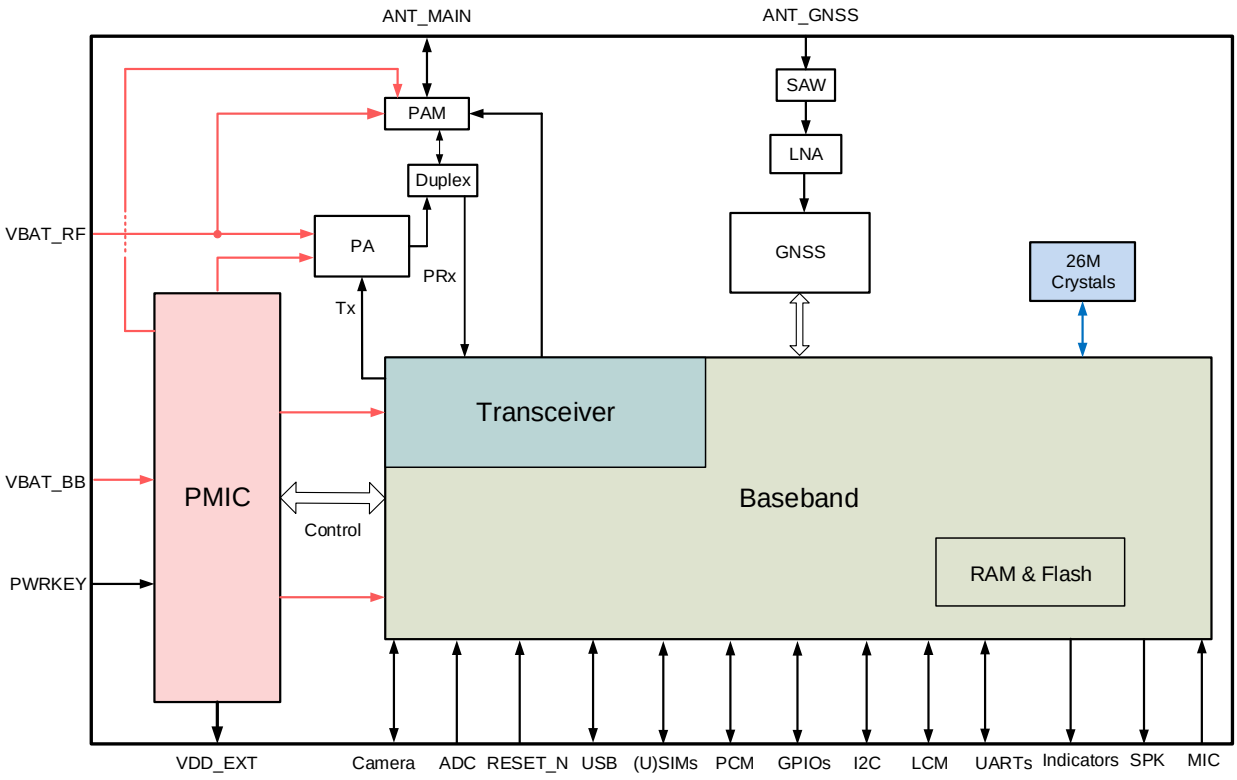


Figure 2: Functional Diagram of EG915N-LA and EG915N-EA

2.4. Pin Assignment

The following figure shows the pin assignment of the module.

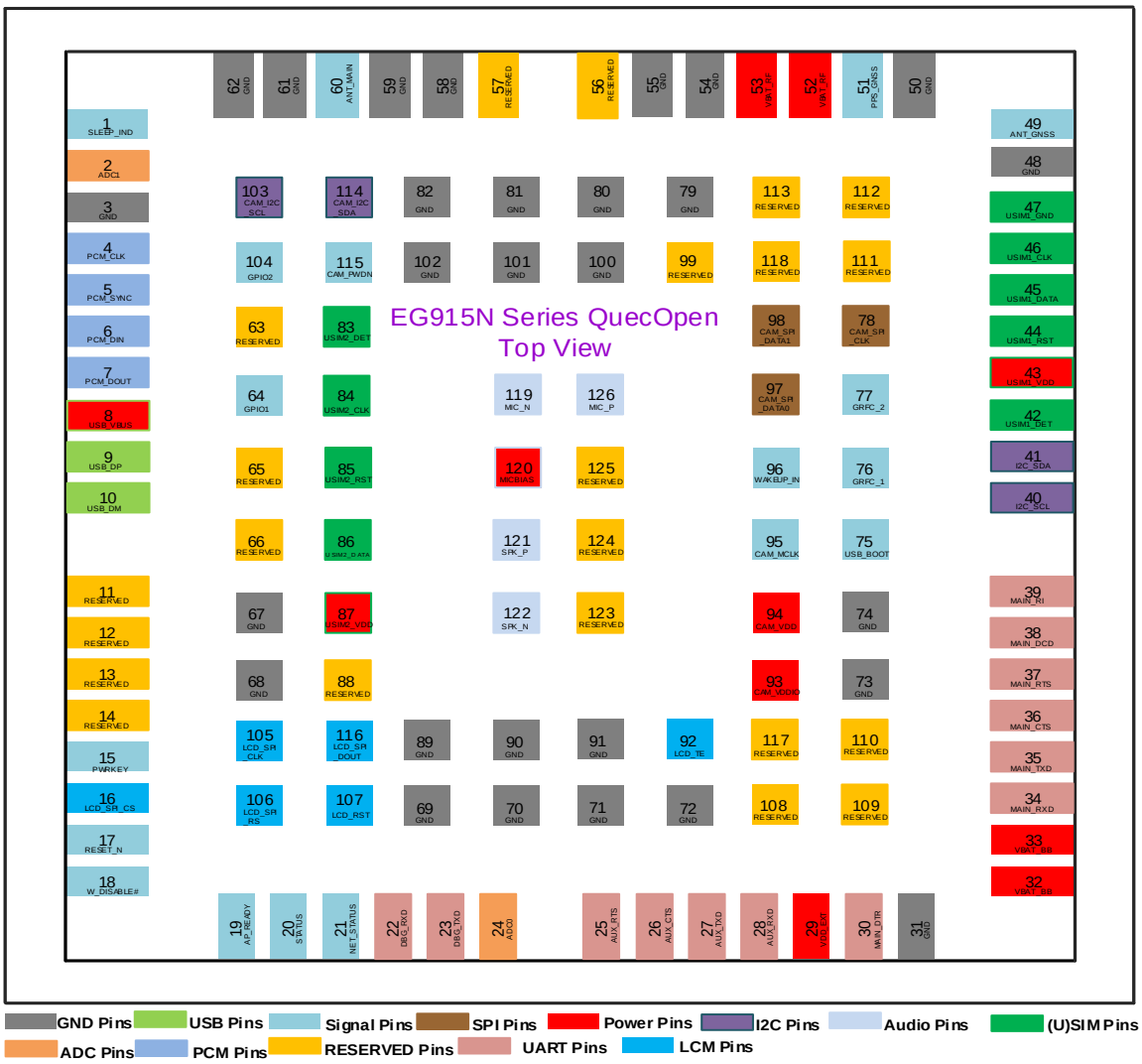


Figure 3: Pin Assignment (Top View)

NOTE

1. USB_BOOT cannot be pulled up to high level before the module starts up successfully.
2. Keep unused and RESERVED pins open.
3. GNSS function is optional. ANT_GNSS and PPS_GNSS are pins for the module with built-in GNSS function.
4. Ensure that there is a complete reference ground plane below the module, and the ground plane is as close to the module layer as possible. At least a 4-layer board design is recommended.

2.5. Pin Description

The following tables show the pin definition and description of the module.

Table 5: Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	Vmax = 4.5 V Vmin = 3.4 V Vnom = 3.8 V	External power supply must be provided with sufficient current of at least 0.8 A. It is recommended to add an external TVS diode. A test point is recommended to be reserved.
VBAT_RF	52, 53	PI	Power supply for the module's RF part		External power supply must be provided with

					sufficient current of at least 2.2 A. It is recommended to add an external TVS diode. A test point is recommended to be reserved.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
Power Supply Output					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. Test point is recommended to be reserved.
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module	V_{IL}max = 0.5 V Vnom = VBAT	VBAT power domain. A test point is recommended to be reserved.
RESET_N	17	DI	Reset the module	V_{IL}max = 0.5 V Vnom = 1.8 V	Active low. 1.8 V power domain. A test point is recommended to be reserved if unused.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SLEEP_IND	1	DO	Indicate the module's sleep mode	1.8 V	If unused, keep them open.
STATUS	20	DO	Indicate the module's operation status		
NET_STATUS	21	DO	Indicate the module's network activity status		

USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	Test point must be reserved.
USB_DP	9	AIO	USB differential data (+)		Requires differential impedance of 90 Ω. USB 2.0 compliant. Test points must be reserved.
USB_DM	10	AIO	USB differential data (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V	If unused, keep it open.
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_O$max = 50 mA 1.8/3.0 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_RST	44	DO	(U)SIM1 card reset	USIM1_VDD 1.8/3.0 V	
USIM1_DATA	45	DIO	(U)SIM1 card data		
USIM1_CLK	46	DO	(U)SIM1 card clock		
USIM1_GND	47	-	Specified ground for (U)SIM1		Connect to main GND of PCB.
USIM2_DET*	83	DI	(U)SIM2 card hot-plug detect	1.8 V	If unused, keep it open.
USIM2_CLK	84	DO	(U)SIM2 card clock	USIM2_VDD 1.8/3.0 V	
USIM2_RST	85	DO	(U)SIM2 card reset		
USIM2_DATA	86	DIO	(U)SIM2 card data		
USIM2_VDD	87	PO	(U)SIM2 card power supply	$I_O$max = 50 mA 1.8/3.0 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
Main UART					

Pin Nam	Pin No.	I/O	Description	DC Characteristics	Comment
MAIN_DTR	30	DI	Main UART data terminal ready	1.8 V	If unused, keep them open
MAIN_RXD	34	DI	Main UART receive		
MAIN_TXD	35	DO	Main UART transmit		
MAIN_CTS	36	DO	Request to send signal from the module		Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	37	DI	Request to send signal to the module		Connect to MCU's RTS. If unused, keep it open.
MAIN_DCD	38	DO	Main UART data carrier detect		If unused, keep them open.
MAIN_RI*	39	DO	Main UART ring indication		
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART receive	1.8 V	Test points must be reserved.
DBG_TXD	23	DO	Debug UART transmit		
Auxiliary UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_RTS	25	DI	Request to send signal to the module	1.8 V	Connect to MCU's RTS. If unused, keep it open.
AUX_CTS	26	DO	Request to send signal from the module		Connect to MCU's CTS. If unused, keep it open.
AUX_TXD	27	DO	Auxiliary UART transmit		If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive		
ADC Interfaces					
Pin Nam	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

ADC0	24	AI	General-purpose ADC interface	Voltage range: 0 V to VBAT_BB	If unused, keep them open.
ADC1	2	AI			
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	40	OD	I2C serial clock	1.8 V	An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK	4	DO	PCM clock	1.8 V	If unused, keep them open.
PCM_SYNC	5	DO	PCM data frame sync		
PCM_DIN	6	DI	PCM data input		
PCM_DOUT	7	DO	PCM data output		
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MICBIAS	120	PO	Bias voltage output for microphone		If unused, keep them open.
MIC_N	119	AI	Microphone analog input (-)		
MIC_P	126	AI	Microphone analog input (+)		
SPK_P	121	AO	Analog audio differential output (+)		The interface can drive 32 Ω earpiece with power rate at 37 mW @ THD = 1 %. It can also be used to drive external power amplifier devices if the output power rate cannot meet the demand. If unused, keep them open.
SPK_N	122	AO	Analog audio differential output (-)		

Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface		50 Ω characteristic impedance.
ANT_GNSS	49	AI	GNSS antenna interface		50 Ω characteristic impedance. If unused, keep it open.
Antenna Tuner Control Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC_1	76	DO	Generic RF Controller		If unused, keep them open.
GRFC_2	77	DO			
Camera Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CAM_MCLK	95	DO	Master clock of camera	1.8 V	If unused, keep it open.
CAM_I2C_SCL	103	OD	I2C clock of camera		Pull each of them up to 1.8 V power domain with an external resistor. If unused, keep them open.
CAM_I2C_SDA	114	OD	I2C data of camera		
CAM_SPI_CLK	78	DI	SPI clock of camera		If unused, keep them open.
CAM_SPI_DATA0	97	DI	SPI data 0 of camera		
CAM_SPI_DATA1	98	DI	SPI data 1 of camera		
CAM_PWDN	115	DO	Power down of camera		
CAM_VDD	94	PO	Analog power supply of camera	Vnom = 2.8 V	Power supply of camera. If unused, keep them open.
CAM_VDDIO	93	PO	Digital power supply of camera	Vnom = 1.8 V	
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

LCD_TE	92	DI	LCD tearing effect	1.8 V	If unused, keep them open.
LCD_RST	107	DO	LCD reset		
LCD_SPI_CS	16	DO	LCD chip select		
LCD_SPI_CLK	105	DO	LCD clock		
LCD_SPI_RS	106	DO	LCD register select		
LCD_SPI_DOUT	116	DO	LCD data output		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN*	96	DI	Wake up the module	1.8 V	If unused, keep them open.
AP_READY	19	DI	Application processor ready		
W_DISABLE#	18	DI	Airplane mode control		In low voltage level, module can enter airplane mode. If unused, keep it open. Pull-up by default.
USB_BOOT	75	DI	Force the module into emergency download mode		Active high. A test point is recommended to be reserved.
PPS_GNSS	51	DO	PPS output		Cannot pull it down when GNSS function is active.
GPIOs					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	64	DIO	General-purpose input/output	1.8 V	If unused, keep them open.
GPIO2	104	DIO			
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	11–14, 56, 57, 63, 65, 66, 88, 99, 108–113, 117, 118, 123–125				Keep them open.

NOTE

1. For more information about GPIO, see ***document [1]*** for details.
2. GNSS function is optional. ANT_GNSS and PPS_GNSS are pins for the module with built-in GNSS function. See ***Chapter 5.2*** for details about GNSS antenna interfaces.

2.6. EVB Kit

To help you develop applications with the module, Quectel provides an evaluation board (LTE OPEN EVB), with accessories to develop or test the module. For more details, see ***document [2]***.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Overview of Operating Modes

Modes	Details	
Full Functionality Mode	Idle	Software is active. The module remains registered on the network, and is ready to send and receive data.
	Voice/Data	Network connection is ongoing. Power consumption is decided by network setting and data transmission rate.
Minimum Functionality Mode	*ql_dev_set_modem_fun()* can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	*ql_dev_set_modem_fun()* or driving W_DISABLE# pin low can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	Power consumption of the module is reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power down Mode	In this mode, the module's power supply is cut off by its power management IC. The software is inactive, while the VBAT_RF and VBAT_BB pins are still powered.	

NOTE

For more information about the API, see ***document [3]***.

3.2. Sleep Mode

With DRX technology, power consumption of the module will be reduced to a minimal level.

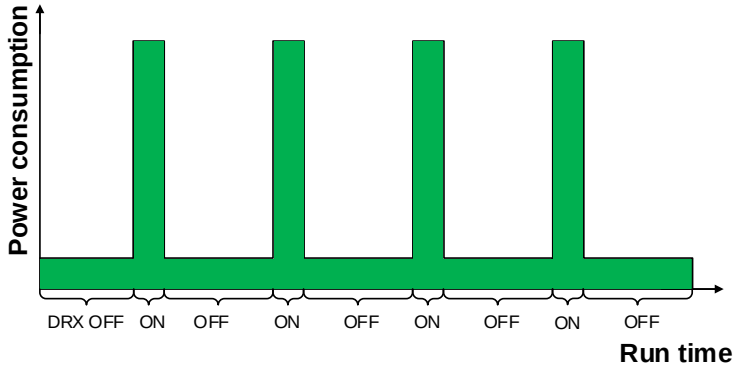


Figure 4: DRX Run Time and Current Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

The following three conditions should be met to set the module into sleep mode.

- Enable sleep function through *ql_autosleep_enable()*.
- All GPIOs configured as interrupt wake-up function are in non-wake-up state.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

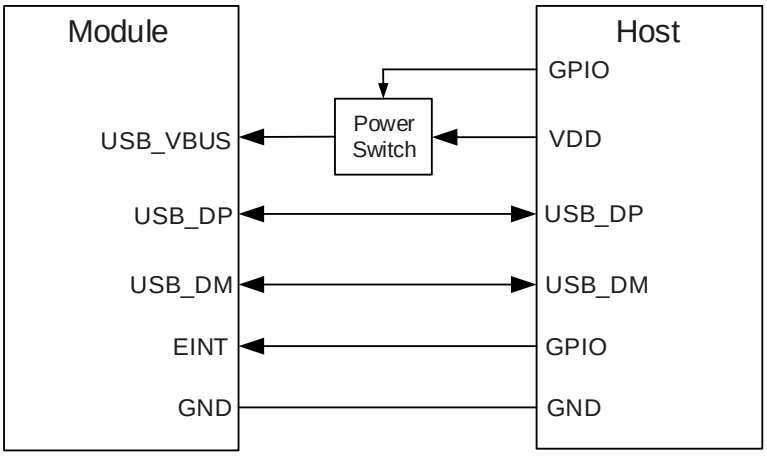


Figure 5: Sleep Mode Application without Suspend Function

You can wake up the module by turning on the power switch to power the USB_VBUS or by using GPIO to interrupt the module.

NOTE

1. Pay attention to the level match shown in dotted line between the module and the host in the circuit diagram.
2. For more information about the API, see ***document [3]***.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all API related to it will be inaccessible. This mode can be set via following ways:

Software:

ql_dev_set_modem_fun() provides choices of the functionality level through setting the parameter *function* to:

- *QL_DEV_MODEM_FULL_FUN*: Minimum functionality mode. Both RF and (U)SIM functions are disabled.
- *QL_DEV_MODEM_FULL_FUN*: Full functionality mode (by default).
- *QL_DEV_MODEM_DISBLE_TRANSMIT_AND_RECEIVE_RF_CIRCUITS*: Airplane mode (disable RF transmitter and receiver circuit).

NOTE

For more details about API, see ***document [3]***.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides four VBAT pins dedicated to the connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

Table 8: Power Supply and GND Pins

Pin Name	Pin No.	I/O	Description	Comment
VBAT_RF	52, 53	PI	Power supply for the module's RF part	External power supply must be provided with sufficient current of at least 2.2 A. It is recommended to add an external TVS diode. A test point is recommended to be reserved.
VBAT_BB	32, 33		Power supply for the module's BB part	External power supply must be provided with sufficient current of at least 0.8 A. It is recommended to add an external TVS diode. A test point is recommended to be reserved.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102			

3.4.2. Voltage Stability Requirements

The power supply range of the module is from 3.4 V to 4.5 V. Make sure the input voltage never drops below 3.4 V. The following figure shows the voltage drop during burst transmission.

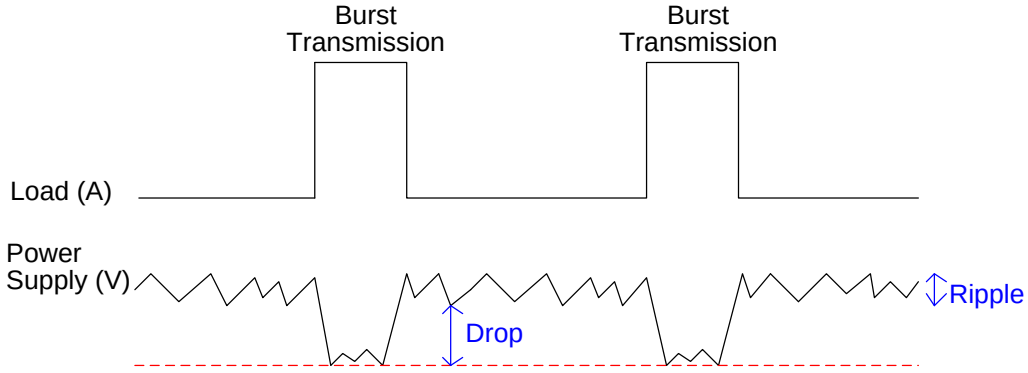


Figure 6: Power Supply Limits during Burst Transmission

To decrease the voltage drop, use bypass capacitors of about 100 µF with low ESR (ESR ≤ 0.7 Ω) and reserve a multi-layer ceramic chip (MLCC) capacitor array due to their ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. When the external power supply is connected to the module, VBAT_BB and VBAT_RF need to be routed in star configuration. The width of VBAT_BB trace should not be less than 1 mm and the width of the VBAT_RF trace should not be less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

To avoid the ripple and surge and ensure the stability of the power supply to the module, add a TVS diode with V_{RWM} = 4.7 V, low-clamp voltage and peak pulse current Ipp at the front end of the power supply.

The following figure shows the star configuration of the power supply.

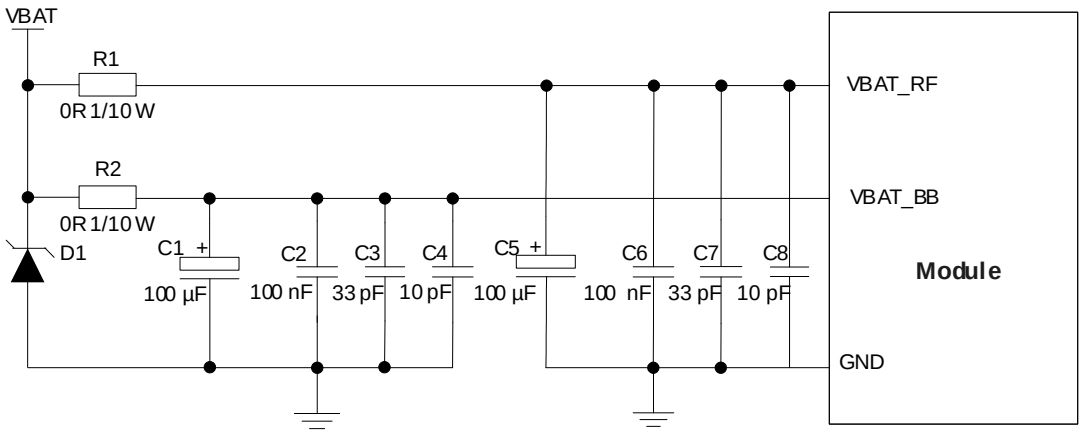


Figure 7: Star Configuration of Power Supply

3.4.3. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 3 A. If the voltage difference between input voltage and the desired output VBAT is small, it is suggested to use an LDO; if the voltage difference is large, then a buck converter is suggested to use.

The following figure illustrates a reference design for 5 V input power supply.

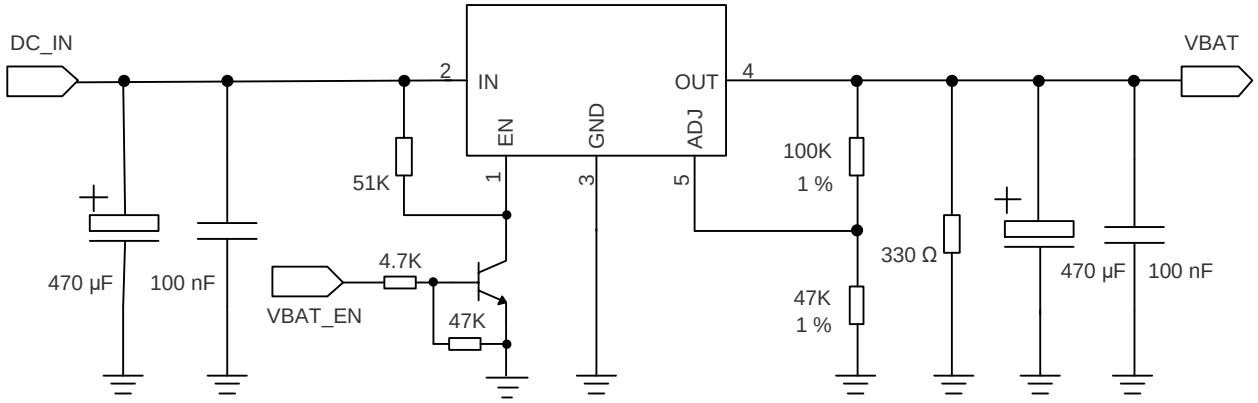


Figure 8: Reference Circuit of Power Supply

3.4.4. Power Supply Voltage Detection

Use *ql_get_battery_vol()* to monitor or read VBAT voltage. For more details, see ***document [5]***.

3.5. Turn On

3.5.1. Turn on with PWRKEY

Table 9: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	VBAT power domain. Pull down PWRKEY to Turn on/off the module. A test point is recommended to be reserved.

When the module is in power down mode, it can be turned on to normal mode by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

A simple reference circuit is illustrated in the following figure.

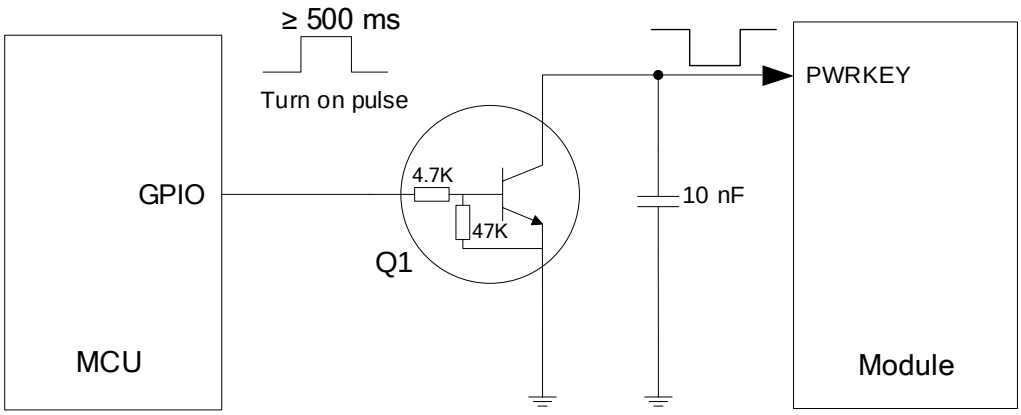


Figure 9: Turning on the Module with Driving Circuit

Another way to control PWRKEY is by using a push button directly. When pressing the button, an electrostatic strike may be generated from finger. Therefore, a TVS diode should be placed near the push button for ESD protection.

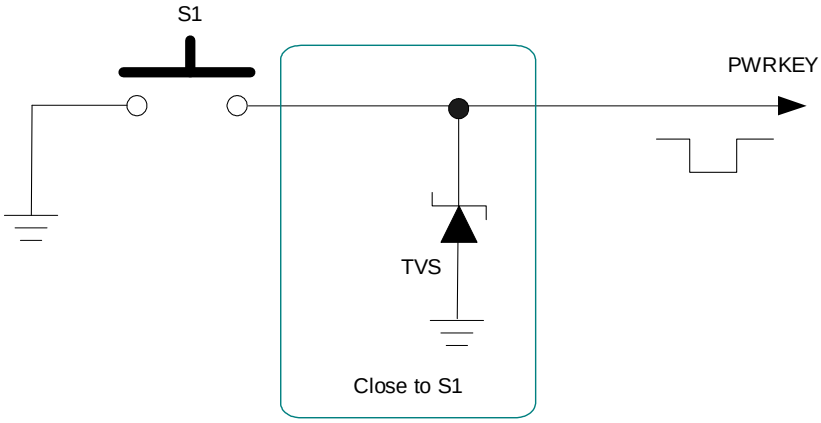


Figure 10: Turning on the Module with a Button

The timing of turning on the module is illustrated in the following figure.

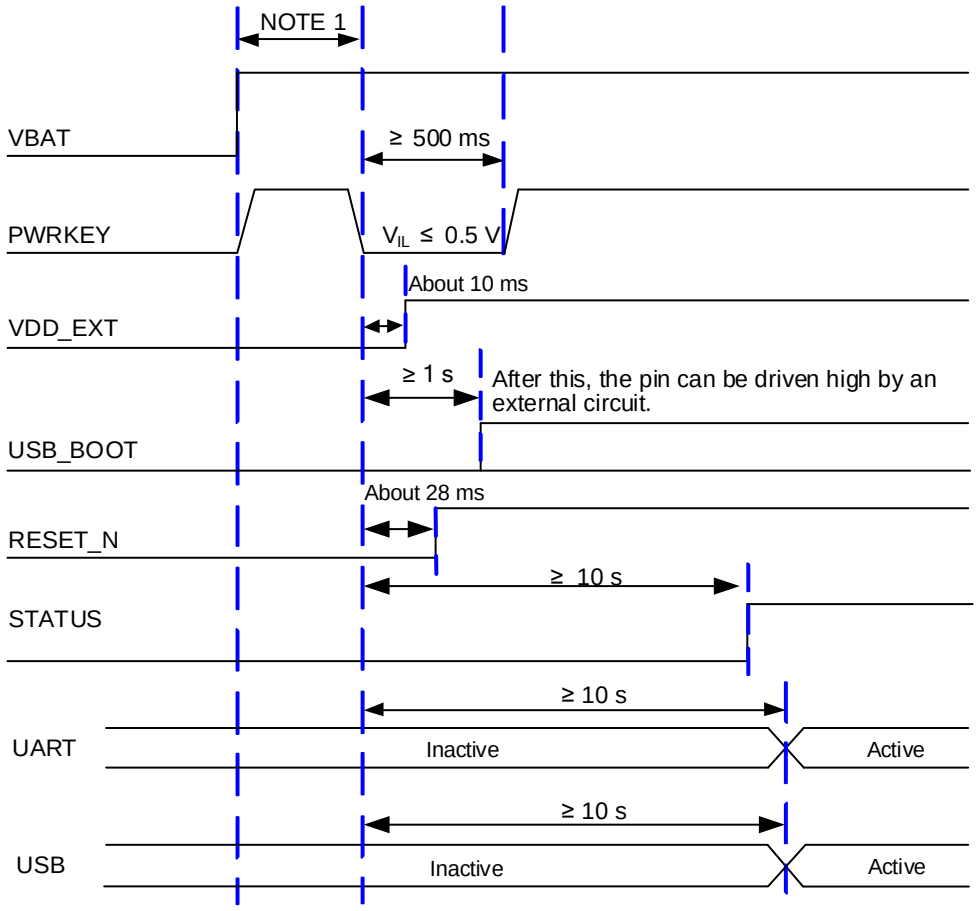


Figure 11: Timing of Turning on Module

NOTE

1. Ensure that VBAT is stable for at least 30 ms before pulling down the PWRKEY.
2. If the module needs to turn on automatically but does not need turn-off function, PWRKEY can be driven low directly to ground with a recommended 4.7 kΩ resistor.

3.6. Turn Off

The following procedures can be used to turn off the module normally:

- Use the PWRKEY pin.
- Execute the related API.

3.6.1. Turn off with PWRKEY

Drive PWRKEY pin for at least 650 ms and then release PWRKEY. After this, the module executes power-down procedure. The power-down scenario is illustrated in the following figure.

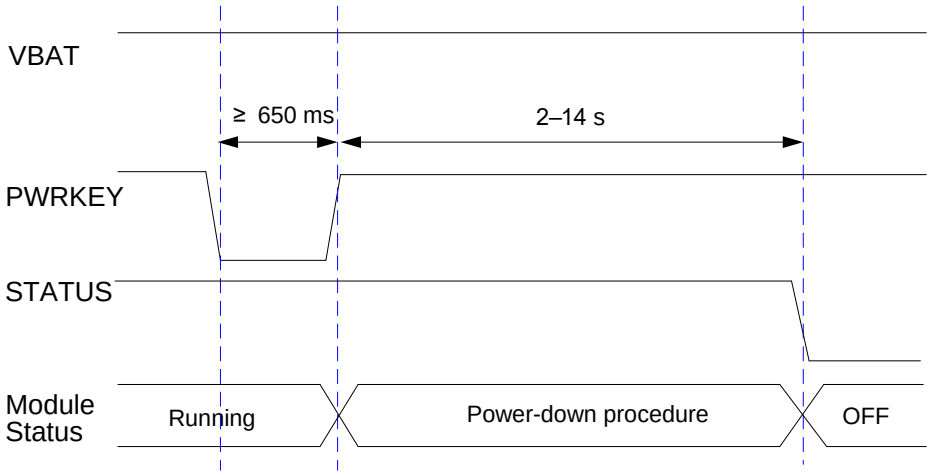


Figure 12: Power-down Timing

3.6.2. Turn off with API

It is also a safe way to use *ql_power_down()* to turn off the module, which is similar to the procedure of turning off the module via PWRKEY pin. See ***document [6]*** for details about the API.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module by PWRKEY or API, can you cut off the power supply.
2. When turning off module with the API, keep PWRKEY at high level. Otherwise, the module will be turned on again after successful turn-off.

3.7. Reset

The module can be reset by driving the RESET_N low for at least 300 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Reset the module	Active low. 1.8 V power domain. Test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. You can use an open drain/collector driver or button to control the RESET_N.

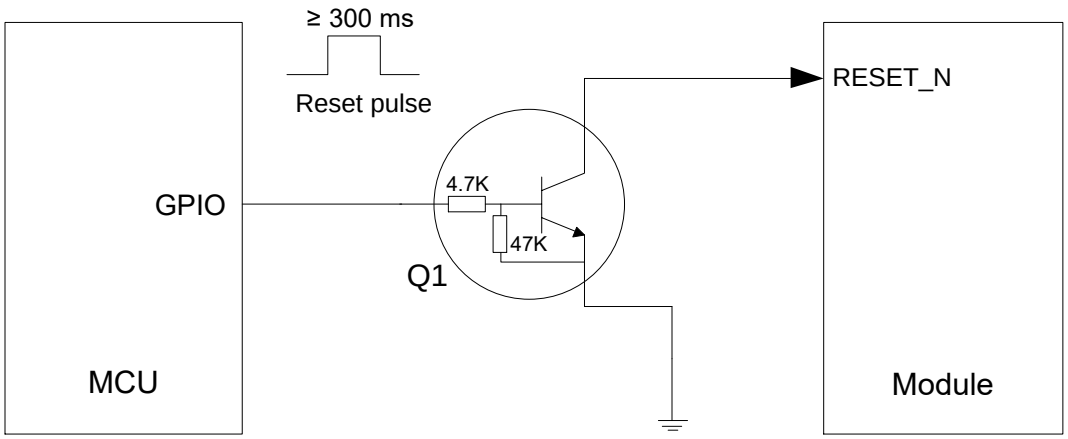


Figure 13: Reference Circuit of RESET_N with Driving Circuit

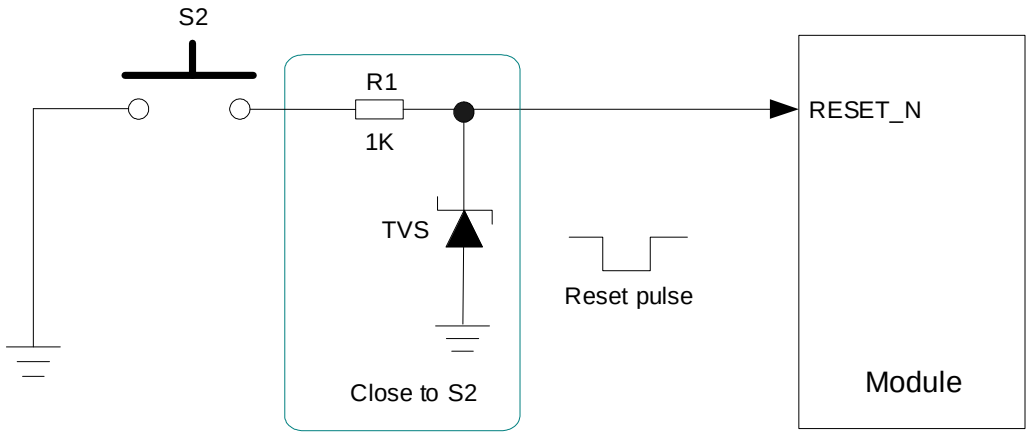


Figure 14: Reference Circuit of RESET_N with a Button

The reset scenario is illustrated in the following figure.

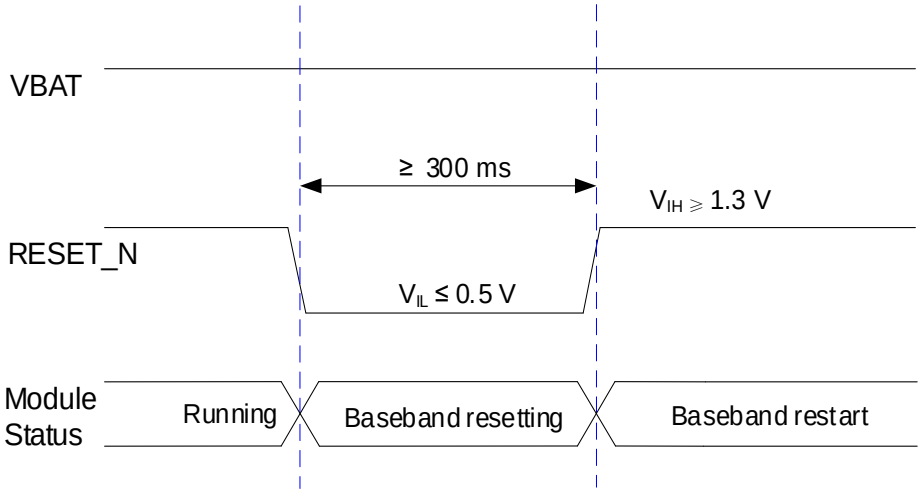


Figure 15: Timing of Resetting the Module

NOTE

1. Ensure that the load capacitance on PWRKEY and RESET_N does not exceed 10 nF.
2. RESET_N only resets the internal baseband chip of the module and does not reset the power management chip.
3. Use RESET_N only when you fail to turn off the module with API and PWRKEY.

4 Application Interfaces

4.1. (U)SIM Interfaces

The (U)SIM interfaces meet ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported. The module supports Dual SIM Single Standby.

Table 11: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_GND	47	-	Specified ground for (U)SIM1	Connect to main GND of PCB.
USIM2_DET*	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_DATA	86	DIO	(U)SIM2 card data	
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.

The module supports (U)SIM1 card hot-plug detection via the USIM1_DET pin and both high and low level detections are supported.

The following figure shows a reference design for (U)SIM card interface with an 8-pin (U)SIM card connector.

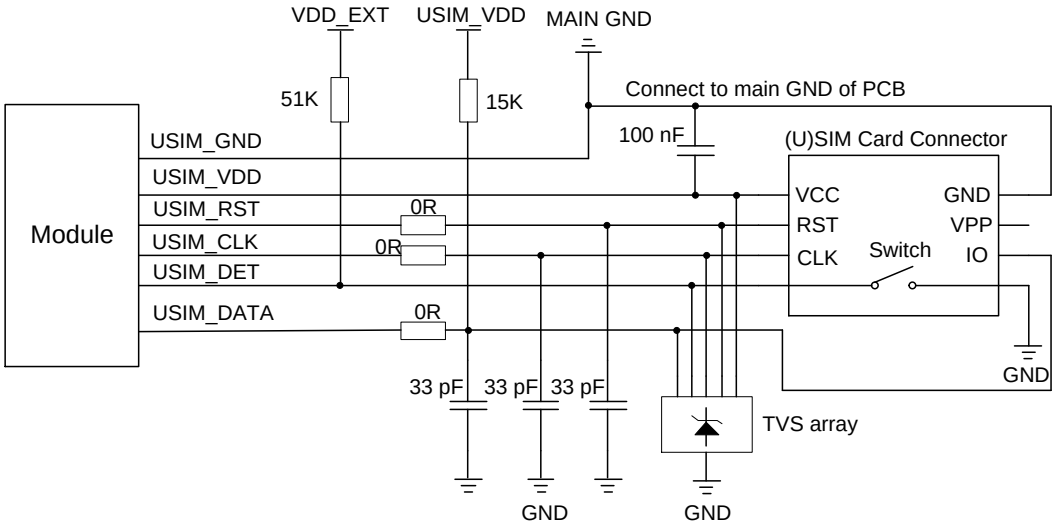


Figure 16: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If the (U)SIM card detection function is not needed, keep USIM_DET disconnected.

A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

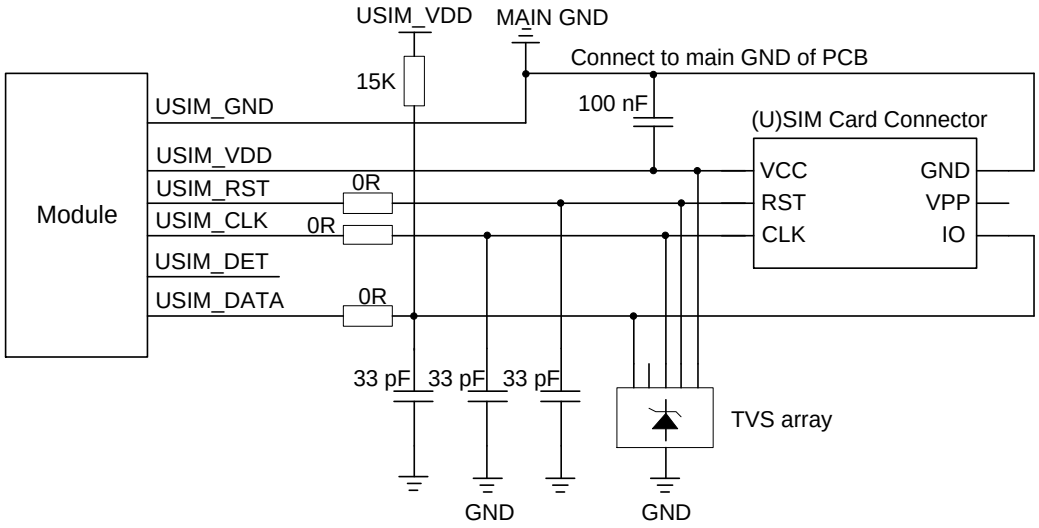


Figure 17: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Place (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- Ensure that the bypass capacitor between USIM_VDD and GND is less than 1 μF, and the capacitor should be close to the (U)SIM card connector.
- Ensure the ground between the module and the (U)SIM card connector is short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential. If the ground is complete on your PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors in parallel on USIM_DATA, USIM_CLK and USIM_RST traces are used for filtering interference of EGSM900. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

4.2. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve in the slave mode. It is used for AT command communication, data transmission, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Typical value: 5.0 V Test point must be reserved.
USB_DP	9	AIO	USB differential data (+)	Requires differential impedance of 90 Ω. USB 2.0 compliant. Test points must be reserved.
USB_DM	10	AIO	USB differential data (-)	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

USB 2.0 interface is recommended to be used for firmware upgrading, and test points must be reserved for debugging.

The following figure shows a reference circuit of USB interface.

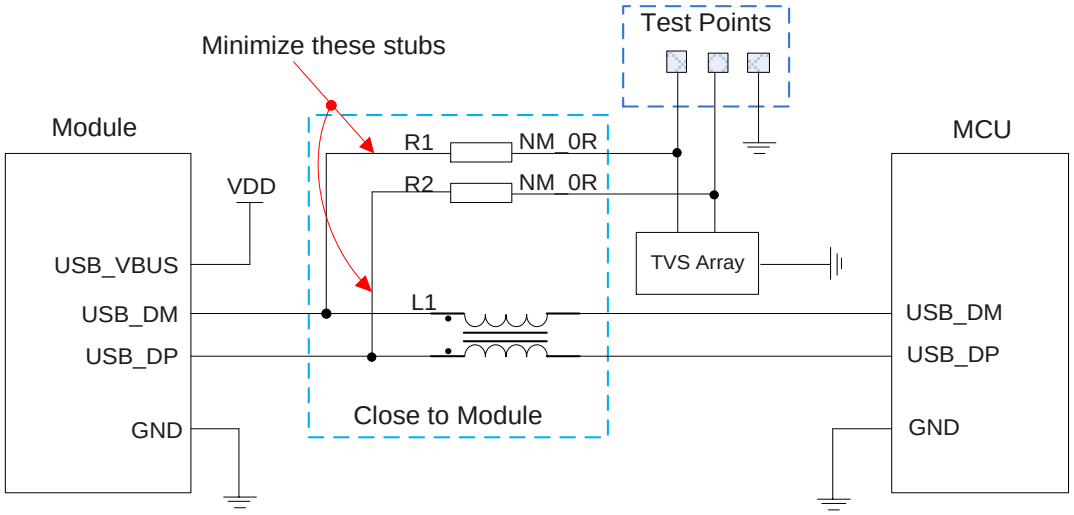


Figure 18: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. To ensure the signal integrity of USB data traces, L1, R1, and R2 must be placed close to the module, and resistors R1 and R2 should be placed close to each other. The extra stubs of trace must be as short as possible.

When designing the USB interface, follow the following principles to meet USB 2.0 specification.

- Route the USB signal traces as a differential pair with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. Route the USB differential traces of equal length in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Pay attention to the selection of the ESD protection components on the USB data trace. Its parasitic capacitance should not exceed 2 pF and should be placed as close as possible to the USB interface.

4.3. UART

The module provides three UART: one main UART, one auxiliary UART and one debug UART. Features of the three UART are described below.

Table 13: UART Information

UART Types	Supported Baud Rates	Default Baud Rates	Functions
Main UART	4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps, 1 Mbps	115200 bps	Data transmission and AT command communication. RTS and CTS hardware flow control is supported.
Auxiliary UART	115200 bps	115200 bps	Communication with peripherals. RTS and CTS hardware flow control is supported.
Debug UART	115200 bps	115200 bps	Partial log and GNSS NMEA message output

Table 14: Pin Definition of Main UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_DTR	30	DI	Main UART data terminal ready	1.8 V power domain. If unused, keep them open.
MAIN_RXD	34	DI	Main UART receive	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_CTS	36	DO	Request to send signal from the module	Connect to MCU's CTS. 1.8 V power domain. If unused, keep it open.
MAIN_RTS	37	DI	Request to send signal to the module	Connect to MCU's RTS. 1.8 V power domain. If unused, keep it open.
MAIN_DCD	38	DO	Main UART data carrier detect	1.8 V power domain. If unused, keep them open.
MAIN_RI*	39	DO	Main UART ring indication	

Table 15: Pin Definition of Auxiliary UART

Pin Name	Pin No.	I/O	Description	Comment
AUX_RTS	25	DI	Request to send signal to the module	Connect to MCU's RTS. 1.8 V power domain. If unused, keep it open.
AUX_CTS	26	DO	Request to send signal from the module	Connect to MCU's CTS. 1.8 V power domain. If unused, keep it open.
AUX_TXD	27	DO	Auxiliary UART transmit	1.8 V power domain. If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive	

Table 16: Pin Definition of Debug UART

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain. Test points must be reserved.
DBG_TXD	23	DO	Debug UART transmit	

The module provides 1.8 V UART. Use a voltage-level translator if the application is equipped with a 3.3 V UART. A voltage-level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

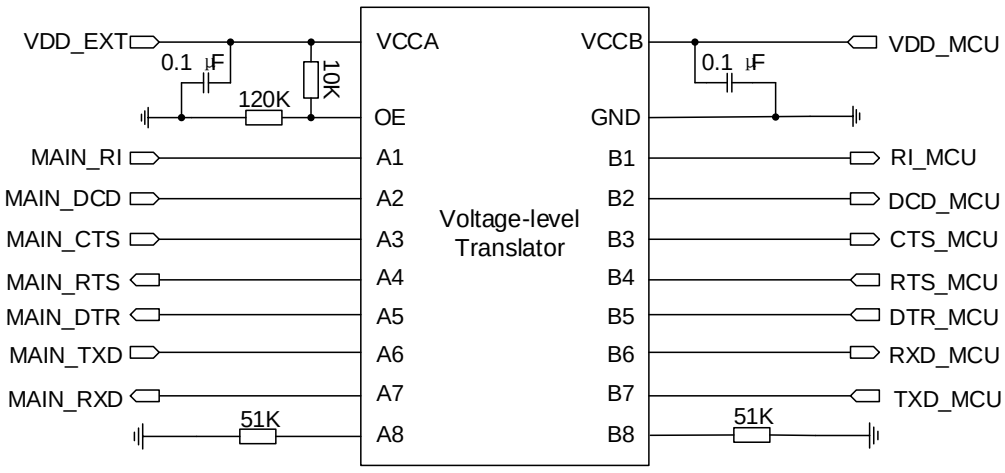


Figure 19: Reference Circuit with Voltage-level Translator

Visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

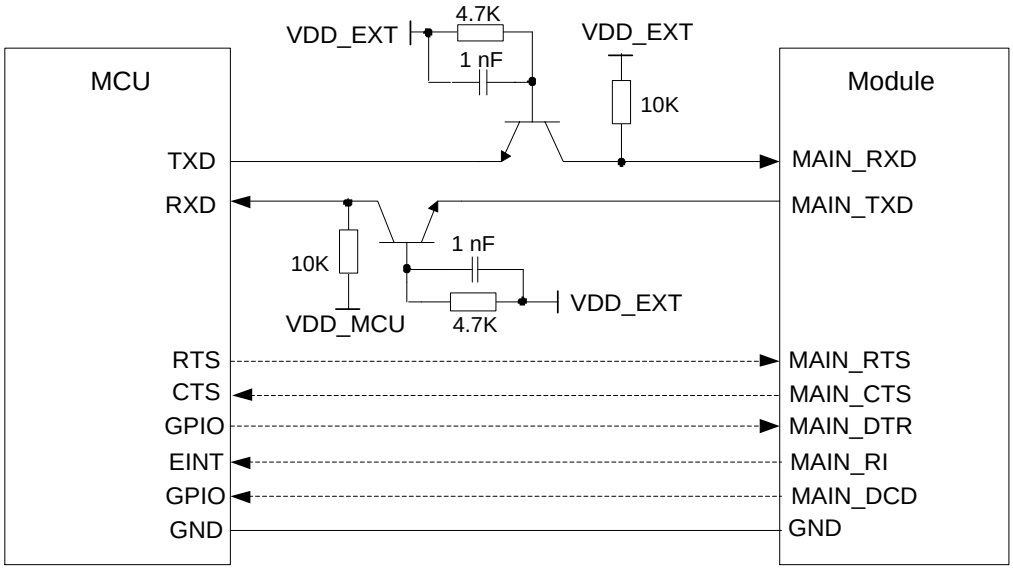


Figure 20: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to MCU's CTS, and the module's RTS is connected to MCU's RTS.

4.4. SPI

The module's SPI supports slave mode* and master mode, the power domain of SPI is 1.8 V and a maximum clock frequency is 26 MHz. The SPI function can be realized by multiplexing from auxiliary UART interface.

Table 17: Pin Description of SPI

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
AUX_RTS	25	SPI1_RXD	DI	SPI data input	1.8 V power domain. If unused, keep them open. When the module is used as master device, SPI1_CLK and SPI1_CS pins are output signals; when the module is used as slave device*, SPI1_CLK and SPI1_CS pins are input signals.
AUX_CTS	26	SPI1_TXD	DO	SPI data output	
AUX_TXD	27	SPI1_CS	DIO	SPI chip select	
AUX_RXD	28	SPI1_CLK	DIO	SPI clock	

The following figure shows a reference design of SPI connected peripherals' circuit:

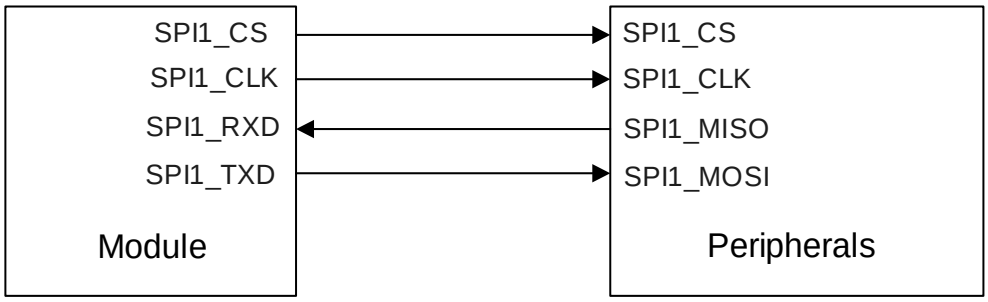


Figure 21: Reference Design of SPI Circuit (Module as Master Device)

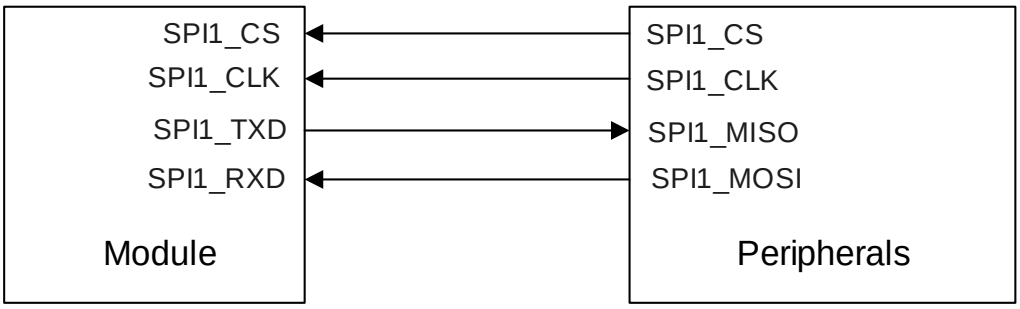


Figure 22: Reference Design of SPI Circuit (Module as Slave Device*)

NOTE

1. The module provides 1.8 V SPI interface. Use a voltage-level translator if the application is equipped with a 3.3 V system.
2. For more information about multiplexing, see ***document [1].***

4.5. PCM and I2C Interfaces

The module provides one I2C interface and one pulse code modulation (PCM) interface for an external codec IC.

Table 18: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_CLK	4	DO	PCM clock	1.8 V power domain. If unused, keep them open.
PCM_SYNC	5	DO	PCM data frame sync	
PCM_DIN	6	DI	PCM data input	
PCM_DOUT	7	DO	PCM data output	
I2C_SCL	40	OD	I2C serial clock	An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data	

PCM interface supports short frame mode: module can only be used as master device.

The module supports 16-bit linear encoding format. The following figure is the short frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 2048 kHz).

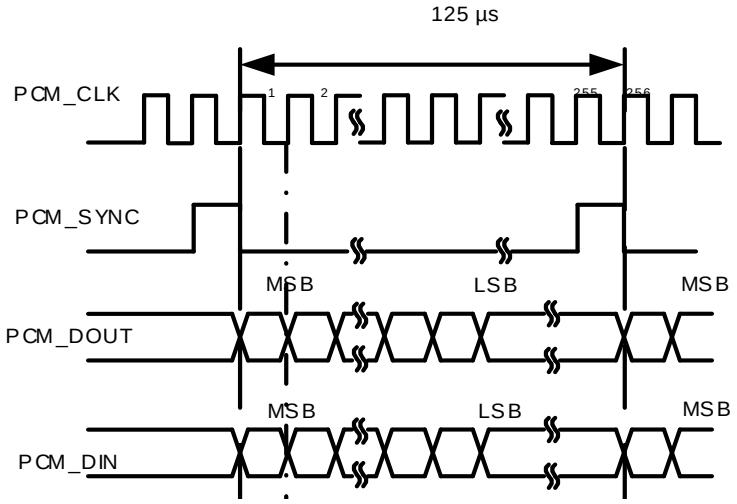


Figure 23: Timing of Short Frame Mode

In short frame mode, data is sampled on the falling edge of PCM_CLK, and sent on the rising edge. The falling edge of PCM_SYNC represents the high effective bit. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz, and 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

The default configuration is short frame mode, PCM_CLK = 2048 kHz, PCM_SYNC = 8 kHz.

The following figure shows a reference design of I2C and PCM interfaces with an external codec IC.

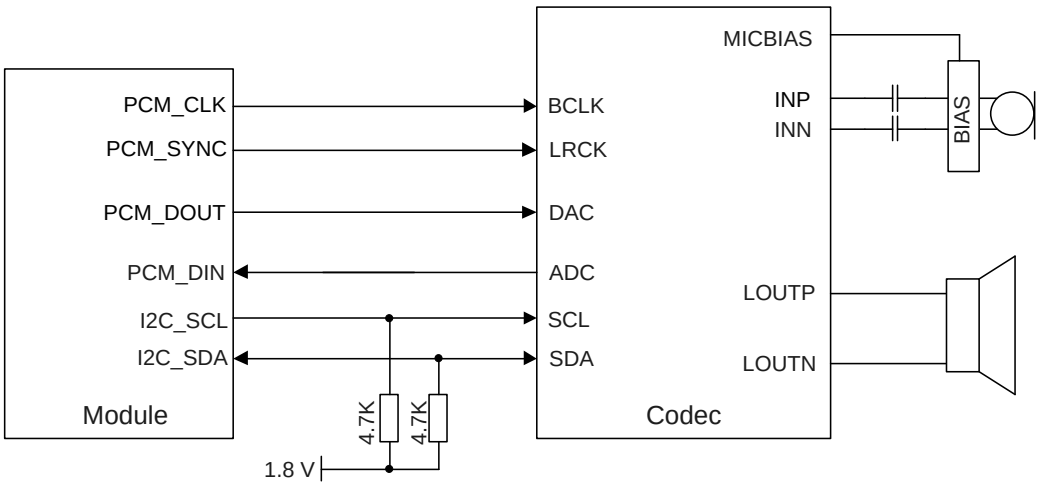


Figure 24: Reference Circuit of I2C and PCM Application with Audio Codec

NOTE

1. It is recommended to reserve an RC (R = 0 Ω, C = 33 pF) circuit on the PCM traces, especially for PCM_CLK.
2. The module can only be used as a master device in applications related to PCM and I2C interfaces.

4.6. Analog Audio Interfaces

The module provides one analog input channel and one analog output channel.

Table 19: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MICBIAS	120	PO	Bias voltage output for microphone	If unused, keep them open.
MIC_P	126	AI	Microphone analog input (+)	
MIC_N	119	AI	Microphone analog input (-)	
SPK_P	121	AO	Analog audio differential output (+)	The interface can drive 32 Ω earpiece with power rate at 37 mW @ THD = 1 %. It can also be used to drive external power amplifier devices if the output power rate cannot meet the demand. If unused, keep them open.
SPK_N	121	AO	Analog audio differential output (-)	

- AI channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- AO channels are differential output channels, which can be applied for output of Earpiece.

4.6.1. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. Without placing this capacitor, TDD noise could be heard. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. Sometimes, even no RF filtering capacitor is required. Therefore, a suitable capacitor can be selected based on the test results. The filter capacitor on the PCB should be placed as close as possible to the audio device or audio interface, and the trace should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To reduce radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces should not be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

4.6.2. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure.

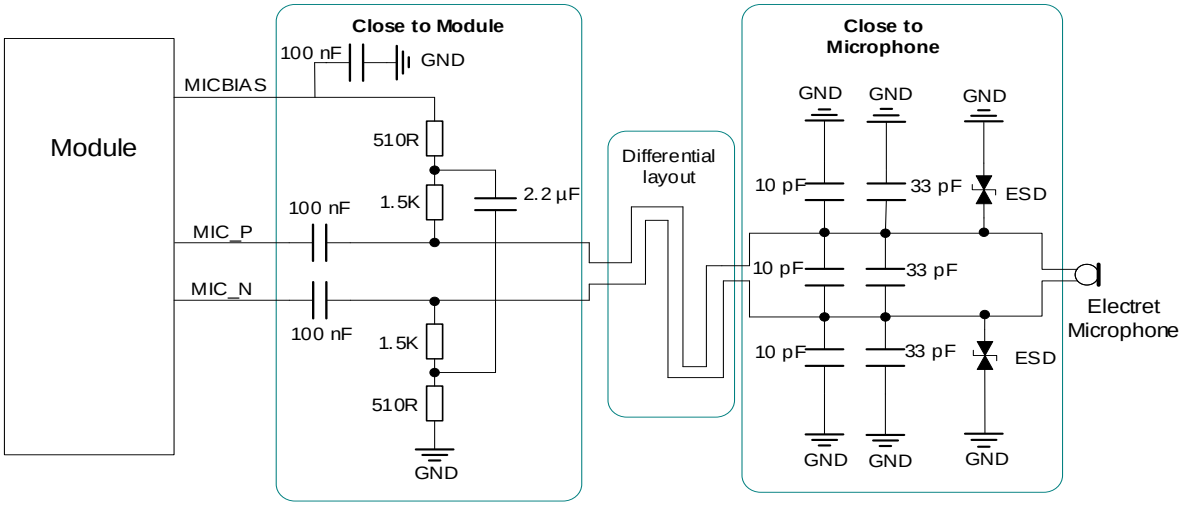


Figure 25: Reference Design for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD protection components used for protecting the MIC.

4.6.3. Earpiece and Loudspeaker Interface Design

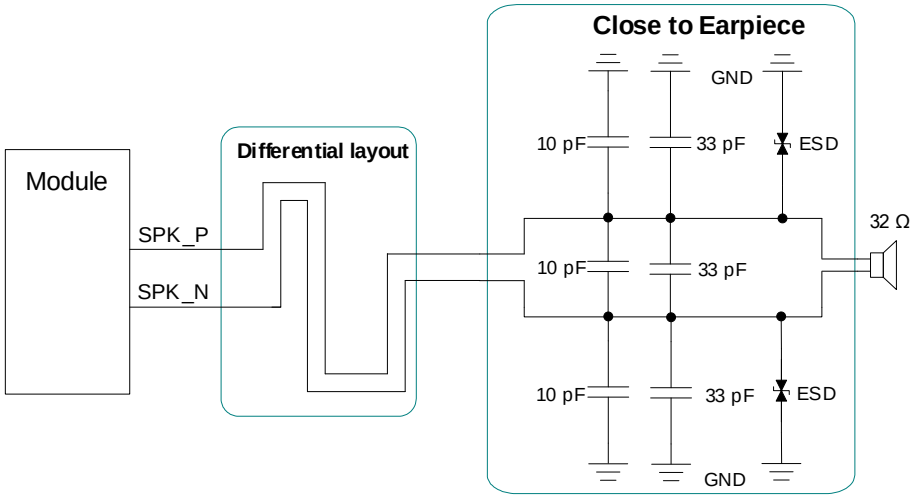


Figure 26: Reference Design for Earpiece Interface

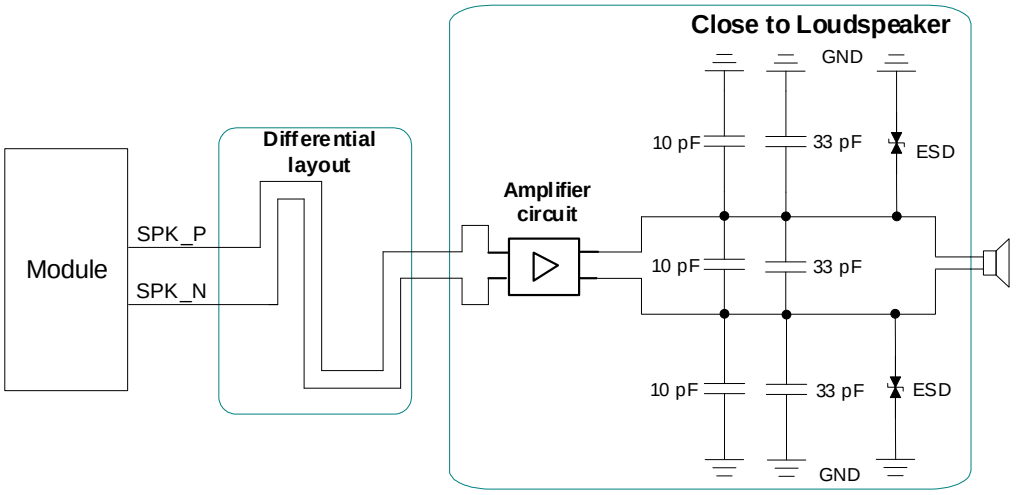


Figure 27: Reference Circuit of External Audio Amplifier Output

For differential input and output audio power amplifiers, please visit http://www.ti.com to obtain the required devices. There are also many audio power amplifiers with the same performance to choose from on the market.

4.7. ADC Interfaces

EG915N-EU provides two analog-to-digital converter (ADC) interfaces.

EG915N-LA and EG915N-EA provide one analog-to-digital converter (ADC) interface.

You can use *ql_adc_read()* to read the voltage value of the ADC. See ***document [5]*** for details about the API.

To improve the accuracy of ADC, surround the trace of ADC with ground.

Table 20: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC1	2	AI	General-purpose ADC interface	If unused, keep them open.
ADC0	24	AI	General-purpose ADC interface	

Table 21: ADC Interfaces' characteristics of EG915N-EU

Parameter	Min.	Typ.	Max.	Unit
ADC0 voltage range	0	-	VBAT_BB	V
ADC1 voltage range	0	-	VBAT_BB	V
ADC resolution	-	-	12	bits

Table 22: ADC Interfaces' characteristics of EG915N-LA and EG915N-EA

Parameter	Min.	Typ.	Max.	Unit
ADC0 voltage range	0	-	VBAT_BB	V
ADC1 voltage range	0	-	VBAT_BB	V
ADC resolution	-	-	10	bits

NOTE

1. It is prohibited to directly supply any voltage to ADC interface when the module is not powered by VBAT.
2. If the collected voltage is greater than 4.5 V, it is recommended to use a resistor divider circuit input for the ADC pin. When designing it, reserve a 1 nF capacitor at both ends of the grounding divider resistor. The capacitor is not mounted by default.

3. EG915N-LA/-EA only support one ADC interface, ADC0 and ADC1 share the same ADC channel.
4. The ADC resolution of EG915N-LA and EG915N-EA is small. See ***document [7]*** for details when designing ADC interface circuit.

4.8. USB_BOOT

The module provides a USB_BOOT. You can pull up USB_BOOT to 1.8 V or short-circuit VDD_EXT and USB_BOOT before the module is powered on and the module will enter download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 23: Pin Definition of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module into emergency download mode	1.8 V power domain. Active high. A test point is recommended to be reserved.

The following figure shows a reference circuit and timing sequence for entering emergency download mode of USB_BOOT.

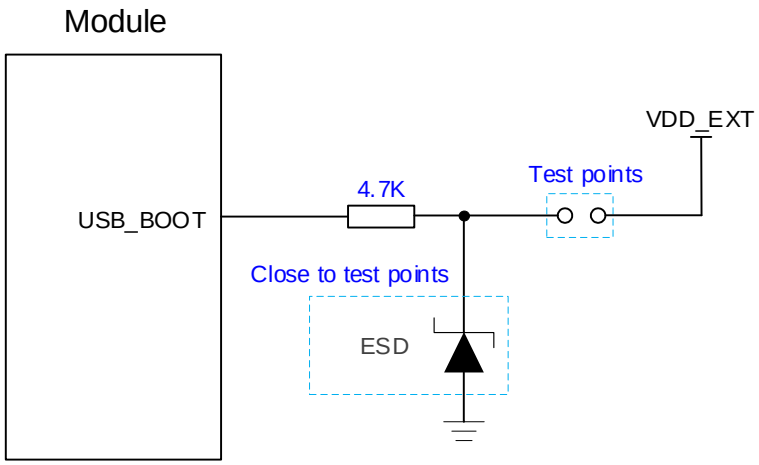


Figure 28: Reference Circuit of USB_BOOT Interface

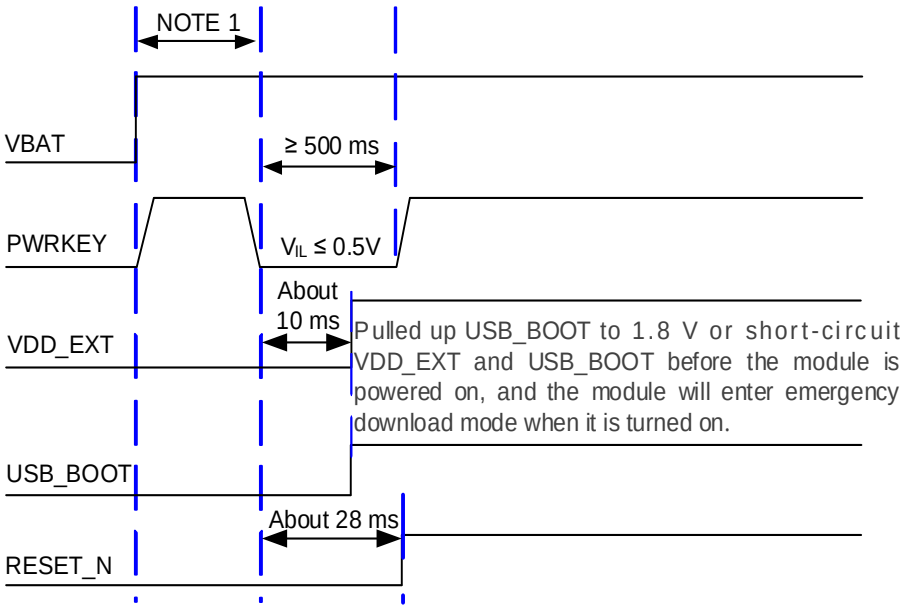


Figure 29: Timing Sequence for Entering Emergency Download Mode

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY pin. The time period between powering up VBAT and pulling down PWRKEY pin should be at least 30 ms.
2. When using MCU to control module to enter the emergency download mode, follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Directly connect the test points as shown in ***Figure 28*** can manually force the module to enter download mode.

4.9. Camera Interface

The module provides one camera interface, supports up to 0.3 MP and supports single data trace or dual data trace transmission of SPI.

Table 24: Pin Definition of Camera Interface

Pin Name	Pin No.	I/O	Description	Comment
CAM_MCLK	95	DO	Master clock of camera	1.8 V power domain. If unused, keep it open.
CAM_I2C_SCL	103	OD	I2C clock of camera	Pull each of them up to 1.8 V

CAM_I2C_SDA	114	OD	I2C data of camera	power domain with an external resistor. If unused, keep them open.
CAM_SPI_CLK	78	DI	SPI clock of camera	1.8 V power domain. If unused, keep them open.
CAM_SPI_DATA0	97	DI	SPI data 0 of camera	
CAM_SPI_DATA1	98	DI	SPI data 1 of camera	
CAM_PWDN	115	DO	Power down of camera	
CAM_VDD	94	PO	Analog power supply of camera	Power supply of camera. If unused, keep them open.
CAM_VDDIO	93	PO	Digital power supply of camera	

4.10. LCM Interface

The module provides one LCM interface and supports an LCD display module with a maximum resolution of 240 × 320. The module supports SPI four-wire single data trace transmission, and supports RGB565 format output.

Table 25: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_TE	92	DI	LCD tearing effect	1.8 V power domain. If unused, keep them open.
LCD_RST	107	DO	LCD reset	
LCD_SPI_CS	16	DO	LCD chip select	
LCD_SPI_CLK	105	DO	LCD clock	
LCD_SPI_RS	106	DO	LCD register select	
LCD_SPI_DOUT	116	DO	LCD data output	

4.11. Matrix Keypad Interfaces

The module supports 4 × 4 matrix keypad interfaces.

Table 26: Pin Definition of Matrix Keypad Interfaces

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
USIM2_DET*	83	KP_MKIN[0]	DI	matrix keypad input 0	1.8 V power domain. If unused, keep them open.
MAIN_RI*	39	KP_MKOUT[0]	DO	matrix keypad output 0	
AUX_RXD	28	KP_MKIN[2]	DI	matrix keypad input 2	
AUX_TXD	27	KP_MKOUT[2]	DO	matrix keypad output 2	
AUX_RTS	25	KP_MKIN[3]	DI	matrix keypad input 3	
AUX_CTS	26	KP_MKOUT[3]	DO	matrix keypad output 3	
SLEEP_IND	1	KP_MKIN[4]	DI	matrix keypad input 4	
STATUS	20	KP_MKOUT[1]	DO	matrix keypad output 1	

NOTE

For more information about multiplexing, see ***document [1]***.

4.12. GPIOs

The module provides two general GPIOs, which can be configured as general GPIO or other functions. For details, see ***document [1]***.

Table 27: Pin Definition of general GPIOs

Pin Name	Pin No.	I/O	Description	Comment
GPIO1	64	DIO	General-purpose input/output	1.8 V power domain. If unused, keep them open.
GPIO2	104	DIO		

4.13. Indication Signal

Relative interfaces' pin definitions are here as follows:

Table 28: Pin Definition of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	21	DO	Indicates the module's network activity status	1.8 V power domain. If unused, keep them open.
STATUS	20	DO	Indicate the module's operation status	

4.13.1. Network Status Indication

The network indication pins can drive the network status indicators. The module provides one network indication pin: NET_STATUS. The following tables describe pin definition and logic level changes in different network status.

Table 29: Working State of Network Activity Indication

Pin Name	Logic Level Changes	Network Status
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker slowly (1800 ms high/200 ms low)	Idle
	Flicker quickly (125 ms high/125 ms low)	Data transmission is ongoing
	Always High (Always ON)	Voice calling

A reference circuit is shown in the following figure.

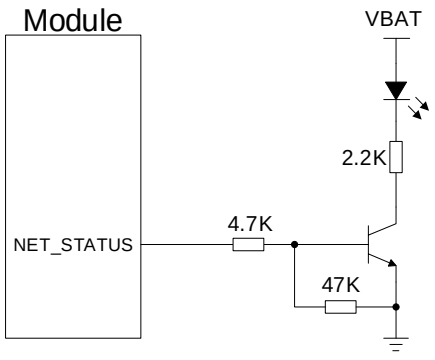


Figure 30: Reference Circuit of Network Status Indication

4.13.2. STATUS

The STATUS pin indicates the module's operation status. When the module is turned on normally, the STATUS will output high level.

The following figure shows a reference circuit of STATUS.

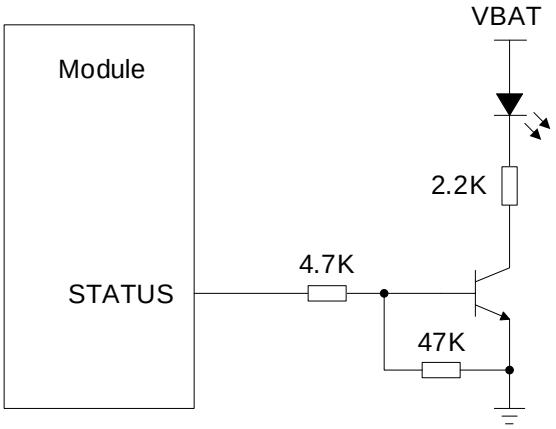


Figure 31: Reference Circuits of STATUS

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module includes one main antenna interface. The module with built-in GNSS function also has one GNSS antenna interface. The impedance of antenna interface is 50 Ω.

5.1. Cellular Network

5.1.1. Main Antenna Interface & Frequency Bands

Table 30: Pin Definition of Cellular Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω characteristic impedance.

Table 31: EG915N-EU Operating Frequency

Operating Frequency	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B20	832–862	791–821	MHz

Table 32: EG915N-LA Operating Frequency

Operating Frequency	Transmit	Receive	Unit
GSM850	824–849	869-894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-FDD B66	1710–1780	2110–2180	MHz

Table 33: EG915N-EA Operating Frequency

Operating Frequency	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B28	703–748	758–803	MHz

5.1.2. Antenna Tuner Control Interfaces*

The module can use GRFC (generic RF control) interfaces to control external antenna tuner.

Table 34: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC_1	76	DO	Generic RF Controller	If unused, keep them open.
GRFC_2	77	DO		

Table 35: EG915N-EU Truth Table of GRFC Interface (Unit: MHz)

GRFC_1 Level	GRFC_2 Level	Frequency Range	Bands
Low	Low	-	-
Low	High	832–862	LTE B20
High	Low	880–915	LTE B8, EGSM900
High	High	1920–1980 1710–1785 2500–2570	LTE B1/B3/B7 DCS1800

Table 36: EG915N-LA Truth Table of GRFC Interface (Unit: MHz)

GRFC_1 Level	GRFC_2 Level	Frequency Range	Bands
Low	Low	703–748	LTE B28
Low	High	824–849	LTE B5, GSM850
High	Low	880–915	LTE B8, EGSM900
High	High	1850–1910 1710–1785 1710–1755 2500–2570	LTE B2/B3/B4/B7/B66 DCS1800, PCS1900

Table 37: EG915N-EA Truth Table of GRFC Interface (Unit: MHz)

GRFC_1 Level	GRFC_2 Level	Frequency Range	Bands
Low	Low	703–748	LTE B28
Low	High	832–862	LTE B20
High	Low	880–915	LTE B8, EGSM900
High	High	1920–1980 1710–1785 2500–2570	LTE B1/B3/B7 DCS1800

5.1.3. Transmitting Power

The following table shows the RF output power of the module.

Table 38: EG915N-EU RF Transmitting Power

Frequency Bands	Max.	Min.
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B7/B8/B20	23 dBm ±2 dB	< -39 dBm

Table 39: EG915N-LA RF Transmitting Power

Frequency Bands	Max.	Min.
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1800	30 dBm ±2 dB	0 dBm ±5 dB
GSM850 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB

EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
PCS1900 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
LTE-FDD B2/B3/B4/B5/B7/B8/B28/B66	23 dBm ±2 dB	< -39 dBm

Table 40: EG915N-EA RF Transmitting Power

Frequency Bands	Max.	Min.
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots Tx mode, the maximum output power is reduced by 4 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

5.1.4. Receiver Sensitivity

The following table shows conducted RF receiver sensitivity of the module.

Table 41: EG915N-EU Conducted RF Receiver Sensitivity

Frequency Bands	Receiver Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
EGSM900	-109 dBm	-	-	-102 dBm
DCS1800	-104 dBm	-	-	-102 dBm
LTE-FDD B1 (10 MHz)	-98 dBm	-	-	-96.3 dBm

LTE-FDD B3 (10 MHz)	-98 dBm	-	-	-93.3 dBm
LTE-FDD B7 (10 MHz)	-97 dBm	-	-	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98 dBm	-	-	-93.3 dBm
LTE-FDD B20 (10 MHz)	-96 dBm	-	-	-93.3 dBm

Table 42: EG915N-LA Conducted RF Receiver Sensitivity

Frequency Bands	Receiver Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
GSM850	-108 dBm	-	-	-102 dBm
EGSM900	-107 dBm	-	-	-102 dBm
DCS1800	-104 dBm	-	-	-102 dBm
PCS1900	-104 dBm	-	-	-102 dBm
LTE-FDD B2 (10 MHz)	-99 dBm	-	-	-94.3 dBm
LTE-FDD B3 (10 MHz)	-98 dBm	-	-	-93.3 dBm
LTE-FDD B4 (10 MHz)	-98.5 dBm	-	-	-9.3 dBm
LTE-FDD B5 (10 MHz)	-99.5 dBm	-	-	-94.3 dBm
LTE-FDD B7 (10 MHz)	-97 dBm	-	-	-94.3 dBm
LTE-FDD B8 (10 MHz)	-99 dBm	-	-	-93.3 dBm
LTE-FDD B28 (10 MHz)	-99 dBm	-	-	-94.8 dBm
LTE-FDD B66 (10 MHz)	-99 dBm	-	-	-96.5 dBm

Table 43: EG915N-EA Conducted RF Receiver Sensitivity

Frequency Bands	Receiver Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
EGSM900	-108 dBm	-	-	-102 dBm
DCS1800	-106 dBm	-	-	-102 dBm
LTE-FDD B1 (10 MHz)	-99 dBm	-	-	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98 dBm	-	-	-93.3 dBm
LTE-FDD B7 (10 MHz)	-97 dBm	-	-	-94.3 dBm
LTE-FDD B8 (10 MHz)	-100 dBm	-	-	-93.3 dBm
LTE-FDD B20 (10 MHz)	-100.8 dBm	-	-	-93.3 dBm
LTE-FDD B28 (10 MHz)	-99 dBm	-	-	-94.8 dBm

5.1.5. Reference Design

Use a π-type matching circuit for all the antenna interfaces for better cellular performance. Capacitors are not mounted by default.

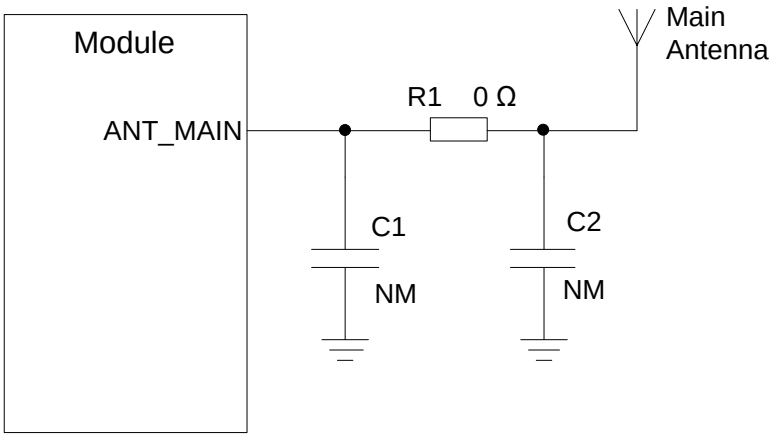


Figure 32: Reference Circuit of RF Antenna Interface

NOTE

Place the π-type matching components (R1, C1 and C2) as close to the antenna as possible.

5.2. GNSS (Optional)

GNSS function is optional for the module. Only the module with built-in GNSS function integrates a multi-constellation GNSS receiver.

For EG915N series, the built-in GNSS parameters are as follows:

- Supports GPS, GLONASS, Galileo, BDS, QZSS positioning system.
- Supports NMEA 0183 protocol and outputs NMEA message via USB interface by default (update rate for positioning: 1 Hz).
- The module's GNSS function is disabled off by default. It must be enabled via *ql_gnss_open()*. See ***document [8]*** for more details about the API.

5.2.1. GNSS Antenna Interface & Frequency Bands

The following table lists the pin definition and frequency characteristics of the GNSS antenna interface.

Table 44: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω characteristic impedance. If unused, keep it open.

Table 45: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023 (L1)	MHz
GLONASS	1597.5–1605.8 (L1)	MHz
Galileo	1575.42 ±2.046 (E1)	MHz
BDS	1561.098 ±2.046 (B1I)	MHz
QZSS	1575.42 ±1.023 (L1)	MHz

5.2.2. GNSS Performance

Table 46: EG915N Series GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity	Acquisition	-145	dBm
	Reacquisition	-159	dBm
	Tracking	-159	dBm
TTFF	Cold start @ open sky	27.98	s
	Warm start @ open sky	27.52	s
	Hot start @ open sky	0.12	s
Horizontal accuracy	CEP-50	1.14	m

NOTE

1. For more information about GNSS performance, contact Quectel Technical Support.
2. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
3. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
4. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. GNSS Antenna Reference Design

5.2.3.1. GNSS Active Antenna

GNSS active antenna connection reference circuit is shown in the figure below.

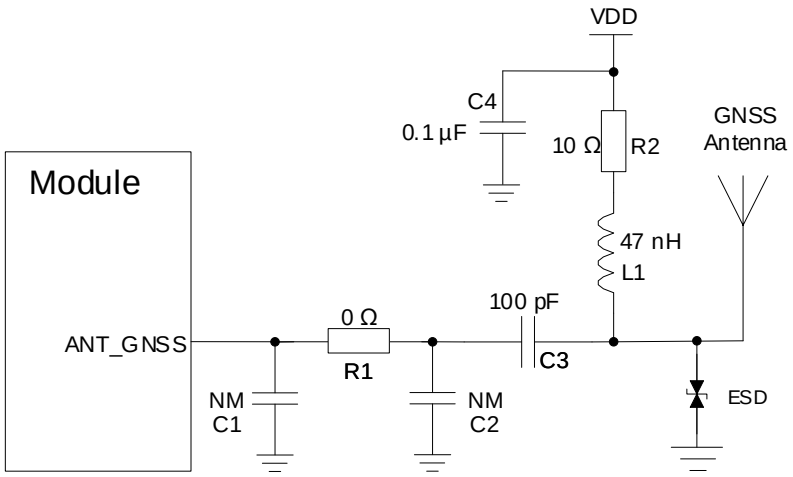


Figure 33: GNSS Active Antenna Reference Circuit

The power supply voltage range of the external active antenna is 2.8–4.3 V, and the typical value is 3.3 V.

5.2.3.2. GNSS Passive Antenna

GNSS passive antenna connection reference circuit is shown in the figure below.

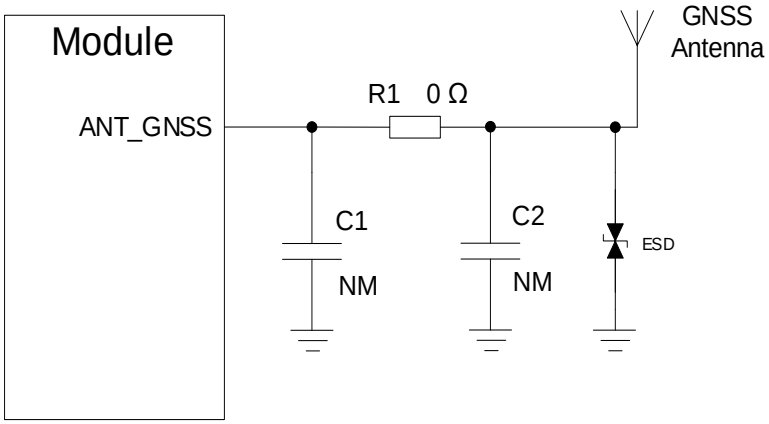


Figure 34: GNSS Passive Antenna Reference Circuit

C1, R1 and C2 form the matching circuit, which is recommended to be reserved for adjusting the antenna impedance. Among them, C1 and C2 are not mounted by default, and R1 is only mounted by a 0 Ω resistor. The impedance of the RF trace should be controlled at about 50 Ω, and the trace should be as short as possible.

NOTE

1. If the module is designed with a passive antenna, then the VDD circuit is not needed.
2. You can select an external LDO for power supply according to the active antenna requirements.
3. The junction capacitance of the antenna interface ESD protection component device is recommended to be less than 0.05 pF.

5.2.4. GNSS Antenna Routing Guidelines

In your application design, the following design principles should be followed:

- The distance between the GNSS antenna and the main antenna should be as large as possible.
- Digital signals such as (U)SIM card, USB interface, camera module, SD card and display interface. should be far away from the antenna.
- Sensitive analog signals should be far away from GNSS signal paths, and ground holes should be added for isolation and protection.
- ANT_GNSS trace maintains 50 Ω characteristic impedance.

For the reference design of GNSS antenna interface and antenna precautions, see ***Chapter 5.2.3.***

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

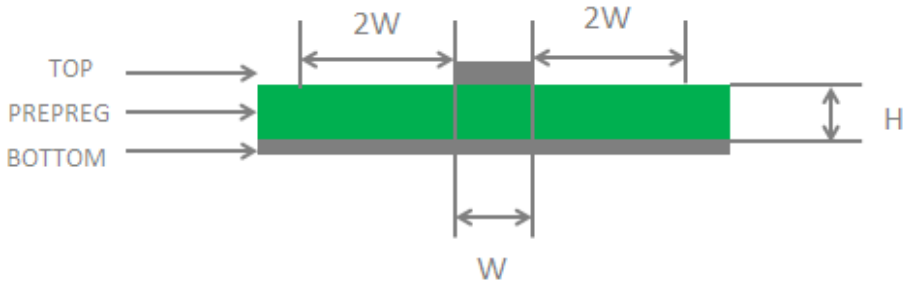


Figure 35: Microstrip Design on a 2-layer PCB

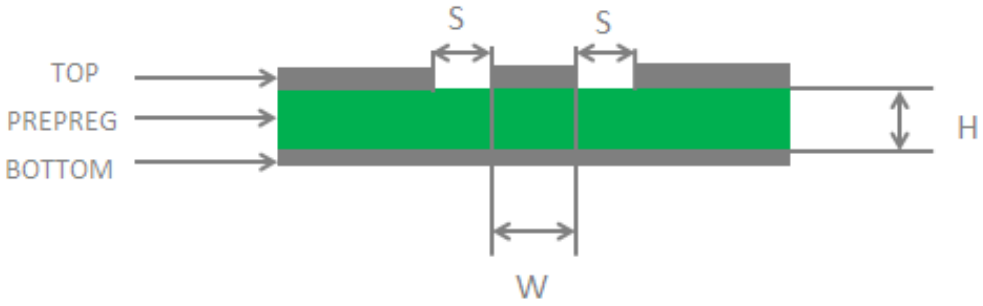


Figure 36: Coplanar Waveguide Design on a 2-layer PCB

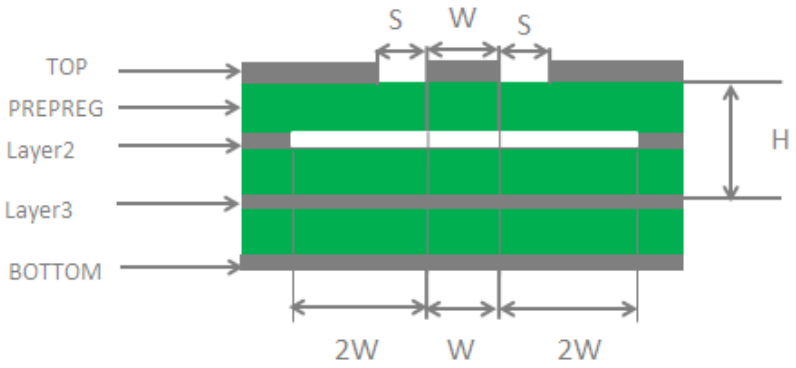


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

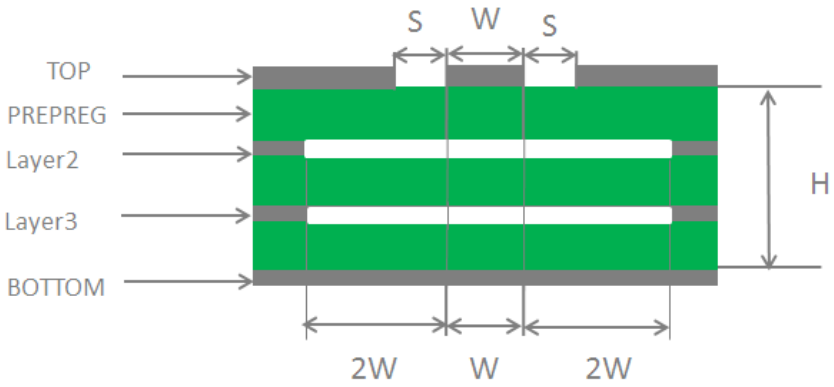


Figure 38: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [9]***.

5.4. Requirements for Antenna Design

Table 47: Antenna Requirements

Type	Requirements
Cellular	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Max input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)
GNSS	● Frequency range: L1: 1559–1609 MHz ● RHCP or linear polarization ● VSWR: ≤ 2 ● Active antenna noise factor: < 1.5 dB ● Active antenna gain: > -2 dBi ● Active antenna internal LNA gain: < 17 dB

5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

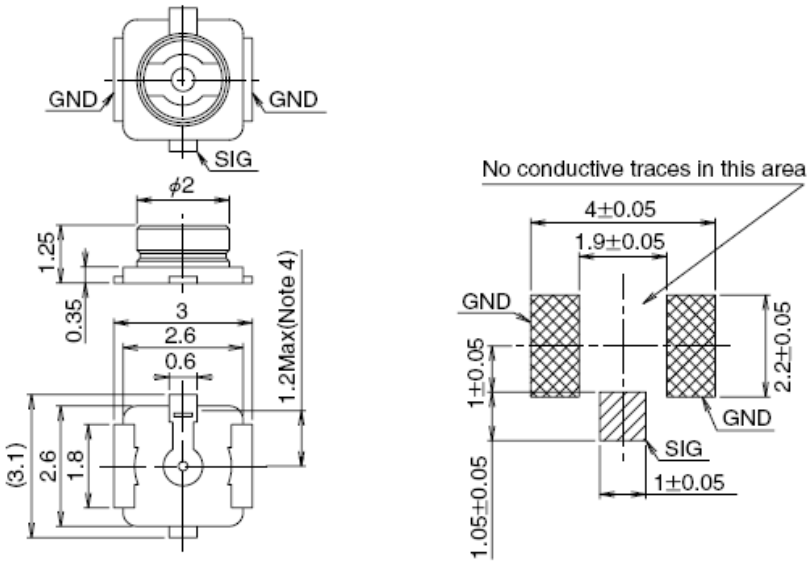


Figure 39: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plug listed in the following figure can be used to match the U.FL-R-SMT.

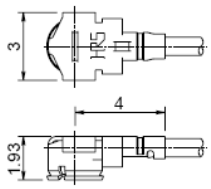
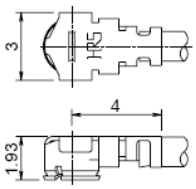
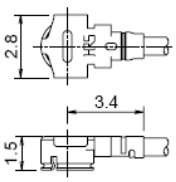
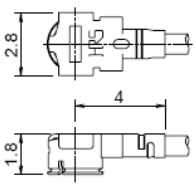
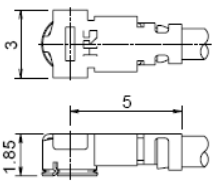
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 40: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of mated connector.

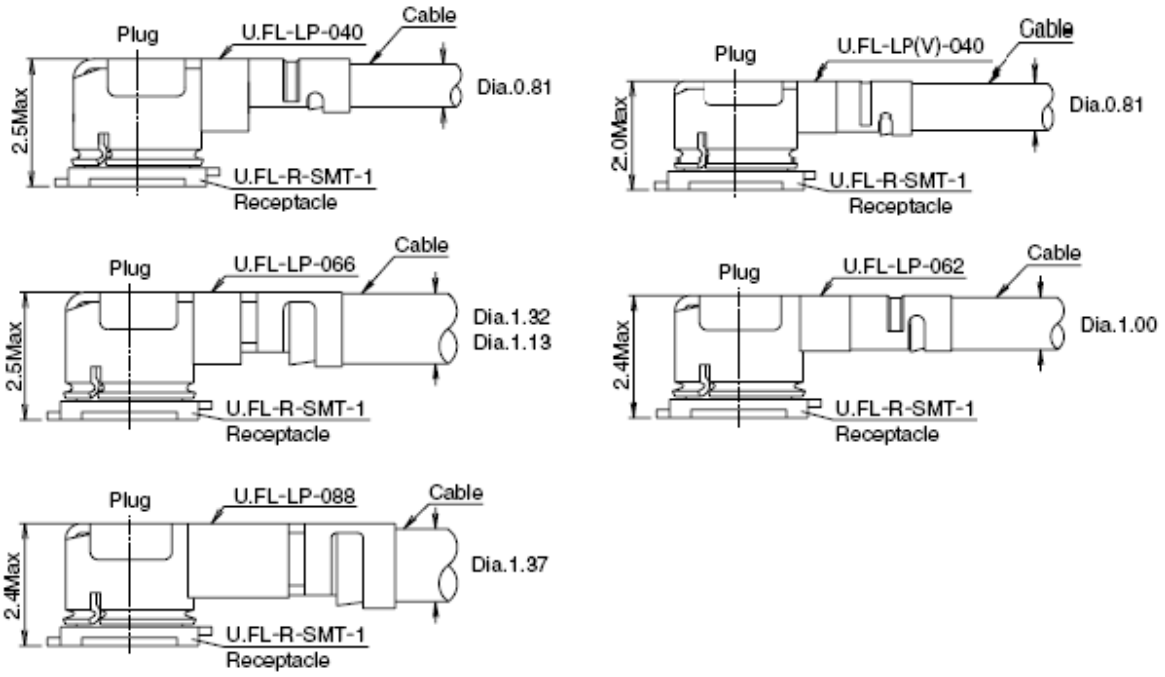


Figure 41: Space Factor of the Mated Connectors (Unit: mm)

For more details, please visit http://hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 48: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_BB/VBAT_RF	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	2.2	A
Voltage at Digital Pins	-0.3	2.3	V

6.2. Power Supply Ratings

Table 49: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.4	3.8	4.5	V
	Voltage drop during burst transmission	Maximum power control level	-	-	400	mV
I_{VBAT}	Peak supply current	Maximum power control	-	2.0	2.5	A

	level				
USB_VBUS	USB connection detect	3.0	5.0	5.25	V

6.3. Power Consumption

The current consumption of the module is shown in the table below.

Table 50: EG915N-EU Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	26.64	μA
Sleep state	Minimum functionality mode (USB disconnected)	0.87	mA
	EGSM900 @ DRX = 2 (USB disconnected)	1.82	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.32	mA
	EGSM900 @ DRX = 5 (USB suspend)	1.47	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.16	mA
	DCS1800 @ DRX = 2 (USB disconnected)	1.92	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.36	mA
	DCS1800 @ DRX = 5 (USB suspend)	1.53	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.19	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.89	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.44	mA
	LTE-FDD @ PF = 64 (USB suspend)	1.62	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.24	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.13	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	19.34	mA

	EGSM900 @ DRX = 5 (USB connected)	29.04	mA
	DCS1800 @ DRX = 5 (USB disconnected)	19.36	mA
	DCS1800 @ DRX = 5 (USB connected)	29.02	mA
	LTE-FDD @ PF = 64 (USB disconnected)	19.70	mA
	LTE-FDD @ PF = 64 (USB connected)	29.60	mA
GPRS data transmission	EGSM900 4DL/1UL @ 32.88 dBm	235.41	mA
	EGSM900 3DL/2UL @ 32.79 dBm	412.87	mA
	EGSM900 2DL/3UL @ 31.52 dBm	511.46	mA
	EGSM900 1DL/4UL @ 29.17 dBm	529.85	mA
	DCS1800 4DL/1UL @ 29.31 dBm	159.05	mA
	DCS1800 3DL/2UL @ 29.24dBm	263.67	mA
	DCS1800 2DL/3UL @ 27.77 dBm	317.38	mA
	DCS1800 1DL/4UL @ 25.98 dBm	345.74	mA
EDGE data transmission	EGSM900 4DL/1UL @ 26.39 dBm	144.67	mA
	EGSM900 3DL/2UL @ 25.9 dBm	229.64	mA
	EGSM900 2DL/3UL @ 25.15 dBm	287.01	mA
	EGSM900 1DL/4UL @ 22.14 dBm	310.43	mA
	DCS1800 4DL/1UL @ 25.01 dBm	128.51	mA
	DCS1800 3DL/2UL @ 25.09 dBm	200.49	mA
	DCS1800 2DL/3UL @ 23.31 dBm	256.65	mA
	DCS1800 1DL/4UL @ 21.27 dBm	298.11	mA
LTE data transmission	LTE-FDD B1	594.00	mA
	LTE-FDD B3	607.00	mA
	LTE-FDD B7	658.00	mA
	LTE-FDD B8	618.00	mA

	LTE-FDD B20	523.00	mA
GSM voice call	EGSM900 PCL = 5 @ 32.53 dBm	225.96	mA
	EGSM900 PCL = 12 @ 19.77 dBm	87.22	mA
	EGSM900 PCL = 19 @ 5.37 dBm	54.57	mA
	DCS1800 PCL = 0 @ 29.25 dBm	151.06	mA
	DCS1800 PCL = 7 @ 16.43 dBm	71.09	mA
	DCS1800 PCL = 15 @ 0.28 dBm	50.98	mA

Table 51: EG915N-LA Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	24.96	μA
Sleep state	Minimum functionality mode (USB disconnected)	0.90	mA
	EGSM900 @ DRX = 2 (USB disconnected)	1.94	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.49	mA
	EGSM900 @ DRX = 5 (USB suspend)	1.65	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.37	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.00	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.53	mA
	DCS1800 @ DRX = 5 (USB suspend)	1.69	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.38	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.87	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.47	mA
	LTE-FDD @ PF = 64 (USB suspend)	1.62	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.23	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.11	mA

Idle state	EGSM900 @ DRX = 5 (USB disconnected)	16.40	mA
	EGSM900 @ DRX = 5 (USB connected)	29.17	mA
	DCS1800 @ DRX = 5 (USB disconnected)	16.44	mA
	DCS1800 @ DRX = 5 (USB connected)	29.15	mA
	LTE-FDD @ PF = 64 (USB disconnected)	16.21	mA
	LTE-FDD @ PF = 64 (USB connected)	28.89	mA
GPRS data transmission	GSM850 4DL/1UL @ 32.66 dBm	224.00	mA
	GSM850 3DL/2UL @ 32.54 dBm	403.00	mA
	GSM850 2DL/3UL @ 31.12 dBm	502.00	mA
	GSM850 1DL/4UL @ 28.95 dBm	530.00	mA
	EGSM900 4DL/1UL @ 32.46 dBm	225.00	mA
	EGSM900 3DL/2UL @ 32.37 dBm	406.00	mA
	EGSM900 2DL/3UL @ 31.03 dBm	511.00	mA
	EGSM900 1DL/4UL @ 28.85 dBm	547.00	mA
	DCS1800 4DL/1UL @ 29.66 dBm	162.00	mA
	DCS1800 3DL/2UL @ 29.59 dBm	282.00	mA
	DCS1800 2DL/3UL @ 27.98 dBm	344.00	mA
	DCS1800 1DL/4UL @ 25.88 dBm	379.00	mA
	PCS1900 4DL/1UL @ 29.73 dBm	153.00	mA
	PCS1900 3DL/2UL @ 29.68 dBm	265.00	mA
	PCS1900 2DL/3UL @ 28.26 dBm	331.00	mA
	PCS1900 1DL/4UL @ 26.36 dBm	362.00	mA
EDGE data transmission	GSM850 4DL/1UL @ 25.85 dBm	135.00	mA
	GSM850 3DL/2UL @ 25.8 dBm	235.00	mA
	GSM850 2DL/3UL @ 24.12 dBm	281.00	mA

	GSM850 1DL/4UL @ 22.76 dBm	324.00	mA
	EGSM900 4DL/1UL @ 26.56 dBm	135.00	mA
	EGSM900 3DL/2UL @ 26.37 dBm	236.00	mA
	EGSM900 2DL/3UL @ 24.63 dBm	293.00	mA
	EGSM900 1DL/4UL @ 23.51 dBm	338.00	mA
	DCS1800 4DL/1UL @ 25.50 dBm	123.00	mA
	DCS1800 3DL/2UL @ 25.66 dBm	218.00	mA
	DCS1800 2DL/3UL @ 24.47 dBm	282.00	mA
	DCS1800 1DL/4UL @ 22.13 dBm	328.00	mA
	PCS1900 4DL/1UL @ 27.41 dBm	133.00	mA
	PCS1900 3DL/2UL @ 27.25 dBm	235.00	mA
	PCS1900 2DL/3UL @ 24.11 dBm	278.00	mA
	PCS1900 1DL/4UL @ 21.61 dBm	314.00	mA
LTE data transmission	LTE-FDD B2	659.00	mA
	LTE-FDD B3	697.00	mA
	LTE-FDD B4	669.00	mA
	LTE-FDD B5	590.00	mA
	LTE-FDD B7	709.00	mA
	LTE-FDD B8	610.00	mA
	LTE-FDD B28	615.00	mA
	LTE-FDD B66	573.00	mA
GSM voice call	GSM850 PCL = 5 @ 32.66 dBm	234.00	mA
	GSM850 PCL = 12 @ 19.48 dBm	95.00	mA
	GSM850 PCL = 19 @ 5.10 dBm	63.00	mA
	EGSM900 PCL = 5 @ 32.61 dBm	242.00	mA

	EGSM900 PCL = 12 @ 19.30 dBm	93.00	mA
	EGSM900 PCL = 19 @ 4.13 dBm	61.00	mA
	DCS1800 PCL = 0 @ 29.43 dBm	159.00	mA
	DCS1800 PCL = 7 @ 16.72 dBm	80.00	mA
	DCS1800 PCL = 15 @ -0.02 dBm	58.00	mA
	PCS1900 PCL = 0 @ 29.63 dBm	159.00	mA
	PCS1900 PCL = 7 @ 16.74 dBm	78.00	mA
	PCS1900 PCL = 15 @0.96 dBm	59.00	mA

Table 52: EG915N-EA Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	23.65	μA
Sleep state	Minimum functionality mode (USB disconnected)	0.92	mA
	EGSM900 @ DRX = 2 (USB disconnected)	1.92	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.46	mA
	EGSM900 @ DRX = 5 (USB suspend)	1.66	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.35	mA
	DCS1800 @ DRX = 2 (USB disconnected)	1.96	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.50	mA
	DCS1800 @ DRX = 5 (USB suspend)	1.64	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.35	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.88	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.44	mA
	LTE-FDD @ PF = 64 (USB suspend)	1.60	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.22	mA

	LTE-FDD @ PF = 256 (USB disconnected)	1.10	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	16.69	mA
	EGSM900 @ DRX = 5 (USB connected)	29.61	mA
	DCS1800 @ DRX = 5 (USB disconnected)	16.73	mA
	DCS1800 @ DRX = 5 (USB connected)	29.59	mA
	LTE-FDD @ PF = 64 (USB disconnected)	16.52	mA
	LTE-FDD @ PF = 64 (USB connected)	29.39	mA
GPRS data transmission	EGSM900 4DL/1UL @ 32.99 dBm	232.00	mA
	EGSM900 3DL/2UL @ 32.45 dBm	411.00	mA
	EGSM900 2DL/3UL @ 30.79 dBm	513.00	mA
	EGSM900 1DL/4UL @ 28.64 dBm	557.00	mA
	DCS1800 4DL/1UL @ 28.75 dBm	170.00	mA
	DCS1800 3DL/2UL @ 29.29 dBm	290.00	mA
	DCS1800 2DL/3UL @ 27.66 dBm	349.00	mA
	DCS1800 1DL/4UL @ 24.73 dBm	376.00	mA
EDGE data transmission	EGSM900 4DL/1UL @ 25.88 dBm	127	mA
	EGSM900 3DL/2UL @ 25.62 dBm	216	mA
	EGSM900 2DL/3UL @ 24.25 dBm	276	mA
	EGSM900 1DL/4UL @ 22.92 dBm	319	mA
	DCS1800 4DL/1UL @ 25.27 dBm	121	mA
	DCS1800 3DL/2UL @ 25.11 dBm	207	mA
	DCS1800 2DL/3UL @ 23.50 dBm	266	mA
	DCS1800 1DL/4UL @ 22.33 dBm	319	mA
LTE data transmission	LTE-FDD B1	682.00	mA
	LTE-FDD B3	743.00	mA

	LTE-FDD B7	737.00	mA
	LTE-FDD B8	611.00	mA
	LTE-FDD B20	555.00	mA
	LTE-FDD B28	534.00	mA
GSM voice call	EGSM900 PCL = 5 @ 32.53 dBm	244.00	mA
	EGSM900 PCL = 12 @ 19.40 dBm	101.00	mA
	EGSM900 PCL = 19 @ 4.05 dBm	68.00	mA
	DCS1800 PCL = 0 @ 29.16 dBm	180.00	mA
	DCS1800 PCL = 7 @ 16.27 dBm	88.00	mA
	DCS1800 PCL = 15 @ -0.72 dBm	66.00	mA

NOTE

For more information about power consumption, contact Quectel Technical Support for the power consumption test report of the module.

6.4. Digital I/O Characteristics

Table 53: 1.8 V Digital I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	0.7 × VDDIO	VDDIO + 0.2	V
V_{IL}	Input low voltage	-0.3	0.3 × VDDIO	V
V_{OH}	Output high voltage	VDDIO – 0.2	-	V
V_{OL}	Output low voltage	-	0.2	V

Table 54: (U)SIM Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.62	1.98	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{IL}	Input low voltage	0	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.15 × USIM_VDD	V

Table 55: (U)SIM High-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.3	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{IL}	Input low voltage	0	0.15 × USIM_VDD	V
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.15 × USIM_VDD	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the module electrostatics discharge characteristics.

Table 56: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 57: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [4]	-35	+25	+75	ºC
Extended Operation Range [5]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

[4] Within operating temperature range, the module is 3GPP compliant.
[5] Within extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

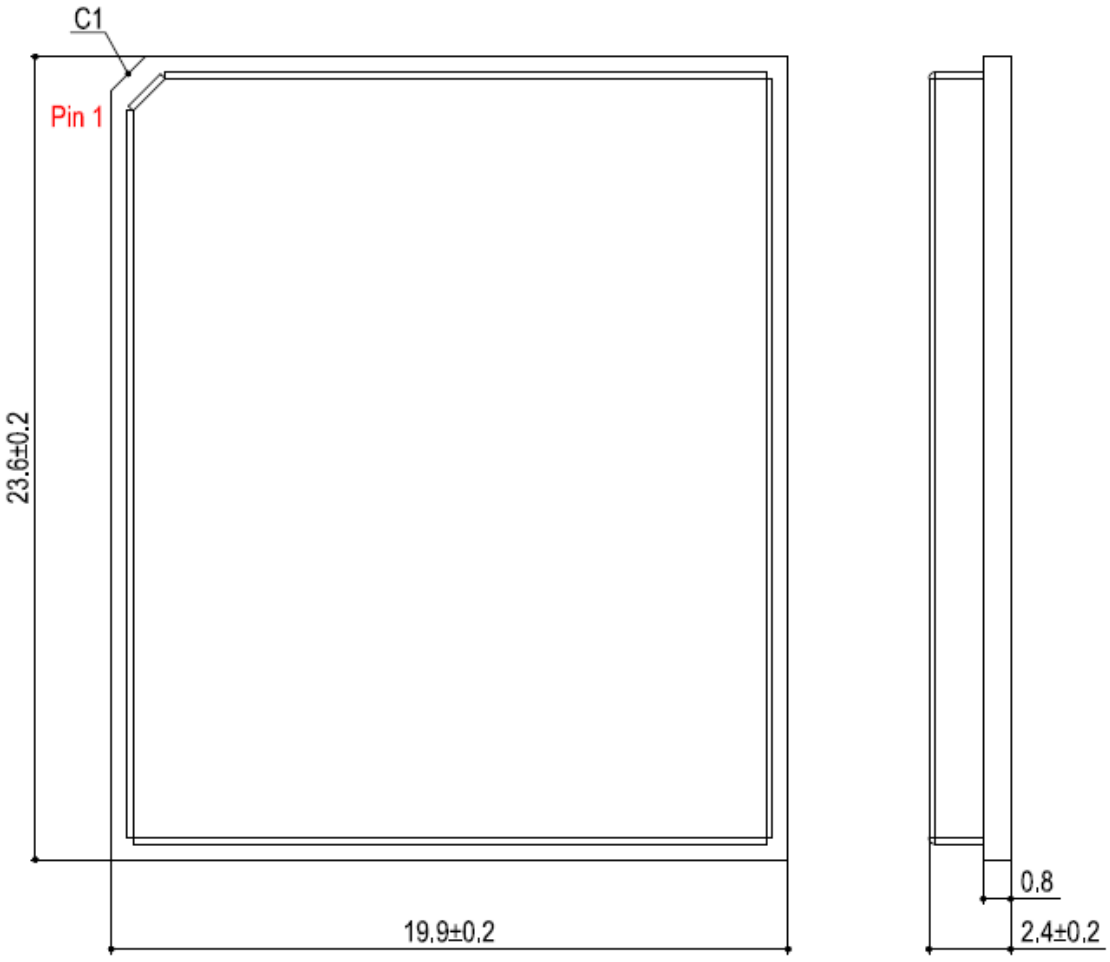


Figure 42: Module Top and Side Dimensions

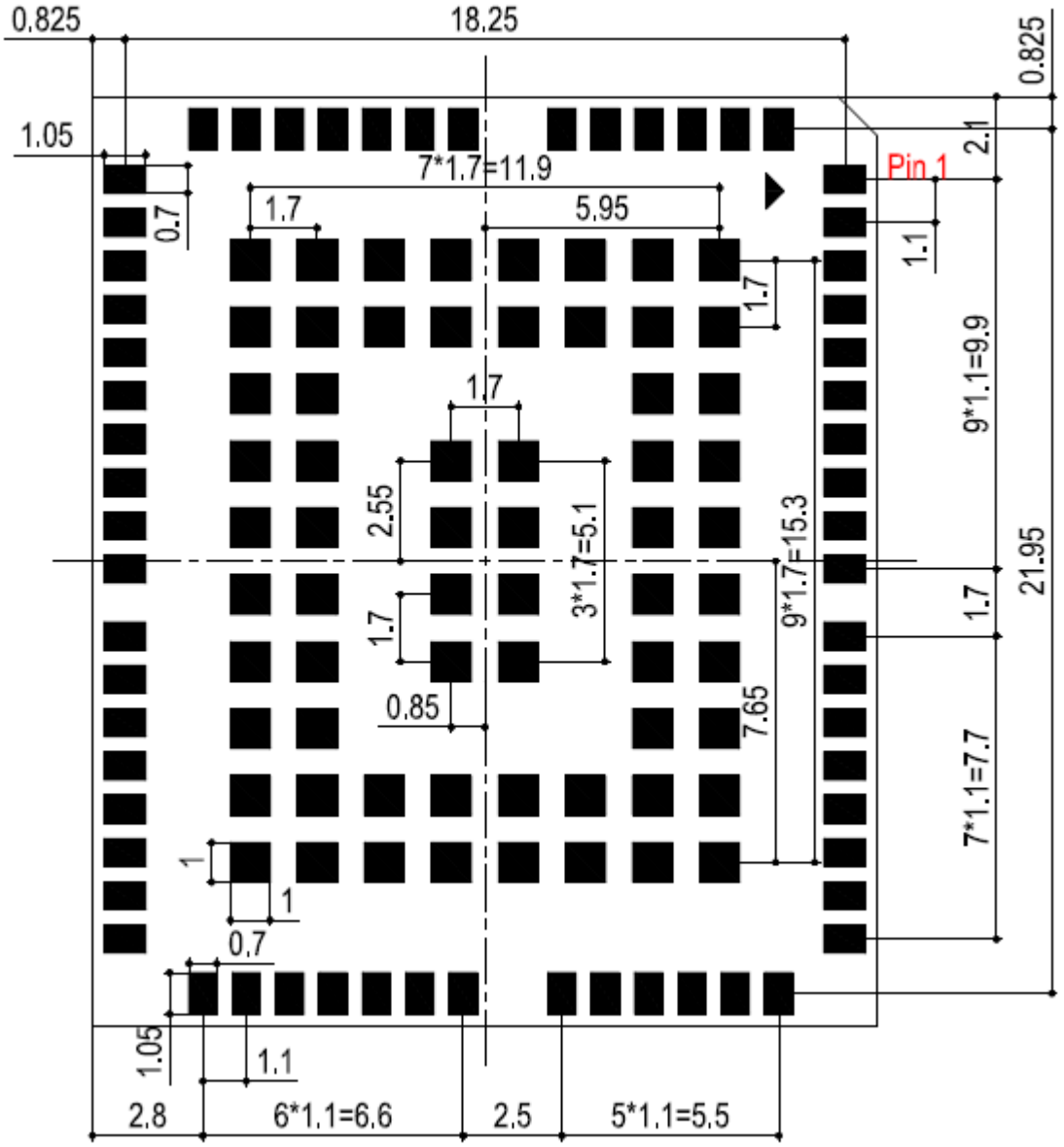


Figure 43: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

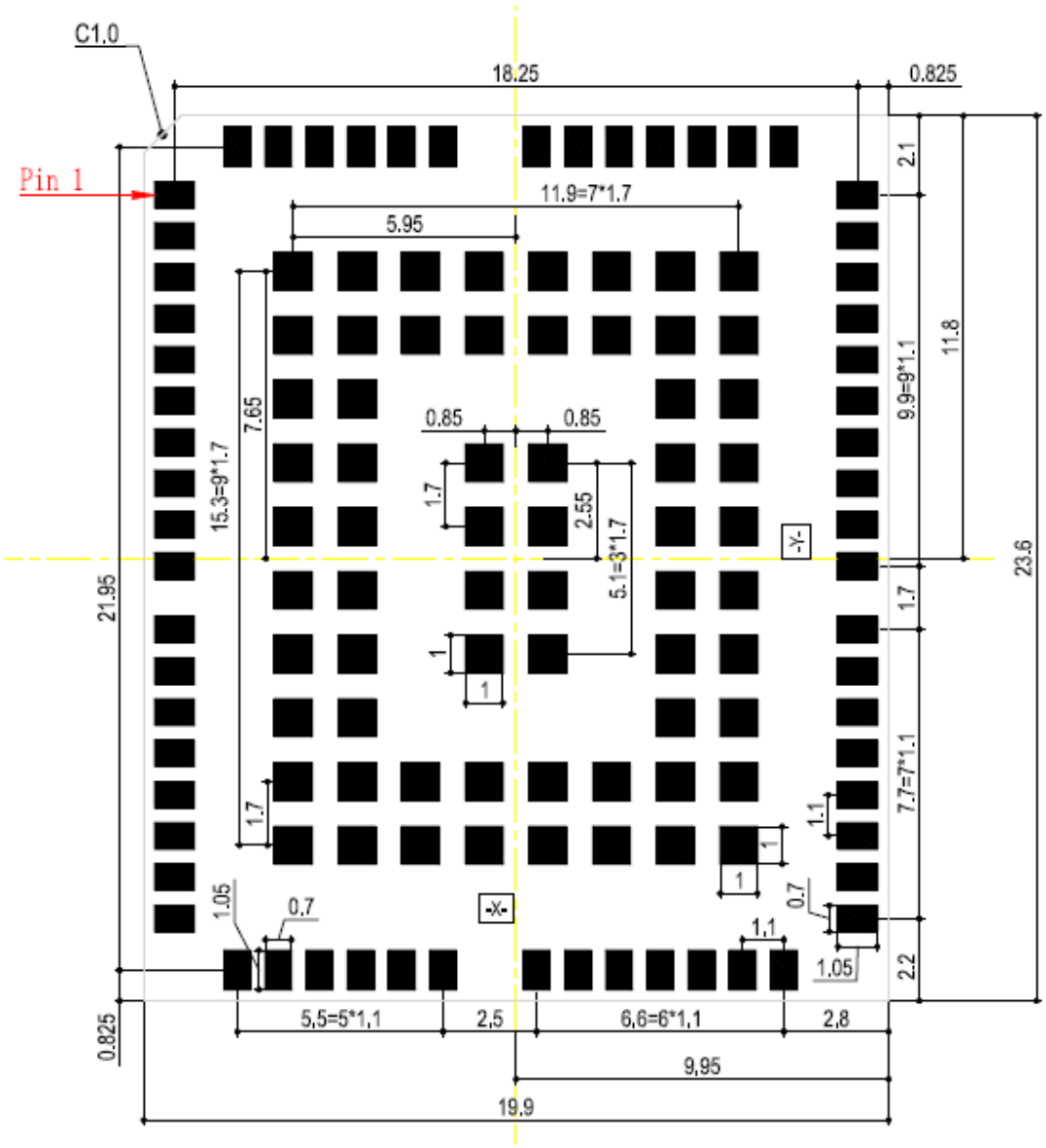


Figure 44: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

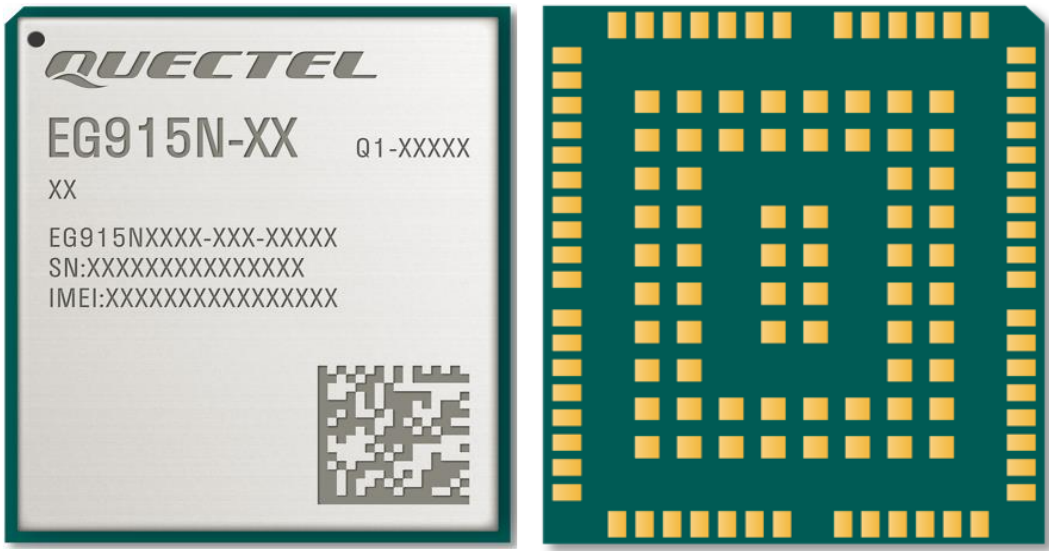


Figure 45: Top and Bottom Views of the module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [6] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[6] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [10]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

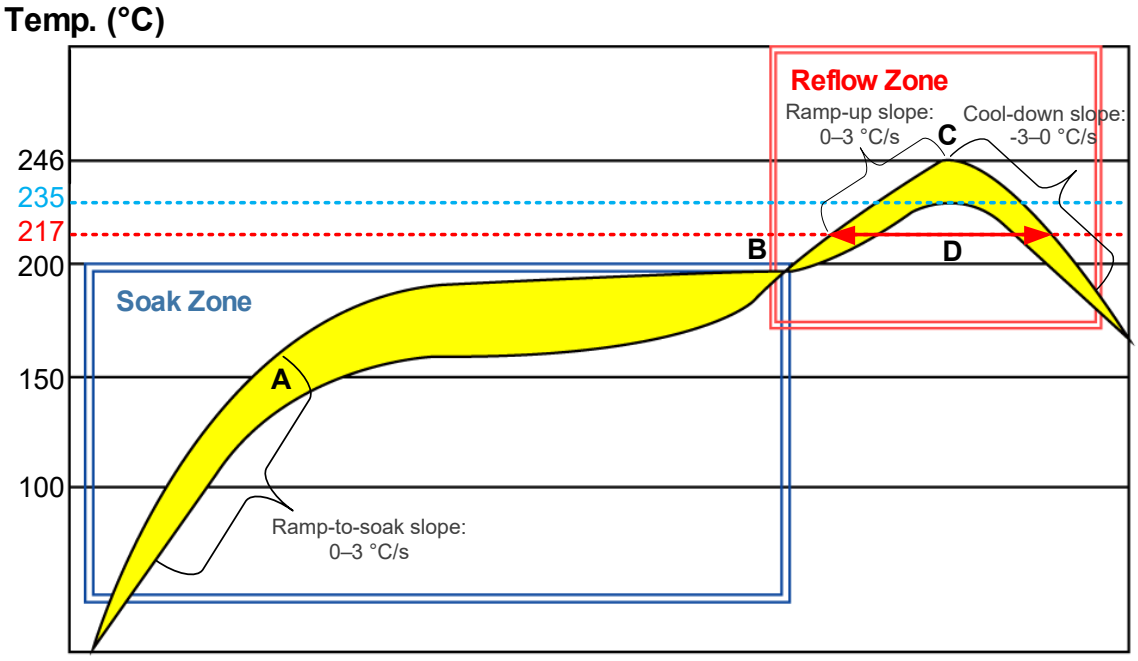


Figure 46: Recommended Reflow Soldering Thermal Profile

Table 58: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, and trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [10]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

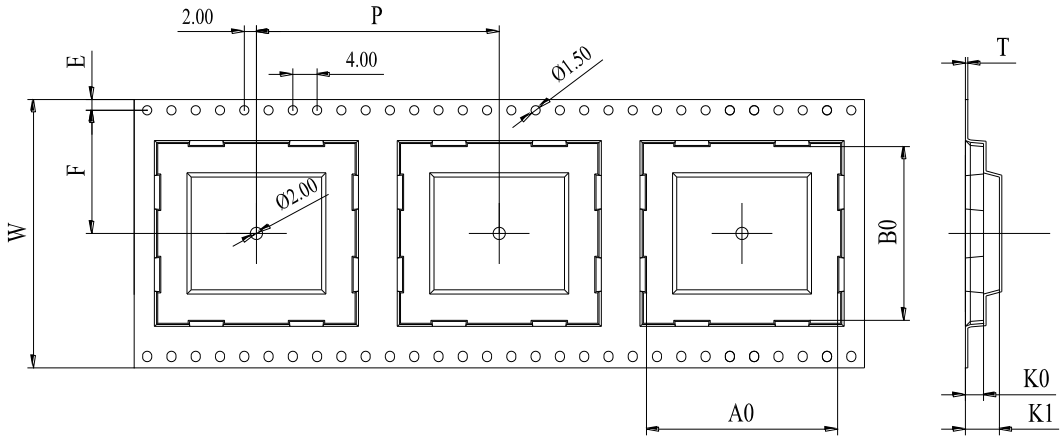


Figure 47: Carrier Tape Dimension Drawing (Unit: mm)

Table 59: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	20.2	24	3.15	6.65	20.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

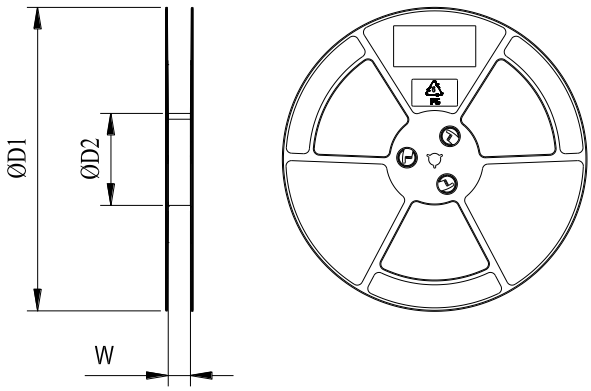


Figure 48: Plastic Reel Dimension Drawing

Table 60: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

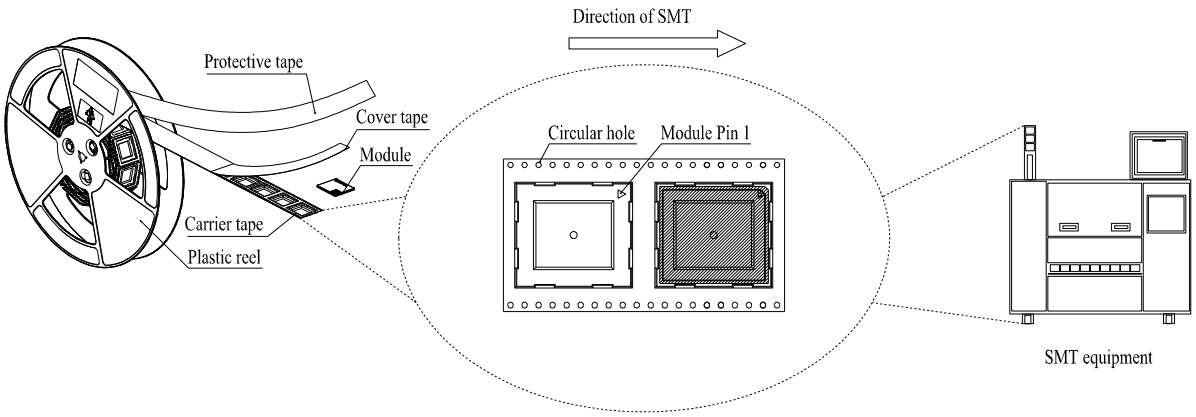
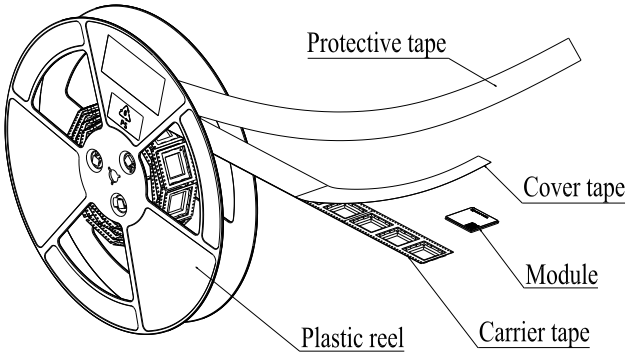


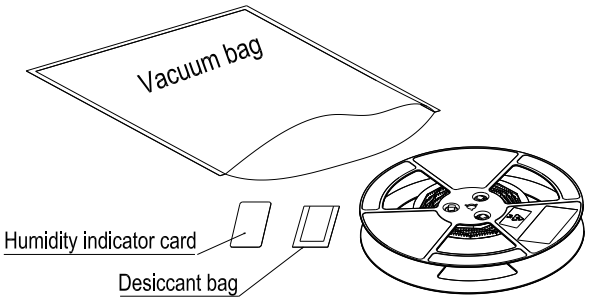
Figure 49: Mounting Direction

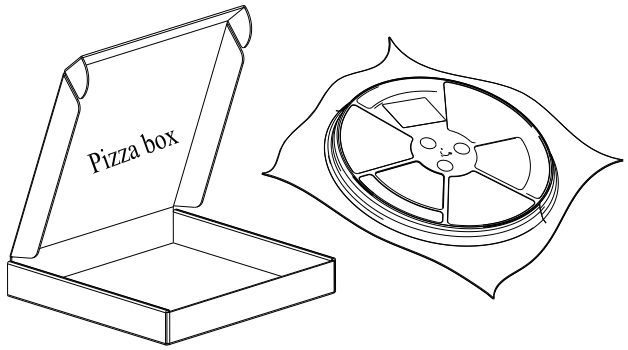
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

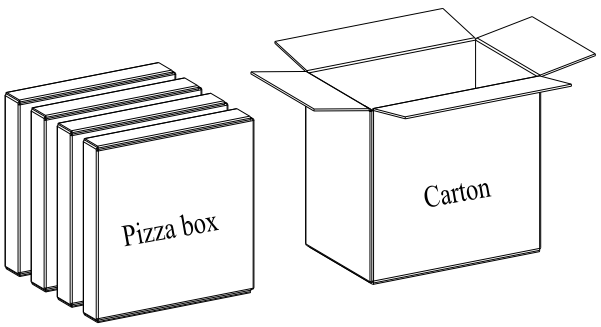


Figure 50: Packaging Process

9 Appendix References

Table 61: Related Documents

Document Name
[1] Quectel_EG915N_Series_QuecOpen_GPIO_Configuration
[2] Quectel_LTE_OPEN_EVB_User_Guide
[3] Quectel_EG91xN_Series_QuecOpen(SDK)_Device_Management_API_Reference_Manual
[4] Quectel_EG91xN_Series_QuecOpen(SDK)_Low_Power_Consumption_API_Reference_Manual
[5] Quectel_EC200S&EG91xN_Series_QuecOpen(SDK)_ADC_Development_Guide
[6] Quectel_EG91xN_Series_QuecOpen(SDK)_Booting&Shutdown_User_Guide
[7] Quectel_EG915N_Series_QuecOpen_Reference_Design
[8] Quectel_EG915N_Series_QuecOpen(SDK)_GNSS_API_Reference_Manual
[9] Quectel_RF_Layout_Application_Note
[10] Quectel_Module_SMT_Application_Note

Table 62: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
AMR-WB	Adaptive Multi-Rate Wideband
BB	Baseband
BDS	BeiDou Navigation Satellite System
bps	Bits Per Second

CEP	Circular Error Probable
CS	Coding Scheme
CTS	Clear To Send
DCE	Data Communications Equipment
DCS	Data Coding Scheme
DL	Downlink
DRX	Discontinuous Reception
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FDD	Frequency Division Duplex
FILE	File Protocol
FOTA	Firmware Over-The-Air
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP over SSL
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Global Navigation Satellite System (Russia)

GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPIO	General-Purpose Input/Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HTTP	Hyper Text Transfer Protocol
HTTPS	Hyper Text Transfer Protocol over Secure Socket Layer
IMT-2000	International Mobile Telecommunications 2000
Iomax	Maximum Output Load Current
I2C	Inter-Integrated Circuit
kbps	kilobits per second
LDO	Low Dropout Regulator
LGA	Land Grid Array
LNA	Low-Noise Amplifier
LSB	Least Significant Bit
LTE	Long Term Evolution
M2M	Machine to Machine
Mbps	Megabits per second
MCU	Microcontroller Unit
MCS	Modulation and Coding Scheme
ME	Mobile Equipment
MIC	Microphone
MLCC	Multi-layer Ceramic Capacitor

MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MO	Mobile Origination
MP	Million Pixel
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
MT	Mobile Terminating
NITZ	Network Identity and Time Zone
NMEA	(National Marine Electronics Association)0183 Interface Standard
NTP	Network Time Protocol
OTA	Over-the-air programming
PA	Power Amplifier
PAM	Power Amplifier Module
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PF	Paging Frame
PING	Packet Internet Groper
PMIC	Power Management IC
POS	Point of Sale
PPP	Point-to-Point Protocol
PSK	Pre-Shared Key/Phase Shift Keying

QZSS	Quasi-Zenith Satellite System
RAM	Random Access Memory
RHCP	Right Hand Circular Polarization
RF	Radio Frequency
RTS	Ready To Send/Request to Send
SAW	Surface Acoustic Wave
SBAS	Satellite-Based Augmentation System
SIM	Subscriber Identity Module
SIMO	Single Input Multiple Output
SMD	Surface Mount Device
SMS	Short Message Service
SMT	Surface Mount Technology
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
THD	Total Harmonic Distortion
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver &Transmitter
UDP	User Datagram Protocol
UL	Uplink
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module

VBAT	Voltage at Battery (Pin)
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio