EG912U-GL

Reference Design

LTE Standard Module Series

Version: 1.0

Date: 2023-01-17

Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2022-08-04	Anla HUANG	Creation of the document
1.0	2023-01-17	Anla HUANG	First official release

Contents

1 Reference Design

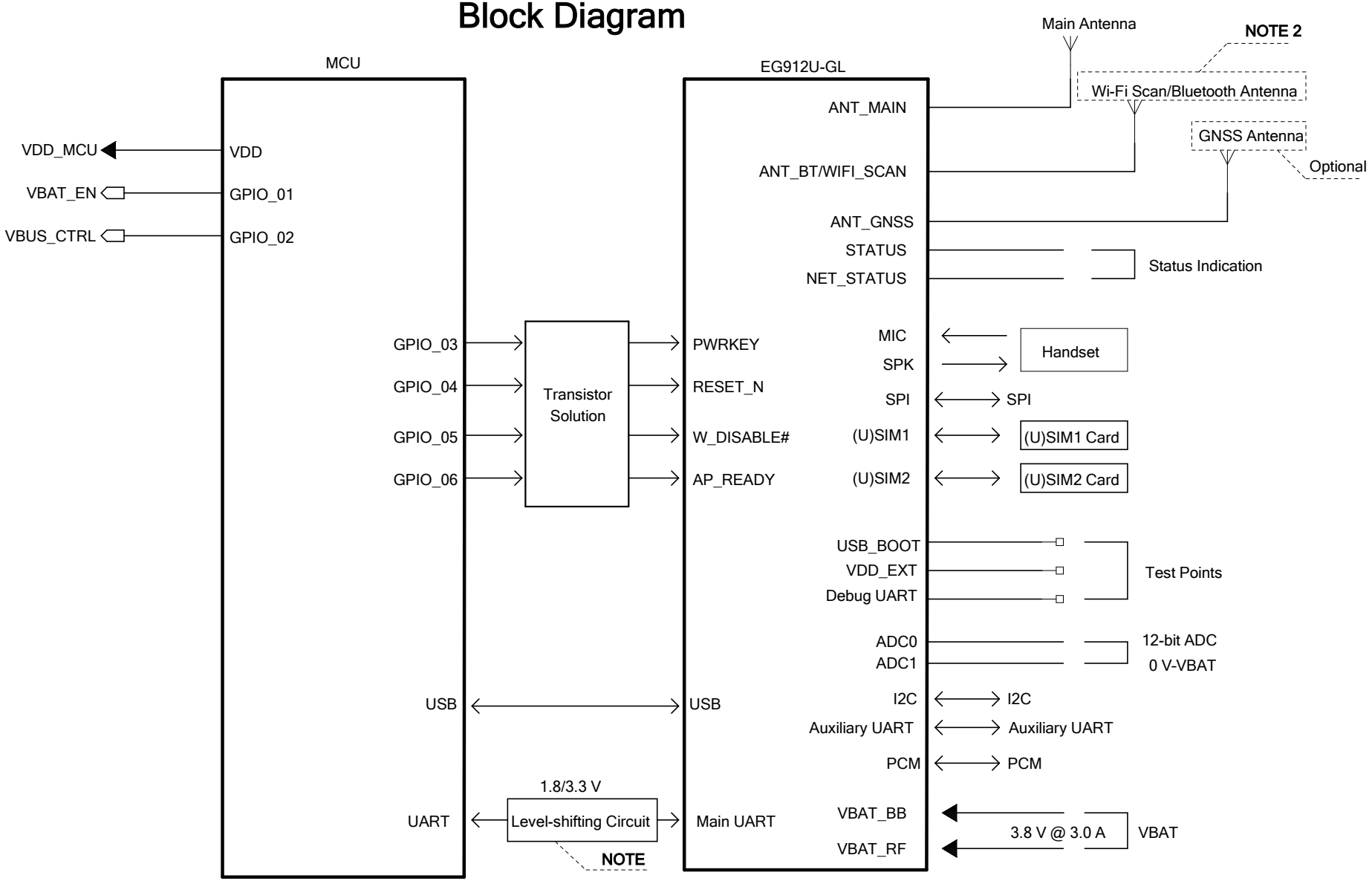
1.1. Introduction

This document provides the reference design for Quectel EG912U-GL module, including block diagrams of the module design, power supply, antenna interfaces, (U)SIM interfaces, analog audio interfaces, UART interface, indicators and other designs.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



NOTE:

1. A level-shifting circuit with a transistor or a voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.
2. The module supports both Wi-Fi Scan and Bluetooth functions. However, as the antenna interface is shared, two functions cannot be used simultaneously. Additionally, Bluetooth and Wi-Fi Scan functions are optional (both supported or not). For details, contact Quectel Technical Support.

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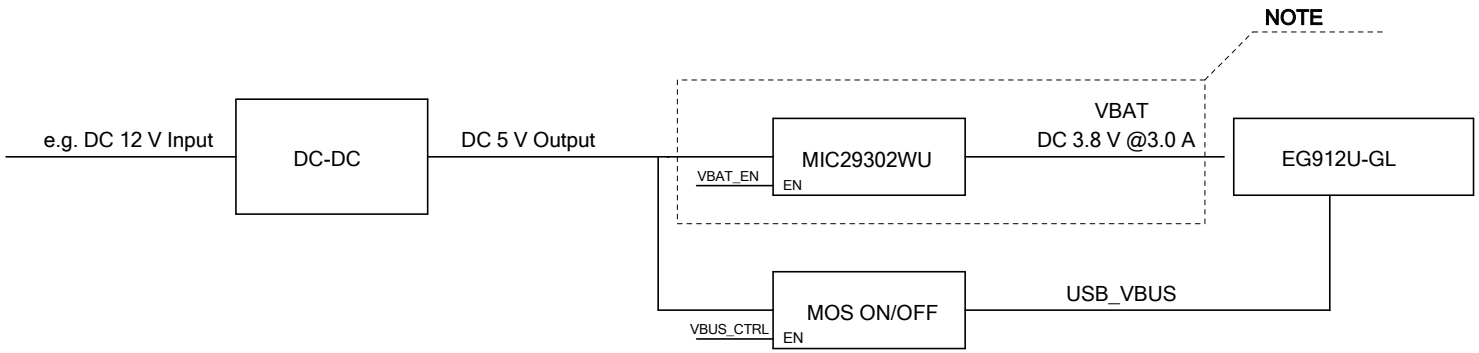
Power System Block Diagram



NOTE:
The LDO is used to convert the input voltage to typical 3.8 V and the power supply should provide at least 3 A current for the module.

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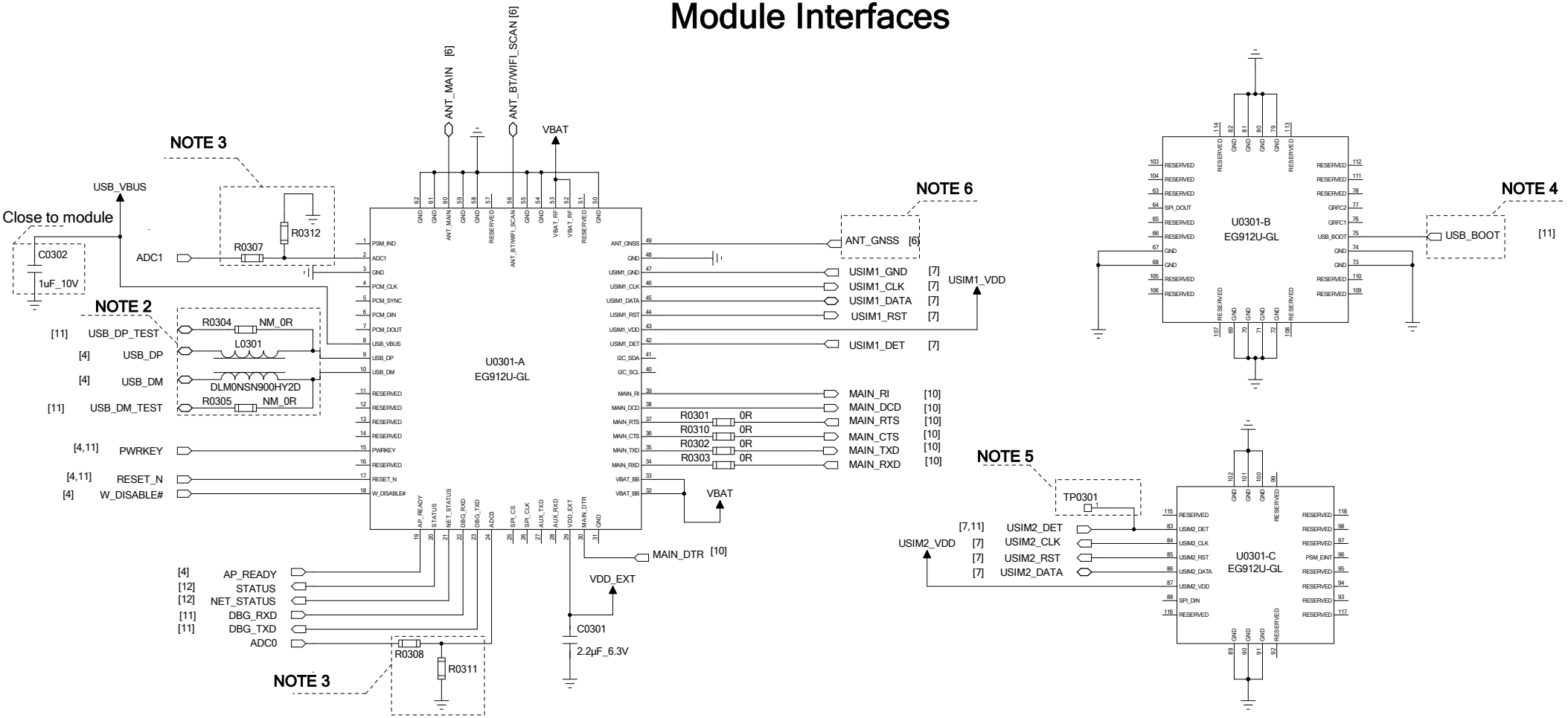
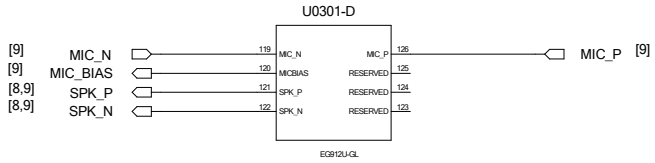
Module Interfaces



NOTE:

1. Keep unused and RESERVED pins open, and connect all GND pins to the ground network.
2. A common mode choke L0301 is recommended to be added in series between the module and your MCU in order to suppress EMI spurious transmission. Meanwhile, test points must be reserved for upgrading firmware and debugging software over USB interface and minimize the extra stubs of the trace. L0301 and the two resistors R0304, R0305 should be placed close to the module to ensure the integrity of USB signal.
3. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins, it is strongly recommended to reserve the voltage divider circuit for better compatibility with other Quectel modules. The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced. When the divider circuit is not used, the ADC pins require 1 kΩ resistors in series.
4. When emergency download function is not required, USB_BOOT cannot be pulled up before the module starts up.
5. A test point must be reserved for USIM2_DET pin for debugging.
6. GNSS antenna is optional for the module.



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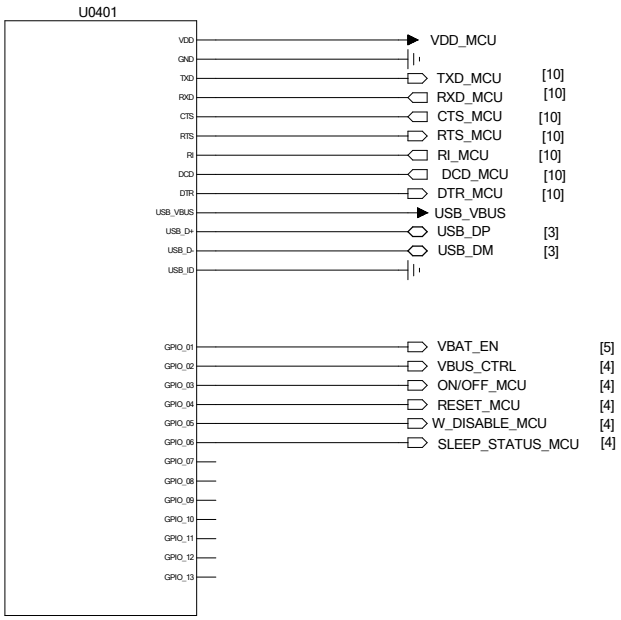
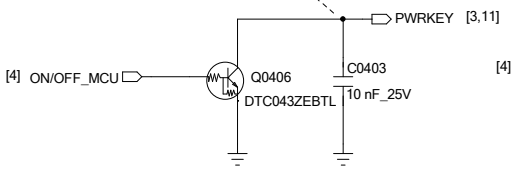
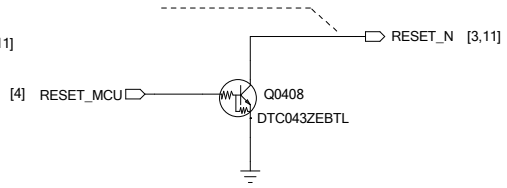
MCU Interfaces

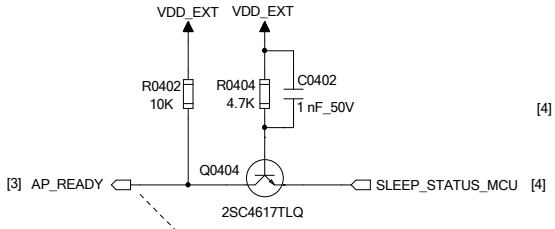


It is used to turn on or off the module.



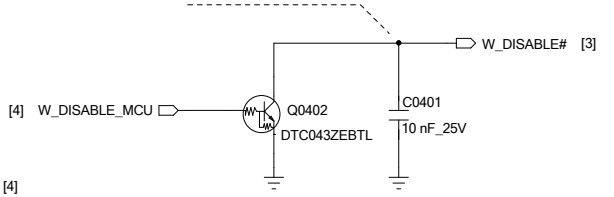
It is used to reset the module.



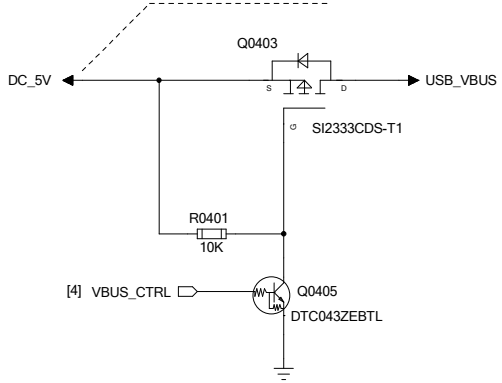


It is used to detect the sleep status of MCU.

It is used to make the module enter the airplane mode.



5 V power source from motherboard.



NOTE:

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V;
   if the GPIO interfaces of U0401 share the same power domain, then the related level-shifting circuit can be omitted.
2. The USB 2.0 interface of the module only serves as a slave device and supports high-speed and full-speed modes.
   To communicate with the USB interface, MCU needs to support USB host mode or OTG function. The USB_VBUS of the module and MCU should be powered by an external power system, and USB_VBUS is for USB detection. VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the default low-level GPIOs of MCU as the control pins for PWRKEY and RESET_N of the module.
   Ensure that the maximum load capacitance of PWRKEY and RESET_N does not exceed 10 nF.

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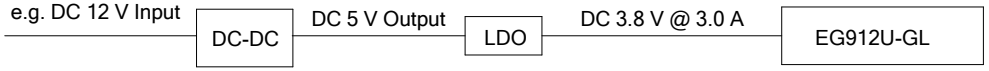
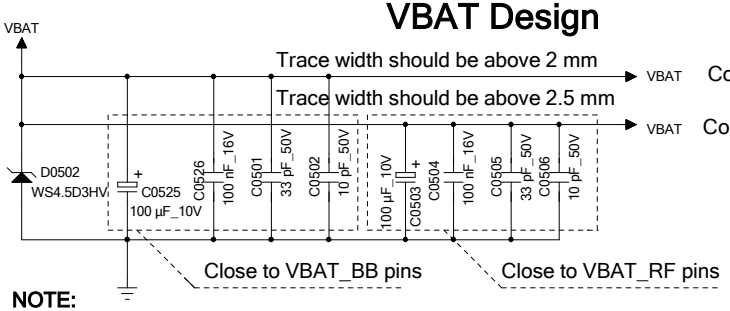
Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC to convert the high input voltage to a 5.0 V output, and then use an LDO to convert it to 3.8 V to power the module.



VBAT Design

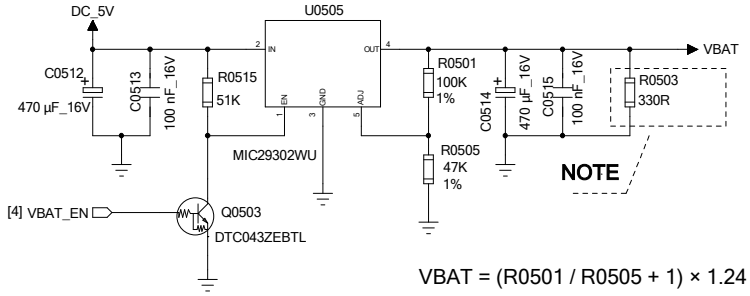


NOTE:

1. For more information about power supply of module, refer to *Quectel_EG912U-GL_Hardware_Design.*
2. The VBAT traces must be connected to pins VBAT_BB and VBAT_RF in a star configuration.
3. The recommended operating voltage of VBAT ranges from 3.3 V to 4.3 V, and the typical value is 3.8 V.

LDO Application

When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



$$VBAT = (R0501 / R0505 + 1) \times 1.24 = 3.88\ V$$

NOTE:

The recommended load current is greater than 10 mA.

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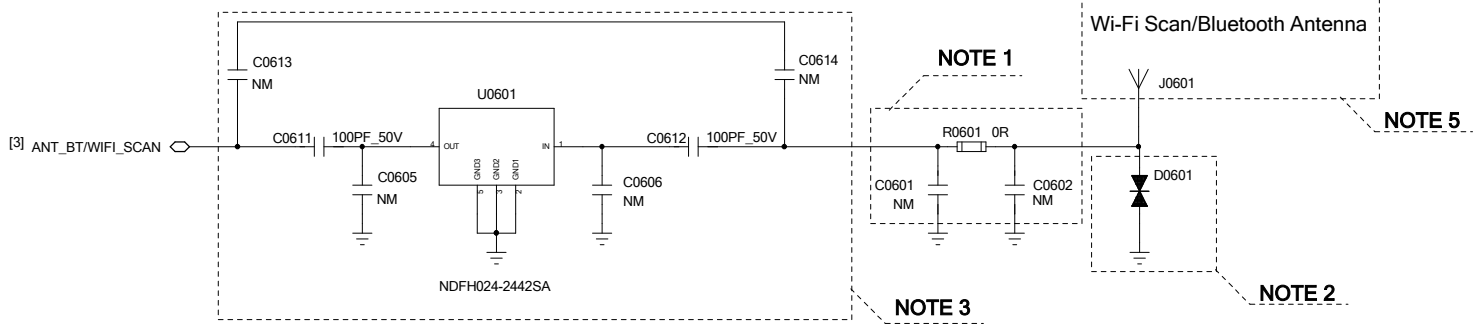
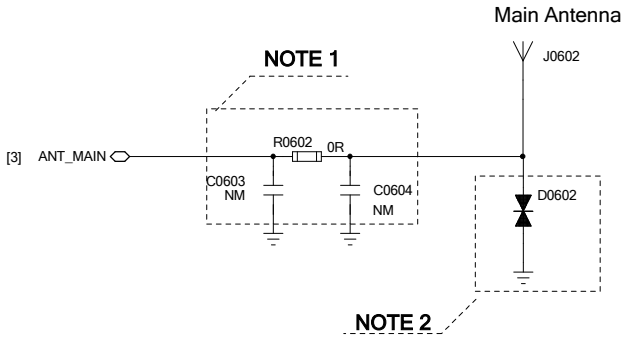
Antenna Interface Design

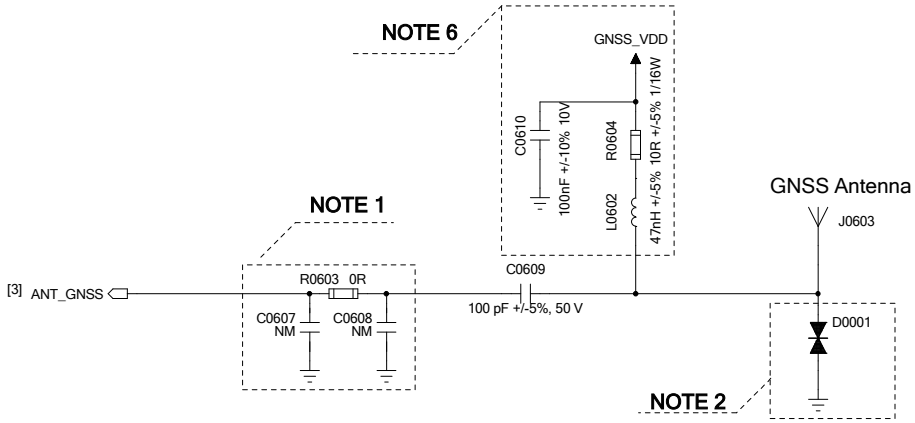
Wi-Fi Scan/Bluetooth Antenna Design



Main Antenna Design



GNSS Antenna Design (Optional)



NOTE:

1. It is highly recommended to reserve a Π type matching circuit for future debugging.
2. It is recommended that the junction capacitance and peak reverse working voltage of the ESD protection components do not exceed 0.05 pF and 5 V respectively.
3. You can also select the solution with C0613 and C0614 in the compatible design. In this case, C0605, C0606, C0611, C0612 and U0601 are not mounted by default.
4. The single-ended impedance of the RF antenna is 50 Ω.
5. The module supports both Wi-Fi Scan and Bluetooth functions. However, as the antenna interface is shared, the two functions cannot be used simultaneously. Additionally, Bluetooth and Wi-Fi Scan functions are optional (both supported or not). For details, contact Quectel Technical Support.
6. The active GNSS antenna requires an external power supply, and the GNSS_VDD nominal value of the power supply is 3.3 V @ 30 mA. The passive GNSS antenna does not require a GNSS_VDD circuit.

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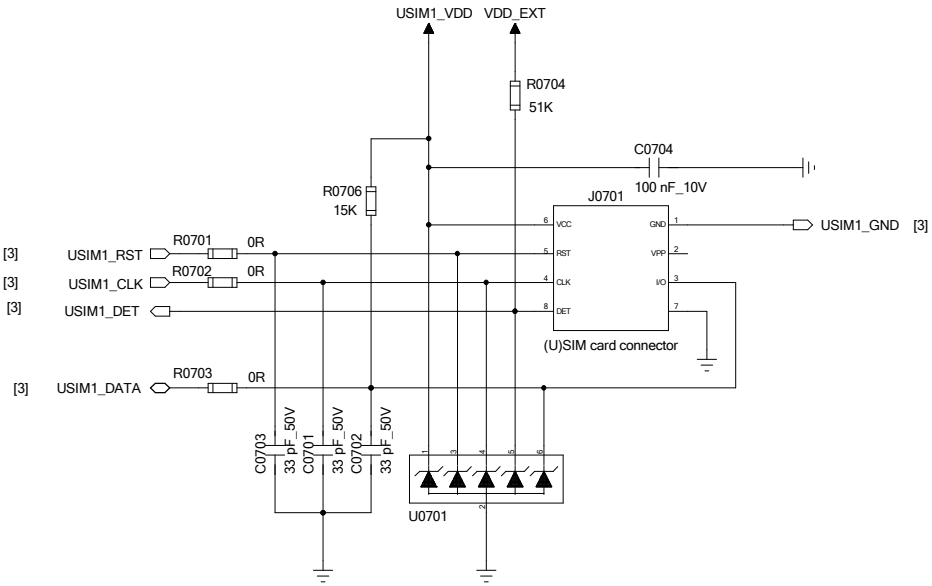
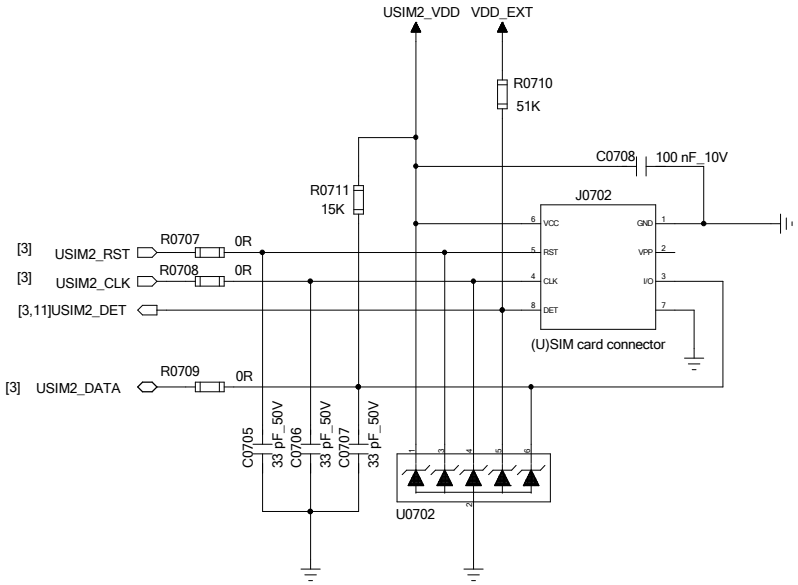
(U)SIM Interface Design

(U)SIM1



(U)SIM2



NOTE:

1. U0701 and U0702 are recommended to be used to offer good ESD protection, and the parasitic capacitance should not exceed 15 pF.
2. The pull-up resistors R0706 and R0711 can improve anti-jamming capability, and they should be placed close to the (U)SIM card connector.
3. R0701-R0703 and R0707-R0709 are used for debugging, and C0701-C0703 and C0705-C0707 are used for filtering out RF interference.
4. C0704 and C0708's capacitance should be less than 1 μF and they should be placed close to the (U)SIM card connector.
5. The GND of the (U)SIM card connector is recommended to be connected to the main GND layer directly.
6. The module supports (U)SIM card hot-swap via the USIM_DET pin and both high- and low-level detections are supported. The function is disabled by default.
7. For more information about the layout of (U)SIM interface, refer to *Quectel_EG912U-GL_Hardware_Design*.

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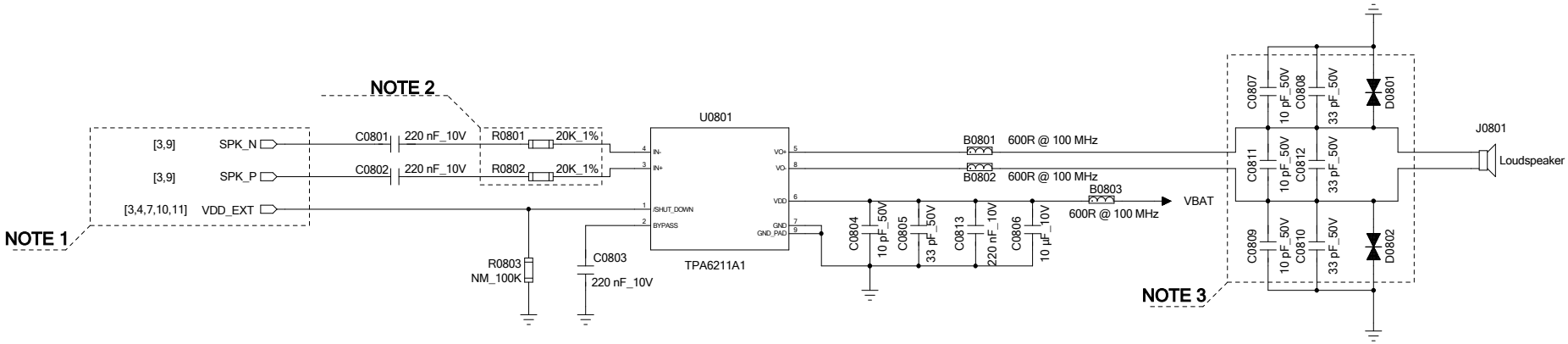
Analog Audio Design (External Audio Power Amplifier)



NOTE:

1. SPK_N and SPK_P are differential output channels. When the channels are turned on or off, it is possible for the module to emit a pop sound, which can be eliminated by controlling the enable pin of the audio PA. For details, contact Quectel Technical Support.
2. Choose the audio power amplifier with appropriate power according to the actual needs. Audio PA Gain = 40 kΩ / R0801 or R0802.
3. Place filter capacitors and ESD protection components close to the loudspeaker and the selection of ESD protection components is related to the selection of audio power amplifiers. Ensure that the output voltage of the audio power amplifier is within the maximum reverse working voltage range of the ESD protection components.

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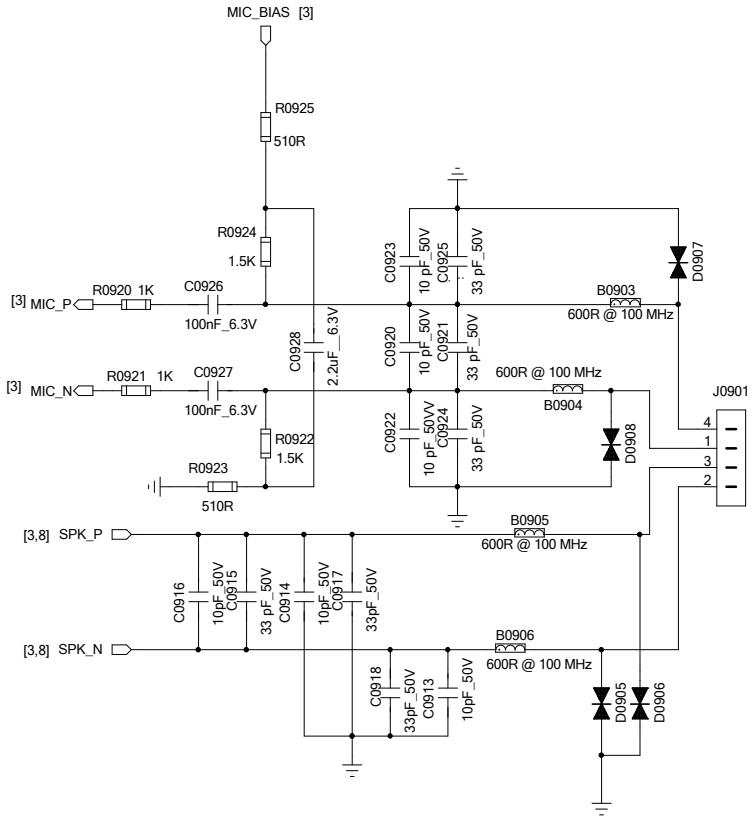
Analog Audio Design (Handset)



NOTE:

1. Both the MIC and SPK signal traces need to be routed as differential pairs.
2. All MIC and SPK signal traces should be surrounded with ground on the layer and with ground planes above and below, and far away from noise sources.
3. ESD protection components should be placed as close to the audio interfaces as possible
   and ensure that the audio voltage is within the maximum reverse working voltage range of the ESD protection components.

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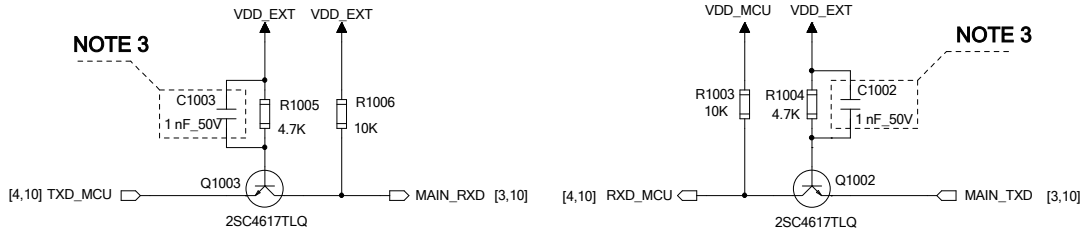
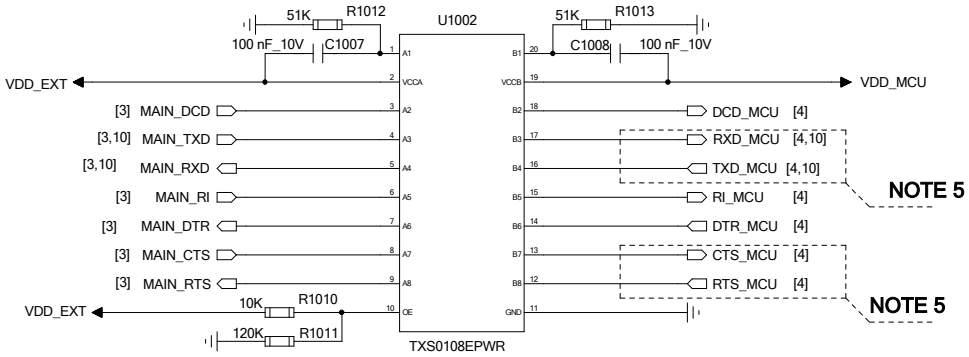
UART Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, and the latter of which is recommended.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, refer to the datasheet of TXS0108EPWR.
3. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C1002 and C1003 of 1 nF can improve the signal quality.
4. The MAIN_RTS and MAIN_DTR level-shifting circuits are similar to that of the MAIN_RXD.
   The MAIN_CTS, MAIN_RI and MAIN_DCD level-shifting circuits are similar to that of the MAIN_TXD.
5. The hardware flow control pins MAIN_CTS and MAIN_RTS adopt the direct connection mode, that is,
   the module CTS is connected to the MCU CTS, and the module RTS is connected to the MCU RTS. In addition, pay attention to the direction of connection.
   MAIN_TXD and MAIN_RXD adopt a cross connection mode, that is, the TXD and RXD of the module are respectively connected to the RXD and TXD of the MCU.

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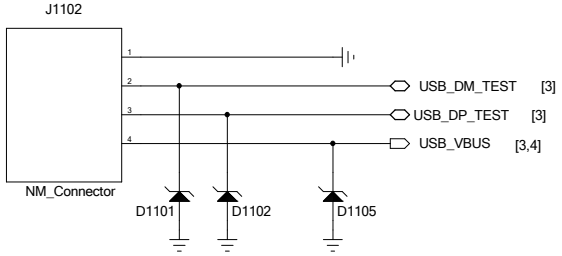
Reserved Test Points

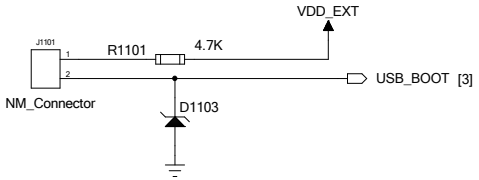
USB Interface Test Points



NOTE:

1. Test points must be reserved for USB interface.
2. The module can upgrade the firmware and debug the software over USB interface test points.
3. The parasitic capacitance of the ESD protection components on USB data traces should not exceed 2 pF. Ensure that the signal voltage is within the maximum reverse working voltage range of the ESD protection components.

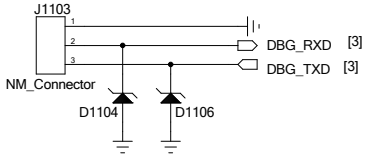
USB_BOOT Interface Test Points



NOTE:

1. It is recommended to reserve a test point for USB_BOOT interface.
2. Pull up the USB_BOOT to VDD_EXT before the module starts up, and the module will enter emergency download mode after powering up. In this mode, the module supports firmware upgrade over USB interface.

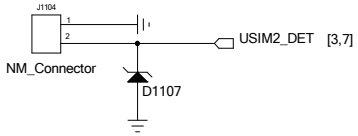
Debug UART Test Points



NOTE:

1. Test points must be reserved for DBG_TXD and DBG_RXD for debugging.
2. The debug UART interface supports 1.8 V power domain, and a level-shifting circuit should be used if the power domain of your application is 3.3 V. For details, refer to "UART Interface Design" sheet.
3. The debug UART only supports the baud rate of 921600 bps.

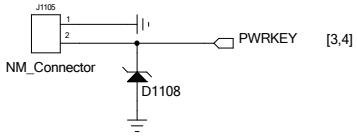
USIM2_DET Test Point



NOTE:

1. A test point must be reserved for USIM2_DET for debugging.
2. USIM2_DET supports 1.8 V power domain.

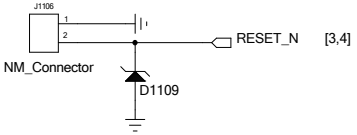
PWRKEY Test Point



NOTE:

It is recommended to reserve a test point for PWRKEY.

RESET_N Test Point



NOTE:

It is recommended to reserve a test point for RESET_N.

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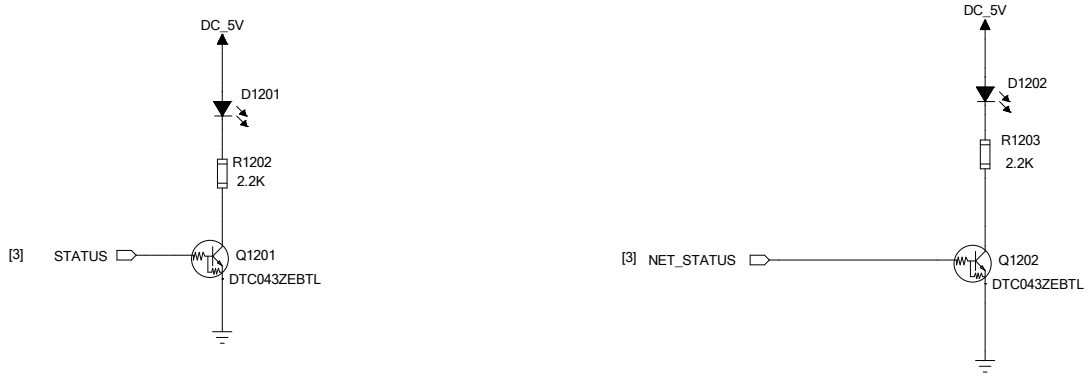
Indicator Design



NOTE:

1. For more details about STATUS and NET_STATUS, refer to *Quectel_EG912U-GL_Hardware Design.*
2. If the low power consumption is required when your device is in sleep status, replace the power supply DC_5V of the STATUS and NET_STATUS indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

Quectel Wireless Solutions		
DRAWN BY Anla HUANG	PROJECT EG912U-GL	TITLE Reference Design
CHECKED BY Vane WANG	SIZE A2	VER 1.0
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