EG912U-GL QuecOpen Hardware Design

LTE Standard Module Series

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-02-18	Anla HUANG/ Nick QIN/ Loft XU	Creation of the document
1.0	2023-08-17	Phoebe FU/ Chris LIANG/ Loft XU	First official release

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

The document defines the EG912U-GL QuecOpen® module and describes its air interfaces and hardware interfaces which are connected with your applications. This document can help you quickly understand interface specifications, RF characteristics, electrical and mechanical details, as well as other information of the module.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument and so on, it indicates that the function, feature, interface, pin, AT command, argument and so on, are under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

The module is an SMD module with compact packaging, which is engineered to meet most of the demands of M2M applications, for instance:

- POS
- PoC
- ETC
- Shared equipment
- Data card
- Energy control and monitoring
- Security and protection
- Industrial PDA

Table 2: Brief Introduction of Module

Category	
Packaging and Number of Pins	LGA; 126 pins
Dimensions	(29.0 ±0.2) mm × (25.0 ±0.2) mm × (2.4 ±0.2) mm
Weight	Approx. 3.67 g
Wireless Technologies	GSM, LTE, GNSS (optional), Bluetooth/Wi-Fi Scan [1]

[1] The module supports both Wi-Fi Scan and Bluetooth functions. However, as the antenna interface is shared, the two functions cannot be used simultaneously. Additionally, Bluetooth and Wi-Fi Scan functions are optional. For details, contact Quectel Technical Support.

2.1. Frequency Bands and Functions

Table 3: Frequency Bands

Wireless Technology	EG912U-GL
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B12/B13/B17/B18/B19/B20/B25/B26/B28/B66
LTE-TDD	B34/B38/B39/B40/B41
GSM	GSM850/EGSM900/DCS1800/PCS1900
GNSS (Optional)	GPS, GLONASS, BDS, Galileo, QZSS
Bluetooth [1]	Bluetooth 4.2
Wi-Fi Scan [1]	2.4 GHz 802.11b (Rx)

2.2. Key Features

Table 4: Key Features

Feature	Description
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● GSM850: Class 4 (33 dBm ±2 dB) ● EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800: Class 1 (30 dBm ±2 dB) ● PCS1900: Class 1 (30 dBm ±2 dB) ● LTE-FDD band: Class 3 (23 dBm ±2 dB) ● LTE-TDD band: Class 3 (23 dBm ±2 dB)
LTE Features	● Supports up to 3GPP Rel-13 Cat 1 FDD/TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports uplink QPSK and 16QAM ● Supports downlink QPSK, 16QAM, and 64QAM ● Max. transmission data rates: LTE-FDD: 10 Mbps (DL)/5 Mbps (UL) LTE-TDD: 8.96 Mbps (DL)/3.1 Mbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12

	● Coding scheme: CS 1–4 ● Max. transmission data rates: 85.6 kbps (DL)/85.6 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/ FTPS/SSL/FILE/MQTT/MMS/SMTP/SMTPS protocols ● Supports PAP and CHAP for PPP connections
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM card and ME; ME by default
USB Interface	● Compliant with USB 2.0 specification (slave mode only), with maximum transmission rate up to 480 Mbps ● Used for data transmission, software debugging and firmware upgrade ● Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–6.5, and Android 4.x–13.x
USB_BOOT Interface	● Supports one USB_BOOT interface ● Forces the module into emergency download mode
(U)SIM Interfaces	● Supports (U)SIM card: 1.8/3.0 V ● Supports Dual SIM Single Standby
UART Interfaces	**Main UART** ● Used for data transmission ● Baud rates: up to 921600 bps; 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART** ● Used for log output and Linux console ● Baud rate: 921600 bps ● Cannot be used as a general-purpose UART **Auxiliary UART** ● The baud rate is the same as that of the main UART
PCM Interface	● Supports one PCM interface (slave mode only) ● Used for audio data transmission between the module and the external codec
I2C Interface	● Supports one I2C interface ● Complies with the I2C-bus Specification
Audio Features	● Supports one analog audio input and two analog audio output channels ● HR/FR/EFR/AMR/AMR-WB ● Supports echo cancellation and noise suppression
ADC Interfaces	Supports two ADC Interfaces
SPI Interface	● Supports one SPI interface (master mode only) ● 1.8 V voltage domain ● Clock rate: up to 25 MHz
External Flash Interface	● Supports connection to external flash chip

	● The external flash interface is multiplexed from other pins
LCM Interface	● Supports LCM interface in SPI mode
SD Card Interface	● Supports one interface compliant with SD 2.0 specification and can be used for external SD card ● Partial SD card pins can be multiplexed from other pins
Camera Interface	● Supports one camera interface ● Supports cameras up to 0.3 MP ● I/O interface only supports 1.8 V power domain ● Supports SPI two-data-line data transmission
Indication Signal	● NET_STATUS indicates module's network activity status ● STATUS indicates module's operation status
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Bluetooth/Wi-Fi Scan antenna interface (ANT_BT/WIFI_SCAN [2]) ● GNSS antenna interface (ANT_GNSS) (optional) ● 50 Ω impedance
Position Fixing	Supports Wi-Fi Scan and GNSS (optional)
Temperature Range	● Operating temperature range: -35 °C to +75 °C [3] ● Extended temperature range: -40 °C to +85 °C [4] ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	Via USB interface and DFOTA
RoHS	All hardware components are fully compliant with EU RoHS Directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- Memory
- Radio frequency
- Peripheral interfaces

[2] The module supports both Wi-Fi Scan and Bluetooth functions. However, as the antenna interface is shared, the two functions cannot be used simultaneously. Additionally, Bluetooth and Wi-Fi Scan functions are optional. For details, contact Quectel Technical Support.
[3] Within operating temperature range, the module meets 3GPP specifications.
[4] Within extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

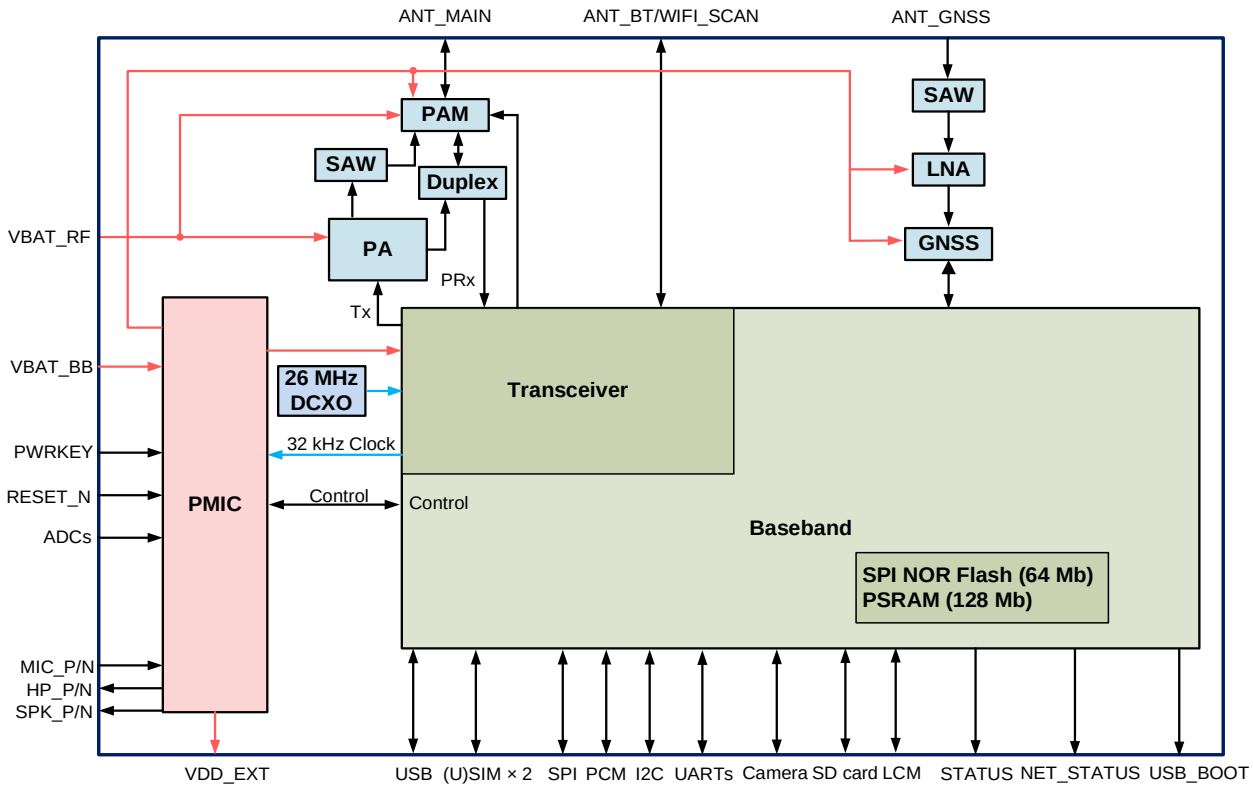


Figure 1: Functional Diagram

NOTE

1. The module supports both Wi-Fi scan and Bluetooth functions. However, as the antenna interface is shared, the two functions cannot be used simultaneously. Additionally, Bluetooth and Wi-Fi scan functions are optional. For details, contact Quectel Technical Support.
2. GNSS function of the module is optional.

2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

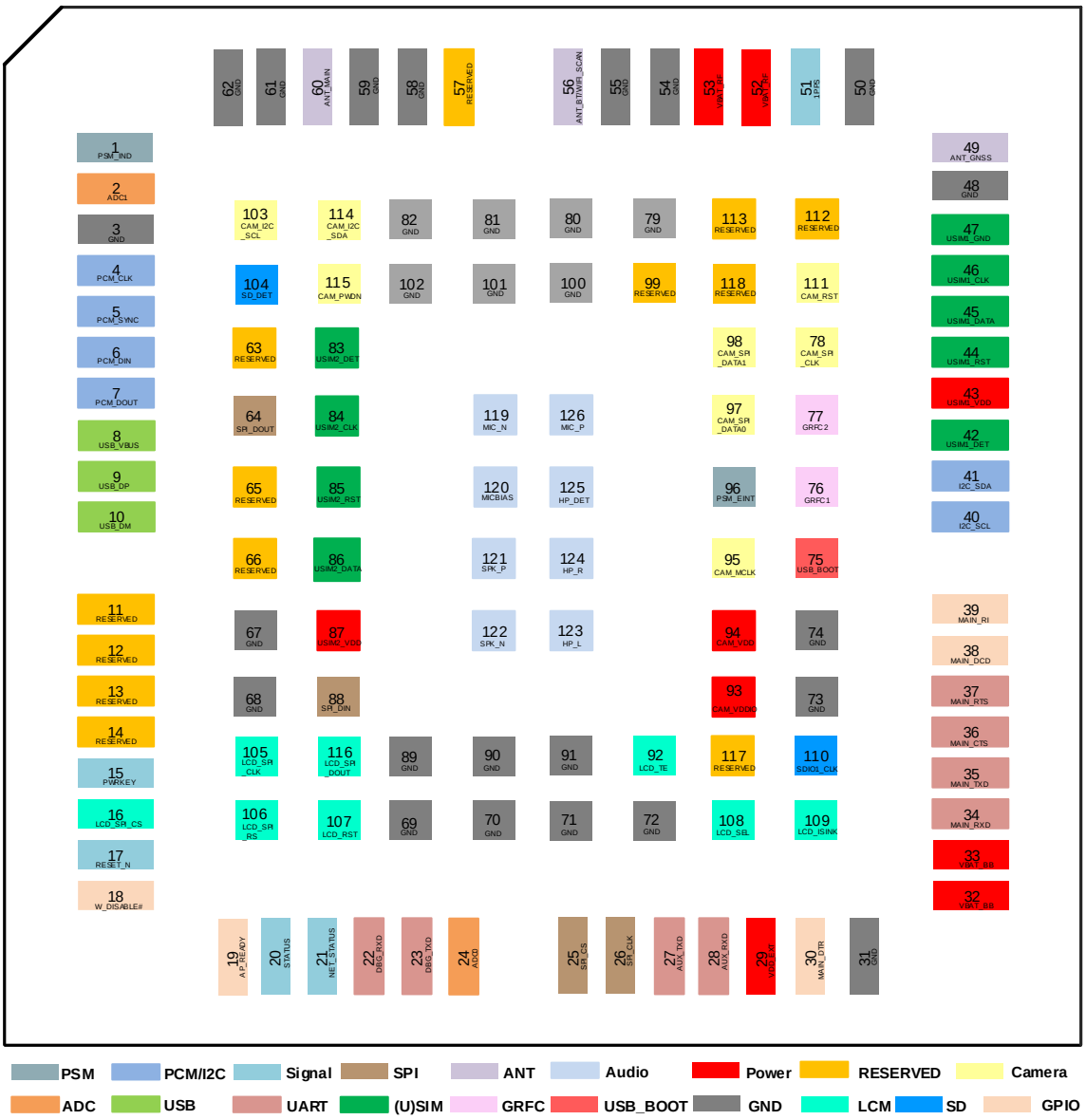


Figure 2: Pin Assignment (Top View)

NOTE

1. If the emergency download function is not used, USB_BOOT cannot be pulled up before the module's startup.
2. Keep all RESERVED pins and unused pins unconnected, and connect all GND pins to ground.
3. The module supports Dual SIM Single Standby. For details, contact Quectel Technical Support.

4. When using pin 18 (W_DISABLE#), pin 19 (AP_READY), pin 30 (MAIN_DTR), pin 38 (MAIN_DCD), pin 39 (MAIN_RI), and pin 110 (SDIO1_CLK), please note that these pins will have a period of variable level state (not controllable by software) after the module is turned on: at high level (3 V) for 2 s and then at low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable level output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

2.5. Pin Description

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rate current.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current of at least 1.0 A.

VBAT_RF	52, 53	PI	Power supply for the module's RF part		It must be provided with sufficient current of at least 2.5 A.
VDD_EXT	29	PO	Provides 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Used with a 2.2 μF capacitor and TVS. It is recommended to reserve a test point.
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turns on/off the module	V_{IL}max = 0.5 V VBAT power domain	Active low. It is recommended to reserve a test point.
RESET_N	17	DI	Resets the module		Active low. A test point is recommended to be reserved if unused.
Indication Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicates the module's operation status	1.8 V power domain	If unused, keep them open.
NET_STATUS	21	DO	Indicates the module's network activity status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	AI	USB connection detect	Input voltage range: 3.5–5.25 V	A test point must be reserved for debugging.
USB_DP	9	AIO	USB differential data (+)		USB 2.0 compliant. Requires differential impedance of 90 Ω. Test points must be reserved for debugging.
USB_DM	10	AIO	USB differential data (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_O$max = 50 mA	Either 1.8 V or 3.0 V (U)SIM card is

					supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data		
USIM1_CLK	46	DO	(U)SIM1 card clock		
USIM1_RST	44	DO	(U)SIM1 card reset		
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain	If unused, keep it open.
USIM1_GND	47	-	Specified ground for (U)SIM 1		
USIM2_VDD	87	PO	(U)SIM2 card power supply	$I_O$max = 50 mA	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA	86	DIO	(U)SIM2 card data		
USIM2_CLK	84	DO	(U)SIM2 card clock		
USIM2_RST	85	DO	(U)SIM2 card reset		
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain	A test point must be reserved for debugging.
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	36	DO	Clear to send signal from the module	1.8 V power domain	Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	37	DI	Request to send signal to the module		Connect to MCU's RTS. If unused, keep it open.
MAIN_RXD	34	DI	Main UART receive		If unused, keep them open.
MAIN_TXD	35	DO	Main UART transmit		
Auxiliary UART					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
AUX_TXD	27	DO	Auxiliary UART transmit	1.8 V power domain	If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive		
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain	Test points must to be reserved for debugging.
DBG_TXD	23	DO	Debug UART transmit		
PSM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PSM_EINT	96	DI	External interrupt, wakes up the module from PSM	1.8 V power domain	Wakes up the module from PSM when being pulled high externally. If unused, keep it open.
PSM_IND*	1	DO	Indicates the module's power saving mode	1.8 V power domain	If unused, keep it open.
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	40	OD	I2C serial clock	1.8 V power domain	External 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	5	DI	PCM data frame sync	1.8 V power domain	If unused, keep them open. Supports slave mode only.
PCM_CLK	4	DI	PCM clock		
PCM_DIN	6	DI	PCM data input		
PCM_DOUT	7	DO	PCM data output		

Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface		50 Ω characteristic impedance.
ANT_BT/ WIFI_SCAN	56	AIO/ AI	Shared interface for Bluetooth and Wi-Fi Scan		Bluetooth and Wi-Fi Scan cannot be used at the same time. Wi-Fi Scan antenna can only receive but not transmit. 50 Ω characteristic impedance. If unused, keep it open.
ANT_GNSS	49	AI	GNSS antenna interface		50 Ω characteristic impedance. If unused, keep it open.
Antenna Tuner Control Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	76	DO	Generic RF controller	1.8 V power domain	If unused, keep them open.
GRFC2	77	DO			
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CLK	26	DO	SPI clock	1.8 V power domain	If unused, keep them open. Supports master mode only.
SPI_CS	25	DO	SPI chip select		
SPI_DIN	88	DI	SPI data input		
SPI_DOUT	64	DO	SPI data output		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General-purpose ADC interfaces	Voltage range: 0 V to VBAT	It is recommended to reserve a voltage divider circuit. If unused, keep them open.
ADC1	2	AI			

Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_N	119	AI	Microphone analog input (-)		If unused, keep them open.
MIC_P	126	AI	Microphone analog input (+)		
MICBIAS	120	PO	Bias voltage output for microphone	Vmax = 3.0 V Vmin = 2.2 V Vnom = 2.2 V	
SPK_P	121	AO	Analog audio differential output (+)		If unused, keep them open.
SPK_N	122	AO	Analog audio differential output (-)		
HP_L	123	AO	Headphone left channel output		If unused, keep them open.
HP_R	124	AO	Headphone right channel output		
HP_DET	125	DI	Headphone hot-plug detect		
USB_BOOT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	75	DI	Forces the module into emergency download mode	1.8 V power domain	Active high. A circuit that can set the module into emergency download mode should be reserved during design. A test point is recommended to be reserved.
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_SPI_CS	16	DO	LCD chip select	1.8 V power domain	If unused, keep them open.
LCD_TE	92	DI	LCD tearing effect		
LCD_SPI_CLK	105	DO	LCD clock		

LCD_SPI_RS	106	DO	LCD register select		
LCD_RST	107	DO	LCD reset		
LCD_SEL	108	DO	Reserved		
LCD_SPI_DOUT	116	DIO	LCD data		
LCD_ISINK	109	PI	Sink current input. Backlight adjustment.	Imax = 200 mA. Current is configurable.	It is driven by the current sink method and connected to the backlight cathode; the brightness can be adjusted with current control.
Camera Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CAM_VDDIO	93	PO	Digital power supply of camera	Vnom= 1.8 V $I_O$max = 100 mA	If unused, keep them open.
CAM_VDD	94	PO	Analog power supply of camera	Vnom= 2.8 V $I_O$max = 100 mA	
CAM_SPI_CLK	78	DI	SPI clock of camera	1.8 V power domain	
CAM_MCLK	95	DO	Master clock of camera		
CAM_SPI_DATA0	97	DI	SPI data 0 of camera		
CAM_SPI_DATA1	98	DI	SPI data 1 of camera		
CAM_RST	111	DO	Reset of camera		
CAM_PWDN	115	DO	Power down of camera		
CAM_I2C_SCL	103	OD	I2C clock of camera		Pull each of them up to 1.8 V power domain with an external resistor. If unused, keep them open.
CAM_I2C_SDA	114	OD	I2C data of camera		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_DET	104	DI	SD card hot-plug detect	1.8 V power domain	If unused, keep them open.

1PPS	51	DO	Pulse signal output		
SDIO1_CLK	110	DO	SD card clock	3.2 V power domain	
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_DCD	38	DIO	General purpose input/output	1.8 V power domain	Used as GPIO by default.
MAIN_RI	39	DIO			
MAIN_DTR	30	DIO			
W_DISABLE#	18	DIO			
AP_READY	19	DIO			
GND Pins					
Pin Name	**Pin No.**				
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
RESERVED pins					
Pin Name	**Pin No.**				
RESERVED	11–14, 57, 63, 65, 66, 99,112, 113, 117, 118,				

NOTE

Pins 18, 19, 30, 38 and 39 (W_DISABLE#, AP_READY, MAIN_DTR, MAIN_DCD, MAIN_RI) are not defined with functions corresponding to the pin names, but are used as GPIOs by default. For GPIO configurations, see ***document [1]***.

2.6. EVB Kit

Quectel supplies an evaluation board (LTE OPEN EVB) with accessories to develop or test the module. For more details, see ***document [2]***.

3 Operating Characteristics

3.1. Operating Modes

The following table briefly outlines the operating modes referred in the following chapters.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module remains registered on the network and is ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transmission rate.
Minimum Functionality Mode	● *ql_dev_set_modem_fun()* can set the module to a minimum functionality mode without removing the power supply. ● In this case, both RF function and (U)SIM card are invalid.	
Airplane Mode	● *ql_dev_set_modem_fun()* can set the module to airplane mode. ● In this mode, RF function is invalid.	
Sleep Mode	In this mode, current consumption of the module is reduced to a low level. The module remains the ability to receive paging message, SMS, voice calls and TCP/UDP data from network normally.	
PSM Mode	In this mode, current consumption of the module is reduced to a minimized level. API function cannot be sent to the module, but the module remains the ability to receive paging message from station and be woken up to work.	
Power Down Mode	PMU shuts down the power supply. Software is not active. However, operating voltage connected to VBAT_BB/VBAT_RF pins remains applied.	

NOTE

For more details about API function, see ***document [3]***.

3.2. Sleep Mode

The module can reduce its power consumption to a low level in the sleep mode. The following chapters describe power saving procedures of the module.

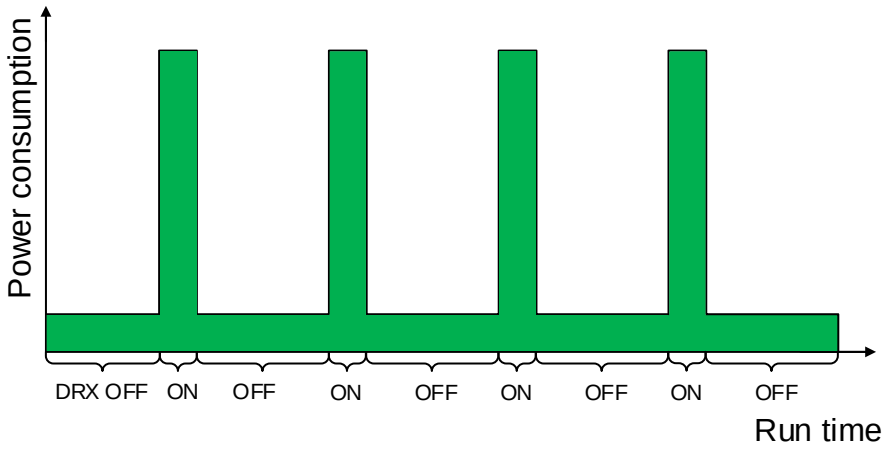


Figure 3: Power Consumption During Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. USB Application with USB Suspend/Resume Function

For the following two scenarios:

- The host supports USB suspend/resume and remote wake-up functions
- The host supports USB suspend/resume, but does not support remote wake-up function

The following three preconditions must be met to make the module enter sleep mode:

- Enable sleep function by using *ql_autosleep_enable()*. See ***document [4]*** for details.
- Ensure that all wakelocks have been released.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure illustrates the connection between the module and the host.

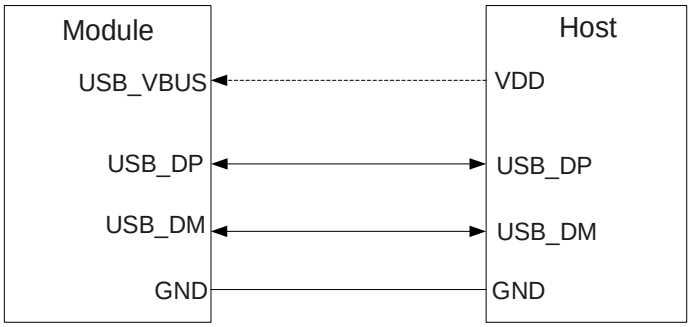


Figure 4: Sleep Mode Application with Suspend/Resume Function

You can wake up the module by sending data to it through USB.

NOTE

USB suspend is supported on Linux system but not on Windows system.

3.2.2. USB Application Without USB Suspend Function

If the host does not support USB suspend function, disconnect USB_VBUS with an external control circuit to make the module enter sleep mode.

- Enable sleep function by using *ql_autosleep_enable()*.
- Ensure that all wakelocks have been released.
- Disconnect USB_VBUS.

The following figure illustrates the connection between the module and the host.

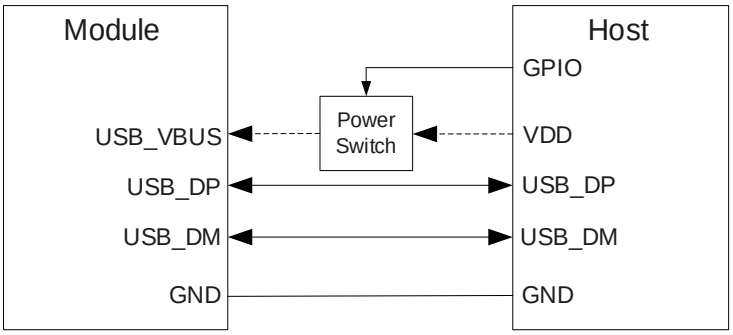


Figure 5: Sleep Mode Application Without Suspend Function

You can wake up the module by turning on the power switch to supply power to USB_VBUS.

NOTE

Pay attention to the level match shown in dotted line between the module and the host.

3.3. Airplane Mode

When the module enters airplane mode, the RF function does not work and APIs related to the RF function are inaccessible.

ql_dev_set_modem_fun() provides the choice of functionality level through setting parameter *at_dst_cfun* into 0, 1 or 4.

- *at_dst_cfun* is 0: Minimum functionality mode. Both RF and (U)SIM functions are disabled.
- *at_dst_cfun* is 1: Full functionality mode (by default).
- *at_dst_cfun* is 4: airplane mode (RF function is disabled).

3.4. PSM

The module supports power saving mode (PSM). It enters the PSM by calling *ql_psm_sleep_enable()* and *ql_autosleep_enable()* when working normally. Pulling up PSM_EINT pin externally or setting the timer by software will enable the module to exit PSM.

Table 8: Pin Definition of PSM Interface

Pin Name	Pin No.	I/O	Description	Comment
PSM_EINT	96	DI	External interrupt, wakes up the module from PSM	Wakes up the module from PSM when being pulled high externally. If unused, keep it open.
PSM_IND*	1	DO	Indicates the module's power saving mode	If unused, keep it open.

NOTE

See ***document [5]*** for details on *ql_psm_sleep_enable().*

3.5. Power Supply

3.5.1. Power Supply Pins

The module provides four VBAT pins for connection with an external power supply.

- Two VBAT_RF pins for RF part.
- Two VBAT_BB pins for BB part.

Table 9: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	3.3	3.8	4.3	V
VBAT_RF	52, 53		Power supply for the module's RF part				V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102						

3.5.2. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of at least 3.0 A when the GSM or both GSM and LTE are available, and provide sufficient current of at least 2.0 A when only LTE is available. If the voltage drop between input and output is not too high, it is suggested that an LDO should be used. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure illustrates a reference design for 5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

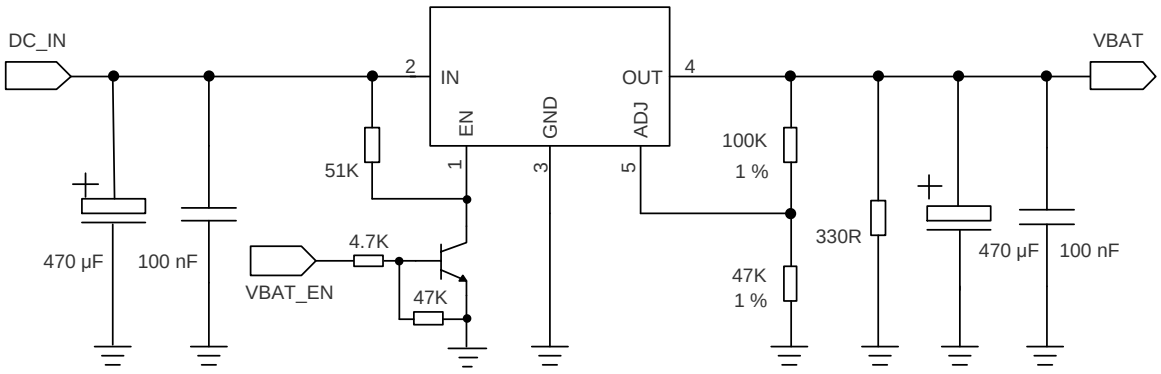


Figure 6: Reference Design of Power Supply

3.5.3. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure the input voltage never drops below 3.3 V.

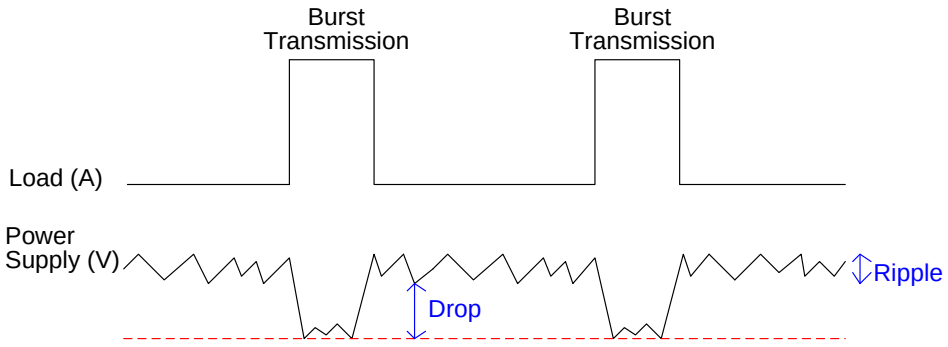


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a filter capacitor of about 100 µF with low ESR (ESR ≤ 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application should be a single voltage source and can be expanded to two sub paths with the star configuration. The width of VBAT_BB trace should be at least 2 mm; and the width of VBAT_RF trace should be at least 2.5 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. The reference circuit is shown as below.

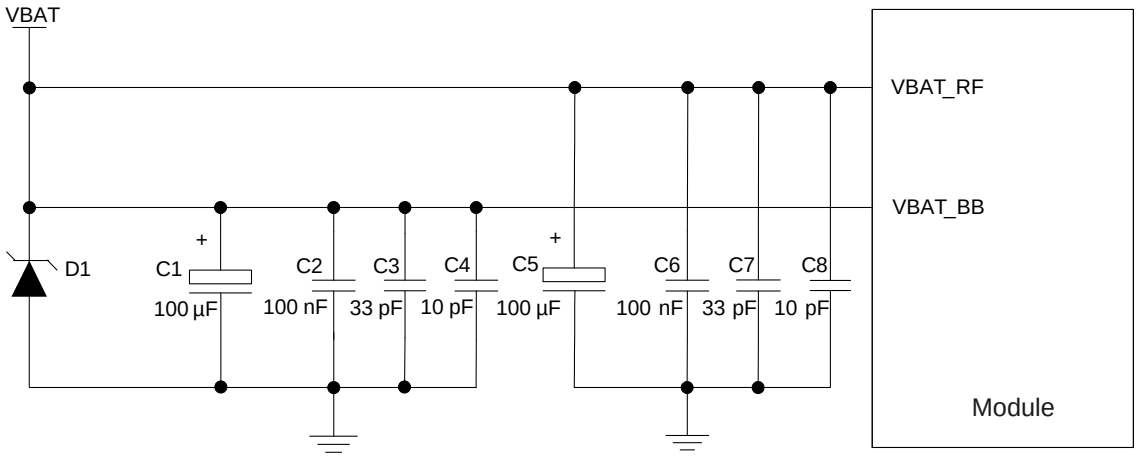


Figure 8: Reference Design of Power Supply

3.6. Turn On

3.6.1. Turn On with PWPKEY

Table 10: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	VBAT power domain. Active low. It is recommended to reserve a test point.

When the module is in power down mode, driving the PWRKEY pin low for at least 2 s can turn on the module. It is recommended to use an open drain/collector driver to control the PWRKEY.

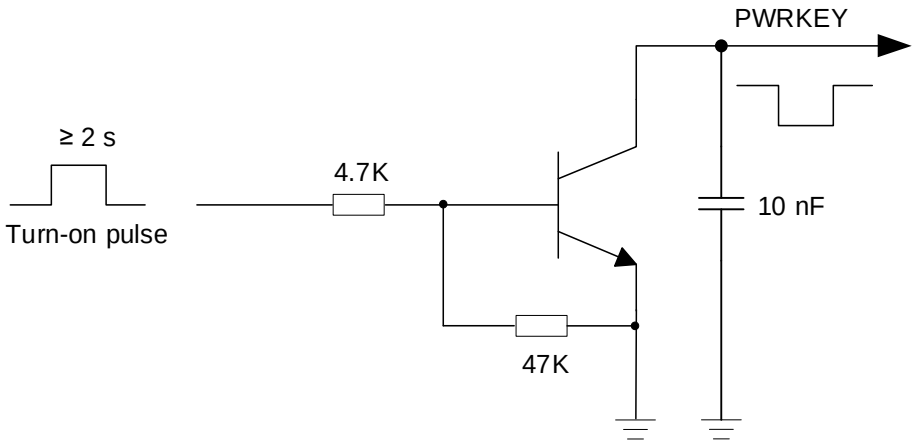


Figure 9: Turn On Module Using Driving PWRKEY

Another way to control the PWRKEY is using a button directly. When you are pressing the button, electrostatic strike may be generated from finger. Therefore, you must place a TVS nearby the button for ESD protection. A reference circuit is shown in the following figure.

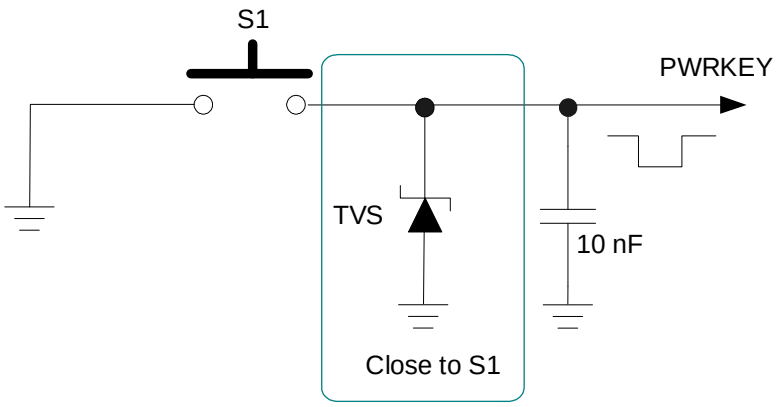


Figure 10: Turn On Module Using Button

If you need the automatic turn-on function, pull the PWRKEY down to the ground. The resistance is recommended to be less than 1 kΩ, but ensure that the VBAT voltage is lower than 0.5 V before power-on.

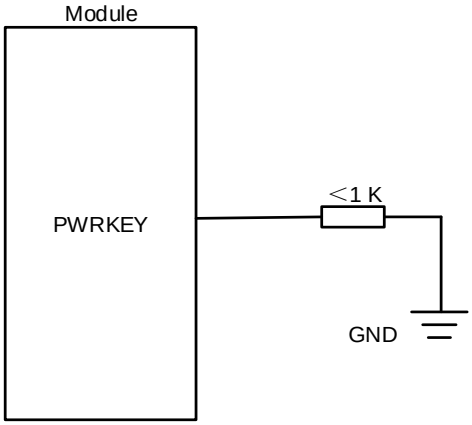


Figure 11: Turn On Module Automatically

The turn-on timing is illustrated in the following figure.

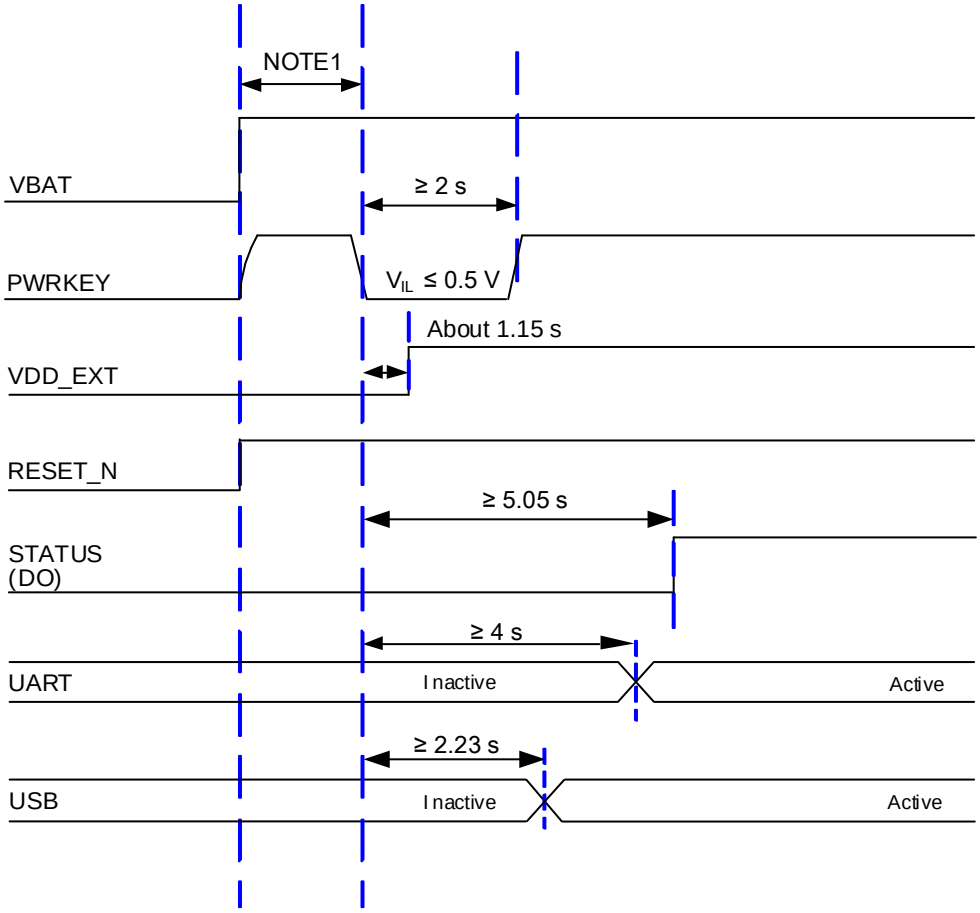


Figure 12: Turn-on Timing

NOTE

1. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. When pulling down PWRKEY to GND by using a resistor, the module will not boot automatically after being turned off with the API. In this case, it is necessary to forcibly disconnect the VBAT power supply and turn on the module again. Therefore, it is recommended to use a control circuit to control PWRKEY to turn on/off the module instead of keeping the PWRKEY connected to GND.
3. Pay special attention to the following two power-on scenarios:
   - In the scenario where USB_VBUS is connected first (or has always been connected), VBAT is powered on later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that VBAT is powered on stably for at least 2 s before PERKEY is pulled down;
   - In the scenario where VBAT is powered on first (or has always been powered on), USB_VBUS is connected later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that USB_VBUS is connected for at least 2 s before PWRKEY is pulled down.
4. Ensure that the VBAT voltage is lower than 0.5 V before power-on.

3.7. Turn Off

Both the following methods can be used to turn off the module:

- Use the PWRKEY pin.
- Use *ql_power_down()*. For more details about the API function, see ***document [6]***.

3.7.1. Turn Off with PWPKEY

Drive the PWRKEY pin low for at least 3 s and then release PWRKEY, and the module executes power-down procedure. The turn-off timing is illustrated in the following figure.

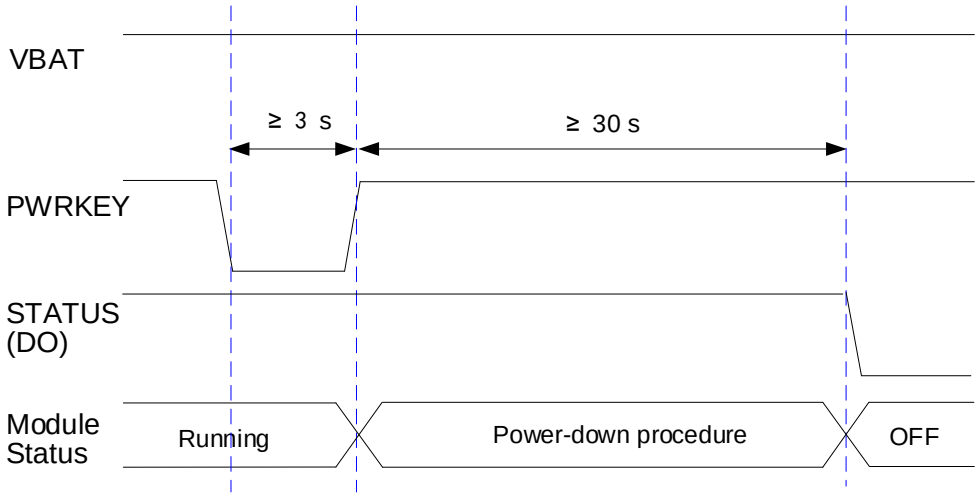


Figure 13: Turn-off Timing

3.7.2. Turn Off with ql_power_down()

It is also a safe way to use *ql_power_down()* to turn off the module, which is similar to turning off the module via the PWRKEY pin.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or API function can you cut off the power supply.
2. During the shutdown, the module will log out of the network. The time for logging out relates to its network status. Thus, pay attention to the shutdown time in your design because the actual shutdown time varies according to the network status.

3.8. Reset

The RESET_N pin can be used to reset the module. The module can be reset by driving the RESET_N pin low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Resets the module	VBAT power domain. Active low. A test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or a button can be used to control the RESET_N.

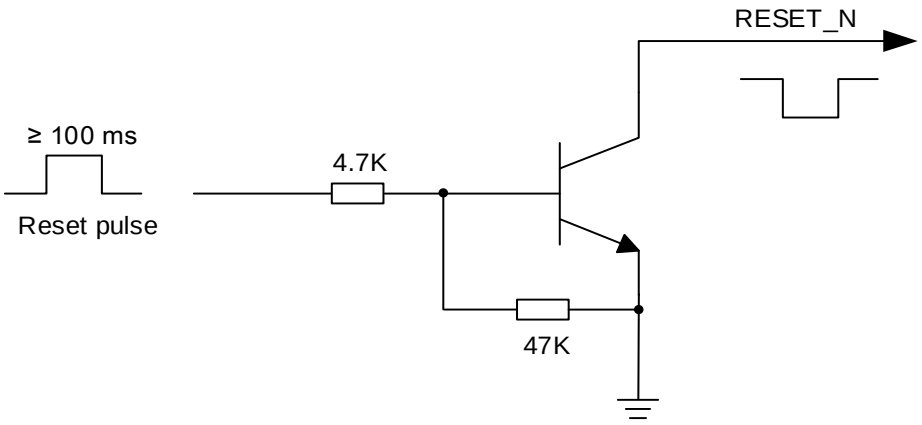


Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

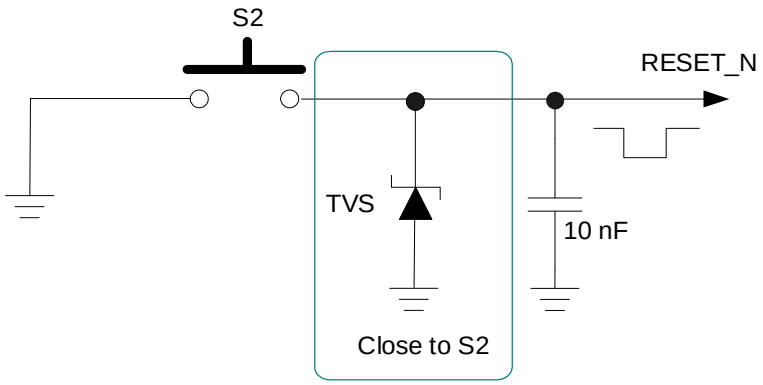


Figure 15: Reference Circuit of RESET_N by Using Button

The reset timing is illustrated in the following figure.

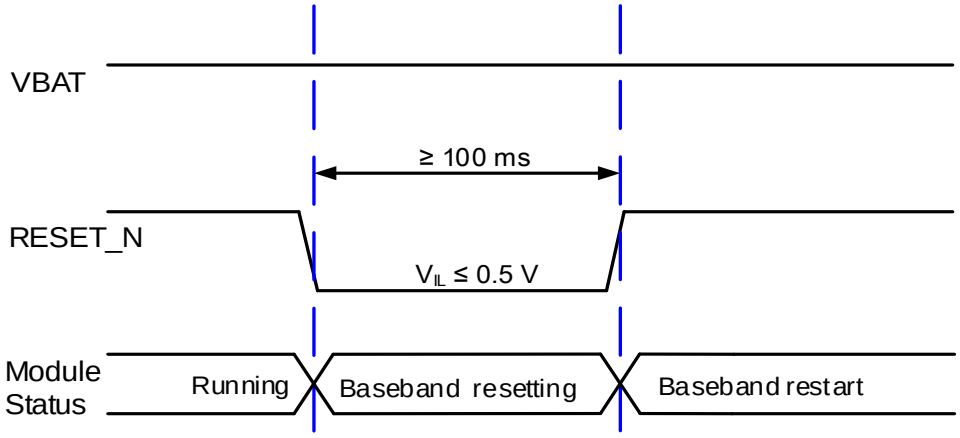


Figure 16: Reset Timing

NOTE

1. Ensure the capacitance on PWRKEY and RESET_N does not exceed 10 nF.
2. Use RESET_N only when you fail to turn off the module with *ql_power_down()* and PWRKEY.

4 Application Interfaces

4.1. USB Interface

The module provides an integrated Universal Serial Bus (USB) interface, which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve as a slave device.

The USB interface can be used for data transmission, software debugging and firmware upgrade.

Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Input voltage range: 3.5 V–5.25 V. A test point must be reserved.
USB_DP	9	AIO	USB differential data (+)	USB 2.0 compliant. Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	10	AIO	USB differential data (-)	

Test points must be reserved for debugging and it is recommended to use USB interface for firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

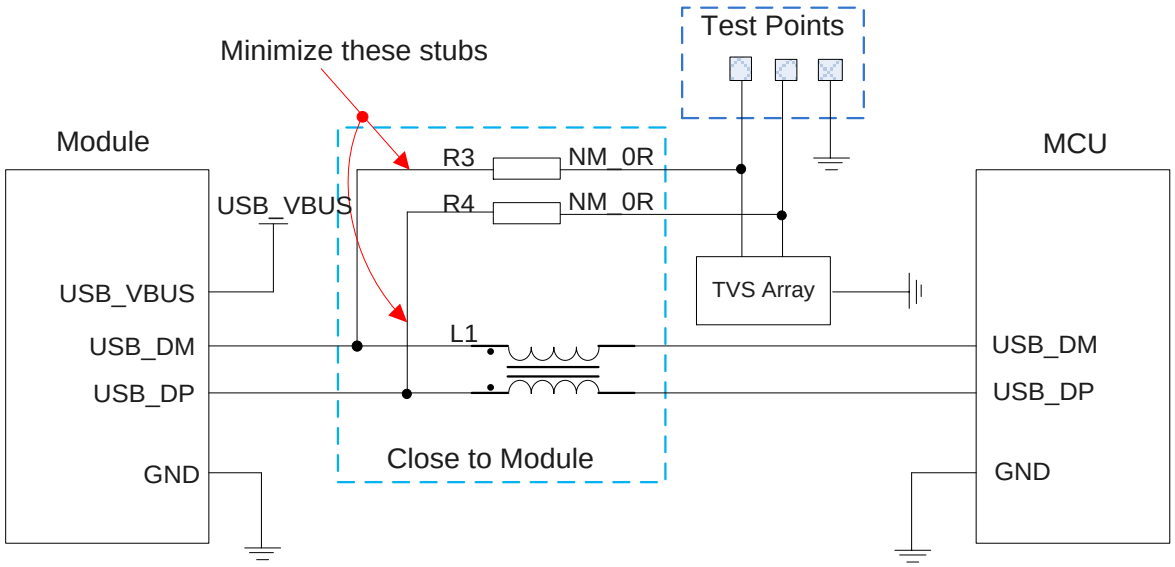


Figure 17: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure the signal integrity of USB data traces, L1, R3, and R4 must be placed close to the module, and resistors R3 and R4 should be placed close to each other. The extra stubs of traces must be as short as possible.

When designing the USB interface, you should follow the following principles to meet USB 2.0 specification.

- Route the USB signal traces as differential pairs in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. The impedance of USB differential traces is 90 Ω.
- Do not route signal traces under or near crystals, oscillators, magnetic devices, and RF signal traces.
- Pay attention to the selection of the TVS array on the USB data traces. Its stray capacitance should not exceed 2 pF and should be placed as close as possible to the USB connector.

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

4.2. USB_BOOT

The module provides a USB_BOOT interface. Pull up USB_BOOT to VDD_EXT before turning on the module, and then the module will enter the emergency download mode. In this mode, the module supports firmware upgrade over USB interface.

Table 13: Pin Definition of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module into emergency download mode	1.8 V power domain. Active high. A circuit that can set the module into emergency download mode should be reserved during design. It is recommended to reserve a test point.

The following figure shows a reference circuit of USB_BOOT.

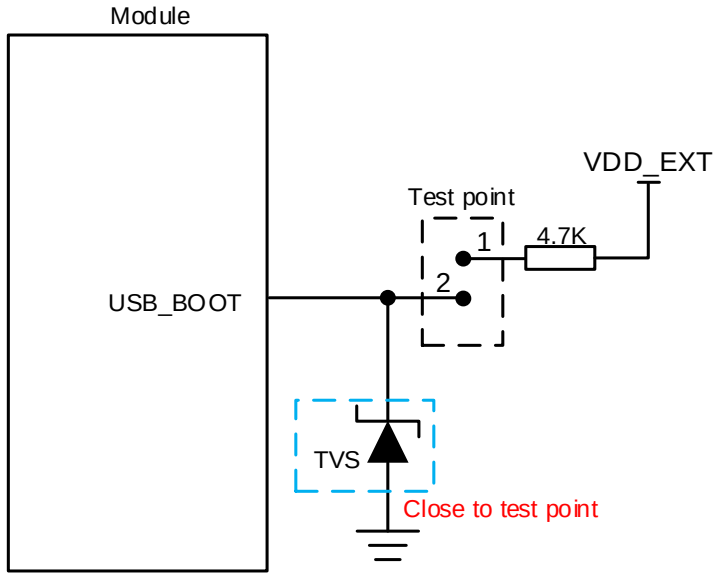


Figure 18: Reference Circuit of USB_BOOT

4.3. (U)SIM Interfaces

The module provides two (U)SIM interfaces that support Dual SIM Single Standby. The (U)SIM interfaces meet ETSI requirement and IMT-2000 specification. Either 1.8 V or 3.0 V (U)SIM card is supported.

Table 14: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.

USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM1_GND	47	-	Specified ground for (U)SIM1	
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA	86	DIO	(U)SIM2 card data	
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. A test point must be reserved for debugging.

The module supports (U)SIM card hot-plug via the USIM_DET pin and both high- and low-level detections are supported. See ***document [7]*** for details on configuring the hot-plug detection function.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

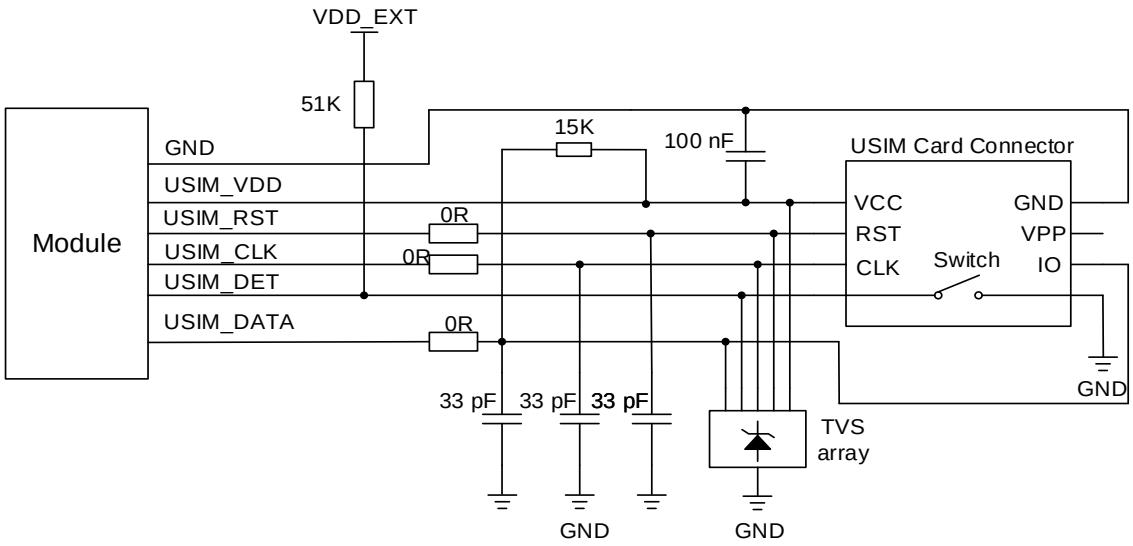


Figure 19: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

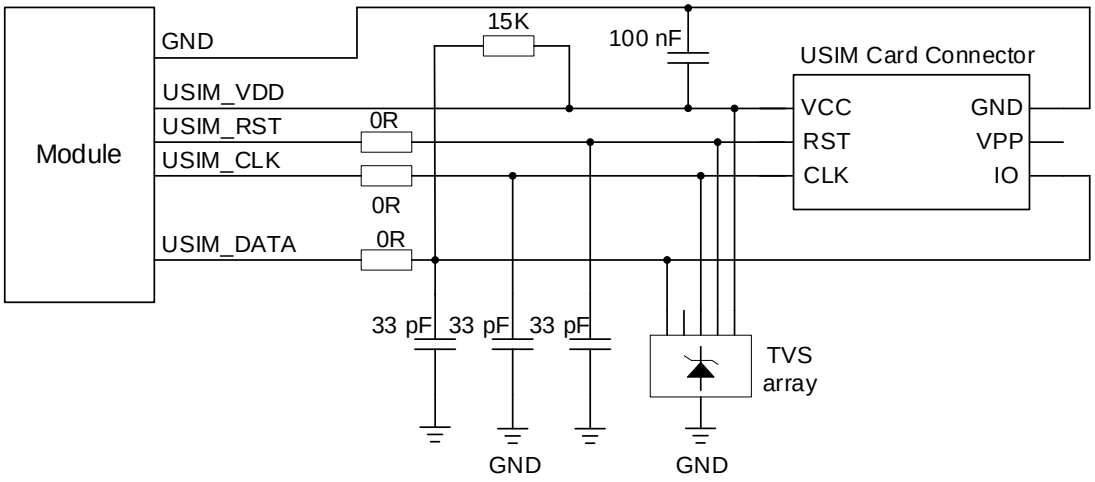


Figure 20: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Place (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- Ensure the bypass capacitor between USIM_VDD and GND is less than 1 μF, and the capacitor should be close to the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering RF interference. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

4.4. UART

The module provides three UART interfaces: main UART, debug UART, and auxiliary UART. Their features are described as follows.

- Main UART: supports baud rates 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, and 921600 bps, and the default is 115200 bps. It supports RTS and CTS hardware flow control. This interface is used for data transmission.
- Debug UART: supports 921600 bps baud rate only. It is used for log output and Linux console. It can only be used as a debugging UART and cannot be used as a general UART.
- Auxiliary UART: the baud rate is the same as that of the main UART.

Table 15: Pin Definition of Main UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	36	DO	Clear to send signal from the module	Connect to MCU's CTS. 1.8 V power domain. If unused, keep it open.
MAIN_RTS	37	DI	Request to send signal to the module	Connect to MCU's RTS. 1.8 V power domain. If unused, keep it open.
MAIN_RXD	34	DI	Main UART receive	1.8 V power domain. If unused, keep them open.
MAIN_TXD	35	DO	Main UART transmit	

Table 16: Pin Definition of Debug UART

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain. Test points must be reserved for debugging.
DBG_TXD	23	DO	Debug UART transmit	

Table 17: Pin Definition of Auxiliary UART

Pin Name	Pin No.	I/O	Description	Comment
AUX_TXD	27	DO	Auxiliary UART transmit	1.8 V power domain. If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive	

The module provides 1.8 V UART interfaces. Use a level-shifting circuit if the application is equipped with a 3.3 V UART interface.

A voltage-level translator TXS0104EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

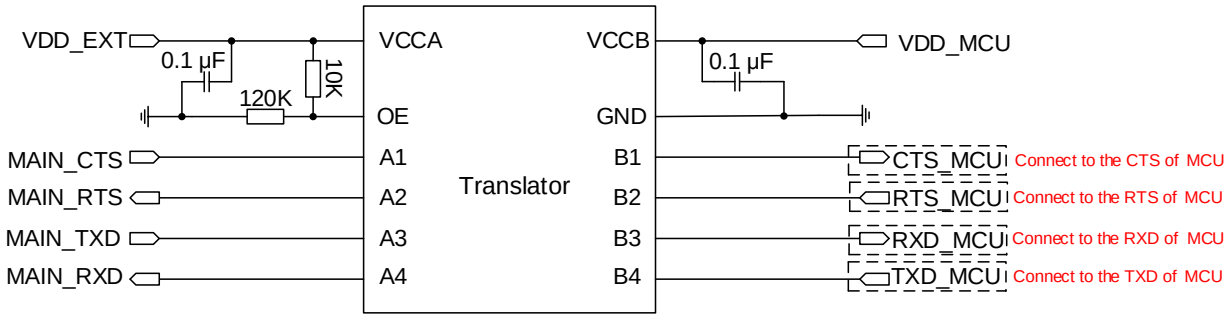


Figure 21: Reference Circuit with Voltage-level Translator

Visit http://www.ti.com for more information.

Another example with level-shifting circuit is shown as follows. For the design of circuits in dotted lines, please refer to that of the circuits in solid lines, but pay attention to the direction of connection.

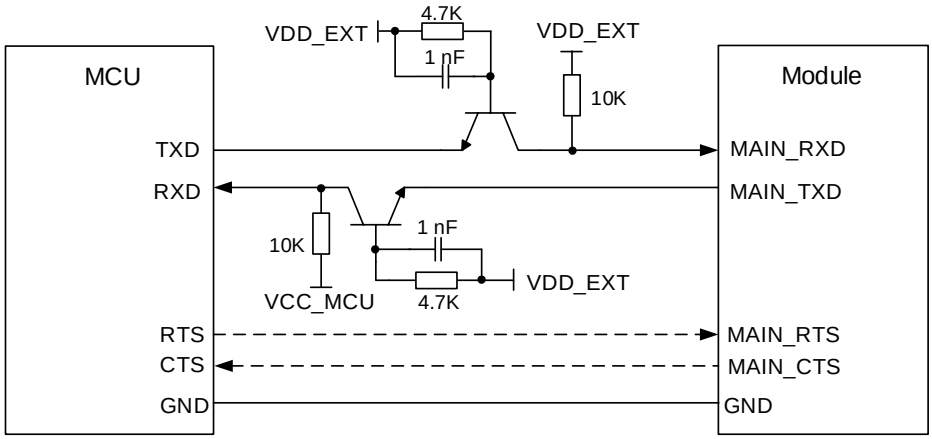


Figure 22: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

4.5. PCM and I2C Interfaces

The module provides one I2C interface and one pulse code modulation (PCM) interface. The PCM interface of the module only supports slave mode; The clock signal of the external codec IC needs to be provided externally.

PCM interface supports the short frame mode and the module can be used as the slave mode only. In short frame mode, PCM_CLK = the number of channels × PCM_SYNC × 16 bit, where the number of channels supports 1–4 channels, but the module will only take the data on the first channel; PCM_SYNC is equal to the audio sampling rate, which supports 8–44.1 kHz.

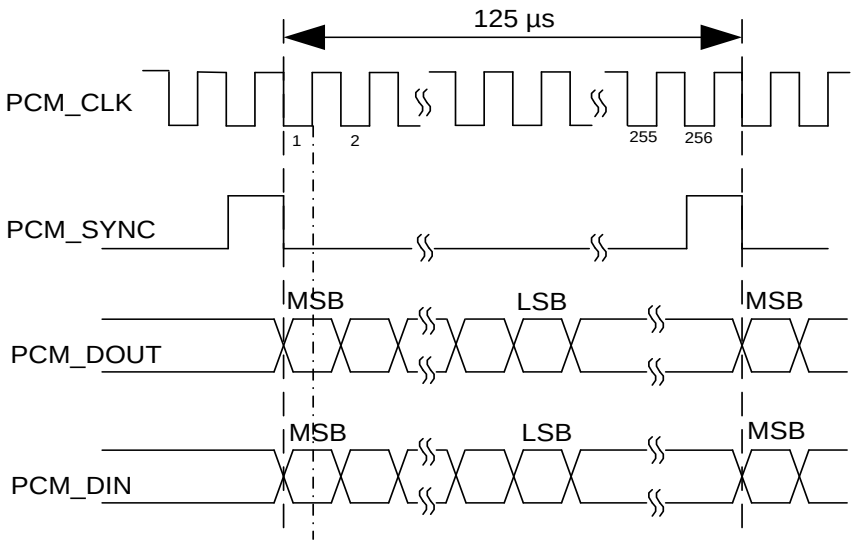


Figure 23: Timing of PCM Mode

NOTE

The clocks of PCM_SYNC and PCM_CLK are provided by the external codec IC, but the provided PCM_SYNC frequency must be equal to the sampling frequency of the audio file played by the module.

Table 18: Pin Definition of I2C and PCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	40	OD	I2C serial clock	External 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data	
PCM_DIN	6	DI	PCM data input	1.8 V power domain.

PCM_DOUT	7	DO	PCM data output	If unused, keep them open. Supports slave mode only.
PCM_SYNC	5	DI	PCM data frame sync	
PCM_CLK	4	DI	PCM clock	

The following figure shows a reference design of I2C and PCM interfaces with an external codec IC.

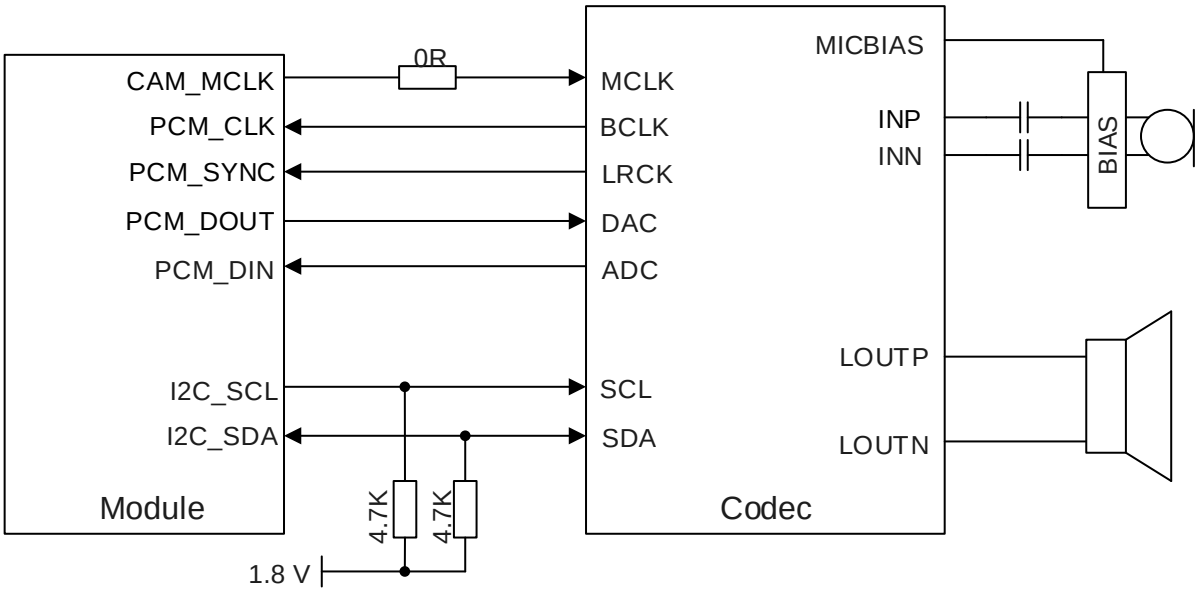


Figure 24: Reference Circuit of I2C and PCM Application with Audio Codec

NOTE

1. It is recommended to reserve a termination resistor and a filter capacitor on the PCM traces (especially on the CAM_MCLK and PCM_CLK traces).
2. The I2C interface supports simultaneous connection of multiple peripherals except for codec IC. In other words, if a codec IC has been mounted on the I2C bus, no other peripherals can be mounted; if there is no codec IC on the bus, multiple peripherals can be mounted.

4.6. Analog Audio Interfaces

The module provides one analog audio input channel and two analog audio output channels. The pin definition is shown in the following table.

Table 19: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC_N	119	AI	Microphone analog input (-)	If unused, keep them open.
MICBIAS	120	PO	Bias voltage output for microphone	
SPK_P	121	AO	Analog audio differential output (+)	If unused, keep them open.
SPK_N	122	AO	Analog audio differential output (-)	
MIC_P	126	AI	Microphone analog input (+)	If unused, keep them open.
HP_L	123	AO	Headphone left channel output	
HP_R	124	AO	Headphone right channel output	
HP_DET	125	DI	Headphone hot-plug detect	

- AI channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- AO channels are differential output channels. SPK_P/_N can be applied for output of handset, earpiece and loudspeaker. HP_L/_R can be applied for the output of headphone. (The module has no built-in PA, the analog audio output SPK_P/_N can be directly used as earpiece, and if connected with external PA, it can be used as loudspeaker.)

4.6.1. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure.

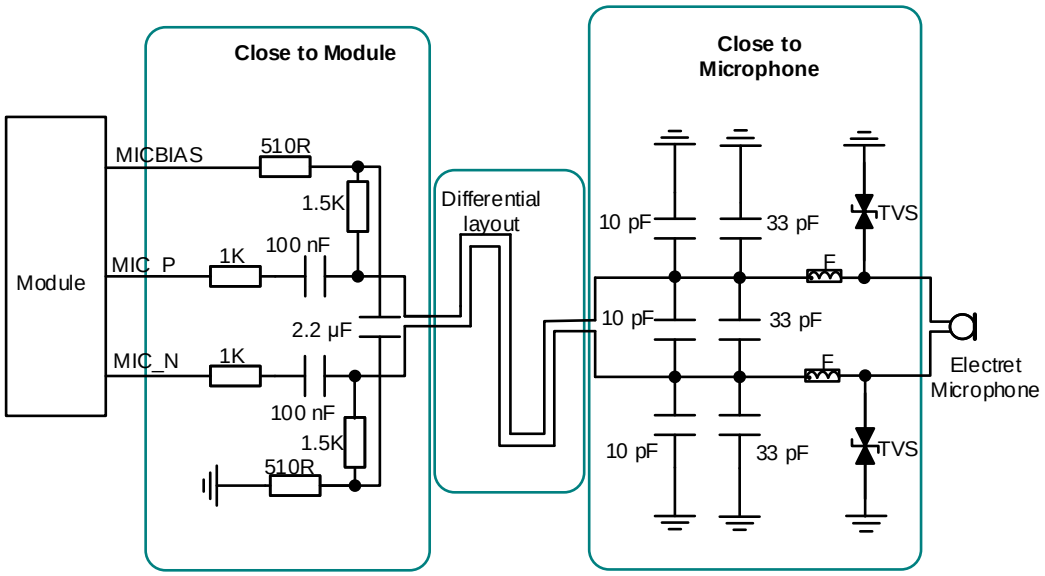


Figure 25: Reference Design for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD protection components used for protecting the MIC.

4.6.2. Earpiece Interface Design

The earpiece channel reference circuit is shown in the following figure:

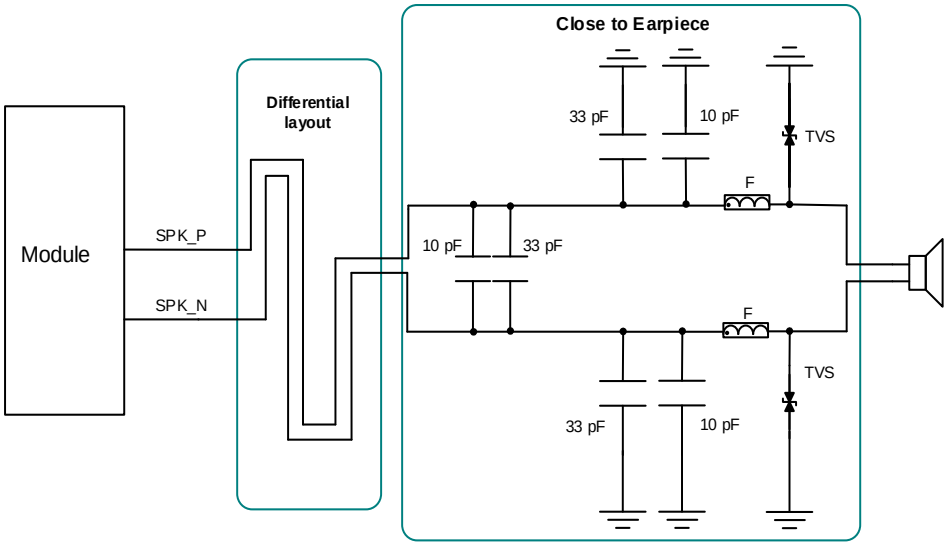


Figure 26: Reference Design for Earpiece Interface

4.6.3. Headphone Interface Design

The headphone channel reference circuit is shown in the following figure:

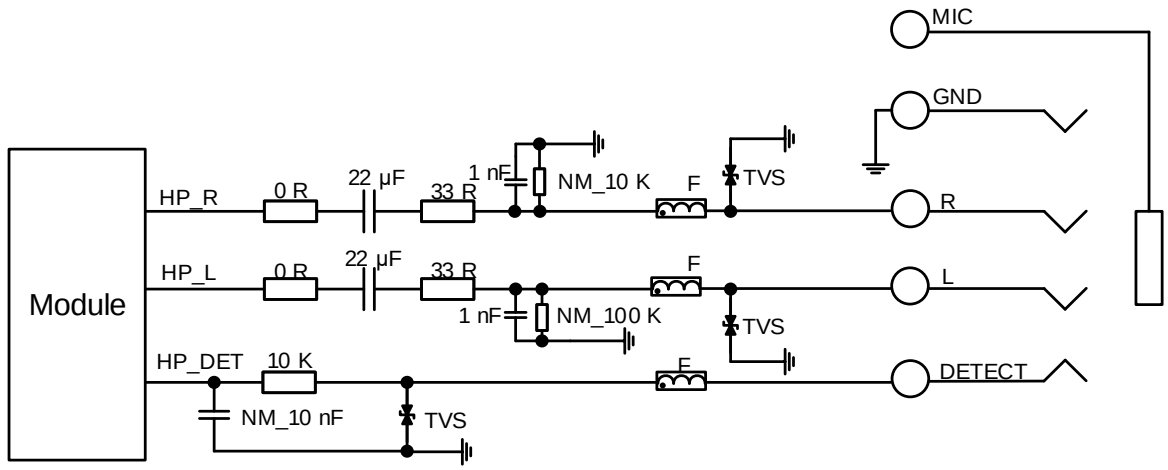


Figure 27: Reference Design for Headphone Interface

4.6.4. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. Without these capacitors, TDD noise could be heard during the call. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor to filter out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required. The filter capacitor on the PCB should be placed near the audio devices or audio interfaces as close as possible, and the trace should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To decrease signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.7. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. To improve the measurement accuracy of ADC, surround the traces of ADC with ground.

Table 20: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interfaces	It is recommended to reserve a voltage divider circuit. If unused, keep them open.
ADC1	2			

Table 21: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC[0:1] Voltage Range	0	-	VBAT	V
ADC Resolution	-	12	-	bits

You can use *ql_adc_get_volt()* to read the voltage of ADC interfaces. See ***document [8]*** for details. The mapping between *ql_adc_channel_id* and ADC channels is as follows:

Table 22: Mapping Between *q_adc_channel_id* and ADC channel

ql_adc_channel_id	ADC Channel
QL_ADC0_CHANNEL	ADC0
QL_ADC1_CHANNEL	ADC1

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC interface when the module is not powered by the VBAT.
3. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins, it is strongly recommended to reserve the voltage divider circuit for better compatibility with other Quectel modules. The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced. When the divider

circuit is not used, the ADC pins require 1 kΩ resistors in series.

4.8. SPI

The module provides one SPI that only supports master mode. The voltage domain is 1.8 V. The maximum clock frequency is 25 MHz.

Table 23: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	1.8 V power domain. If unused, keep them open. Supports master mode only.
SPI_CS	25	DO	SPI chip select	
SPI_DIN	88	DI	SPI data input	
SPI_DOUT	64	DO	SPI data output	

NOTE

1. When the general 4-wire SPI interface is used for connecting external NOR flash, it supports basic flash operations such as read, write and erase, file systems, wear leveling, FOTA upgrade and preset files. It can be used only for storage purpose and cannot be used to run code.
2. When the general 4-wire SPI interface is used for connecting external NAND flash, it supports basic flash operations such as read, write and erase, file systems and wear leveling. It does not support FOTA upgrade and preset files. it can be used only for storage purpose and cannot be used to run code.

4.9. External Flash Interface

The module supports connection to an external flash chip, and the external flash interface is multiplexed from other pins. Pin assignments are described in the figure below.

Table 24: Multiplexing Function Definition of External Flash Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description
PCM_DIN	6	SPI_FLASH1_SIO_0	DIO	External flash data bit 0
PCM_DOUT	7	SPI_FLASH1_SIO_1	DIO	External flash data bit 1
PCM_SYNC	5	SPI_FLASH1_CS	DO	External flash chip select
PCM_CLK	4	SPI_FLASH1_CLK	DO	External flash clock
PSM_IND	1	SPI_FLASH1_SIO_2	DIO	External flash data bit 2
STATUS	20	SPI_FLASH1_SIO_3	DIO	External flash data bit 3

Pins 4–7, 1, 20 can be multiplexed into a dedicated SPI interface for connecting external 6-wire NOR flash or NAND flash.

- When the dedicated SPI interface is used for connecting external NOR flash, it supports file system, wear leveling, FOTA upgrade and preset files. It can be used only for storage purpose and cannot be used to run code.
- When the dedicated SPI interface is used for connecting external NAND flash, it supports basic flash operations such as read, write and erase, file systems and wear leveling. It does not support FOTA upgrade and preset files. it can be used only for storage purpose and cannot be used to run code.

See ***document [9]*** for the design details of the two interface circuits.

NOTE

1. Pins 4–7 can also be multiplexed into a general SPI interface for connecting external 4-wire flash and other peripherals.
2. See ***document [1]*** for details about pin multiplexing of the module.

4.10. LCM Interface

The LCM interface of the module supports the LCD display with a maximum resolution of 320 × 240 pixel, DMA transmission, as well as 16-bit RGB565 and YUV formats.

Table 25: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_TE	92	DI	LCD tearing effect	1.8 V power domain. If unused, keep them open.
LCD_RST	107	DO	LCD reset	
LCD_SEL	108	DO	Reserved	
LCD_SPI_CS	16	DO	LCD chip select	
LCD_SPI_CLK	105	DO	LCD clock	
LCD_SPI_RS	106	DO	LCD register select	
LCD_SPI_DOUT	116	DIO	LCD data	
LCD_ISINK	109	PI	Sink current input. Backlight adjustment.	It is driven by the current sink method and connected to the backlight cathode; the brightness can be adjusted with current control.

NOTE

1. The recommended value of LCD digital power LCD_VDDIO should be designed as Vnom = 1.8 V @ 200 mA.
2. The recommended value of LCD analog power LCD_AVDD should be designed as Vnom = 2.8 V @ 200 mA.

4.11. SD Card Interface

The module provides an SD card interface compliant with SD 2.0 specification and its partial pins can be multiplexed from other pins.

Table 26: Multiplexing Function Definition of SD Card Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
W_DISABLE#	18	SDIO1_DATA2	DIO	SDIO1 data bit 2	3.2 V power domain. If unused, keep them open.
AP_READY	19	SDIO1_DATA3	DIO	SDIO1 data bit 3	

MAIN_DTR	30	SDIO1_DATA0	DIO	SDIO1 data bit 0	
MAIN_DCD	38	SDIO1_CMD	DIO	SD card command	
MAIN_RI	39	SDIO1_DATA1	DIO	SDIO1 data bit 1	
SDIO1_CLK	110	-	DO	SD card clock	
SD_DET	104	-	DI	SD card hot-plug detect	1.8 V power domain. If unused, keep it open.

The reference design circuit is shown in the figure below.

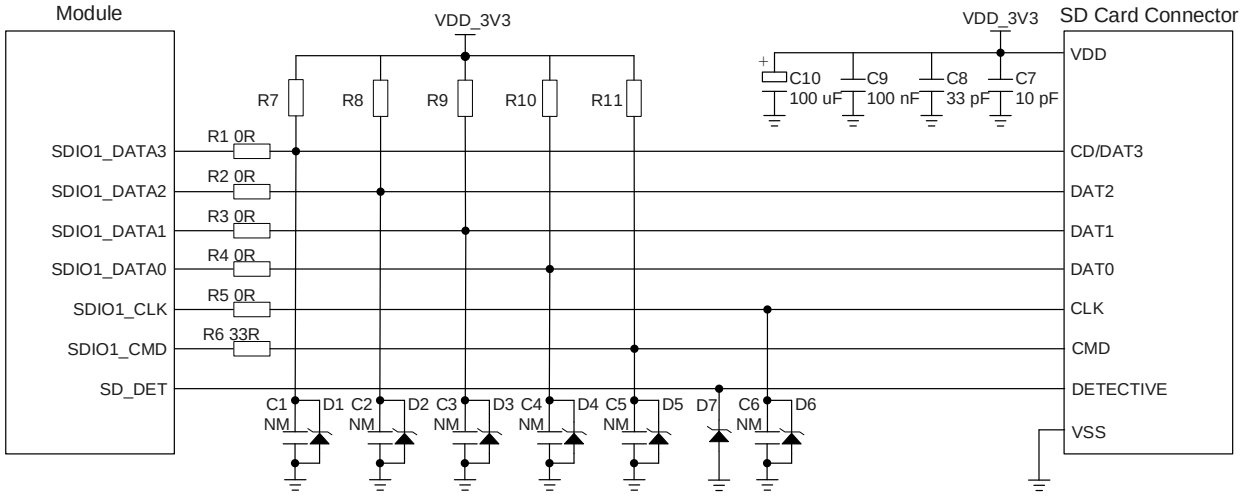


Figure 28: SD Card Interface Reference Design

To ensure good performance and reliability of the SD card, the following principles are recommended in the circuit design of the SD card interface.

- SD card needs to be powered externally. The voltage range of VDD_3V3 is 2.7–3.6 V and it should provide at least 800 mA current. The recommended nominal value of VDD_3V3 is 3.2 V.
- To avoid the jitter of bus, it is necessary to reserve pull-up resistors R7–R11 on the SDIO signal traces. The recommended value is 4.7 kΩ and they are not mounted by default. The pull-up power supply can be the external power supply VDD_3V3 whose voltage is 3.2 V.
- To adjust signal quality, it is necessary to add resistors R1–R6 in series between the module and the SD card connector. The recommended value for R1–R5 is 0 Ω, and for R6 is 33 Ω. The bypass capacitors C1–C6 are reserved and not mounted by default. The resistors and capacitors should be placed close to the module when placing the PCB.
- For good ESD protection, it is recommended to add a TVS on each SD card pin, and place them as close to the SD card connector as possible. The parasitic capacitance of TVS should be less than 15 pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noise signals such as clock and DC-DC signals.

- Route SDIO signals with ground surrounded. The impedance of SDIO data traces should be kept at 50 Ω ±10 %.
- Keep the space between SDIO signal traces and other signal traces greater than twice the trace width and ensure that the bus capacitance is less than 15 pF.
- Keep the trace length difference among SDIO1_CLK, SDIO1_DATA[0:3] and SDIO1_CMD less than 1 mm and the total routing length should be less than 50 mm.

4.12. Camera Interface

The module provides one camera interface supporting cameras up to 0.3 MP, and supports SPI two-data-line data transmission.

Table 27: Pin Definition of Camera Interface

Pin Name	Pin No.	I/O	Description	Comment
CAM_I2C_SCL	103	OD	I2C clock of camera	Pull each of them up to 1.8 V power domain with an external resistor. If unused, keep them open.
CAM_I2C_SDA	114	OD	I2C data of camera	
CAM_MCLK	95	DO	Master clock of camera	1.8 V power domain. If unused, keep them open.
CAM_SPI_CLK	78	DI	SPI clock of camera	
CAM_SPI_DATA0	97	DI	SPI data 0 of camera	
CAM_SPI_DATA1	98	DI	SPI data 1 of camera	
CAM_PWDN	115	DO	Power down of camera	
CAM_RST	111	DO	Reset of camera	
CAM_VDD	94	PO	Analog power supply of camera	Power supply of camera. If unused, keep them open.
CAM_VDDIO	93	PO	Digital power supply of camera	

NOTE

If the camera interface is not required, pins 103 and 114 can be used as an I2C interface to connect other peripherals.

4.13. Indication Signals

Table 28: Pin Definition of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicates the module's operation status	1.8 V power domain. If unused, keep them open.
NET_STATUS	21	DO	Indicates the module's network activity status	

4.13.1. NET_STATUS

The network indication pin NET_STATUS can drive the network status indicator. The following table describes its working states in different network status.

Table 29: Working States of Network Connection Status/Activity Indication

Pin Name	State	Network Status
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker quickly (234 ms high/266 ms low)	Registered on network and idle
	Flicker rapidly (63 ms high /62 ms low)	Data transmission is ongoing
	Always high	Voice calling

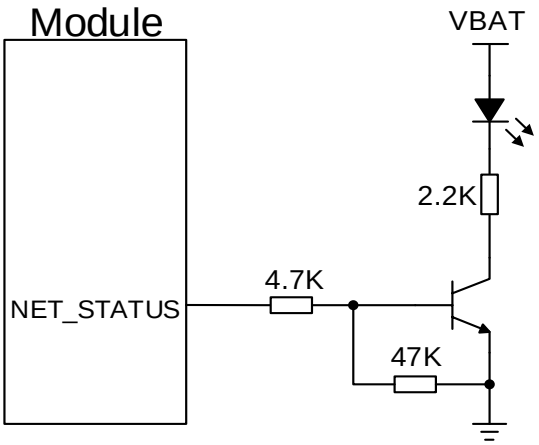


Figure 29: Reference Circuit of Network Status Indication

4.13.2. STATUS

The STATUS pin indicates the module's operation status. It will output high level when module is powered on successfully. A reference circuit is shown as below.

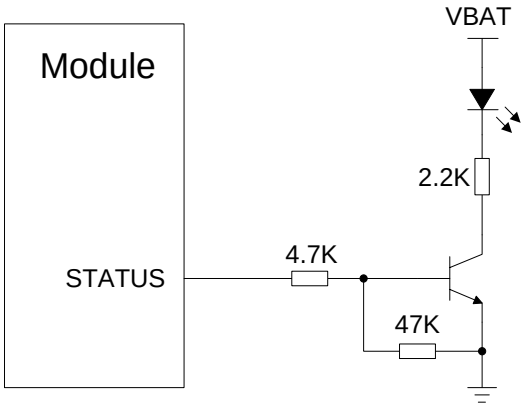


Figure 30: Reference Circuit of STATUS

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module provides a main antenna interface, a Bluetooth/Wi-Fi Scan antenna interface and a GNSS antenna interface. The antenna interfaces have an impedance of 50 Ω.

5.1. Main Antenna and Bluetooth/Wi-Fi Scan Antenna

5.1.1. Antenna Interface & Frequency Bands

Table 30: Pin Definition of Main and Bluetooth/Wi-Fi Scan Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω characteristic impedance.
ANT_BT/WIFI_SCAN	56	AIO/AI	Shared interface for Bluetooth and Wi-Fi Scan	Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan antenna can only receive but not transmit. 50 Ω characteristic impedance. If unused, keep it open.

NOTE

The module supports both Wi-Fi Scan and Bluetooth functions. However, as the antenna interface is shared, the two functions cannot be used simultaneously. Additionally, Bluetooth and Wi-Fi Scan functions are optional. For details, contact Quectel Technical Support.

Table 31: Operating Frequency (Unit: MHz)

Operating Frequency	Transmit	Receive
GSM850	824–849	869–894
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B12	699–716	729–746
LTE-FDD B13	777–787	746–756
LTE-FDD B17	704–716	734–746
LTE-FDD B18	815–830	860–875
LTE-FDD B19	830–845	875–890
LTE-FDD B20	832–862	791–821
LTE-FDD B25	1850–1915	1930–1995
LTE-FDD B26	814–850	859–894
LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710–1780	2110–2180
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620

LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2496–2690	2496–2690

5.1.2. Antenna Tuner Control Interfaces

The module can use GRFC (generic RF control) interfaces to control external antenna tuner.

Table 32: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	76	DO	Generic RF Controller	If unused, keep them open.
GRFC2	77	DO		

Table 33: Truth Table of GRFC Interfaces (Unit: MHz)

GRFC1 Level	GRFC2 Level	Frequency Range	Band
Low	Low	699–802.9	B12/B13/B17/B28
Low	High	814–893.9	● B5/B18/B19/B20/B26 ● GSM850
High	Low	880–959.9	● LTE B8 ● EGSM900
High	High	1710–2689.9	● B1/B2/B3/B4/B7/B25/B34/B38/ B39/B40/B41/B66 ● DCS1800/PCS1900

5.1.3. Tx Power

Table 34: RF Output Power

Frequency Band	Max. RF Output Power	Min. RF Output Power
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB

DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B2/B3/B4/B5/B7/B8/ B12/B13/B17/B18/B19/B20/B25/B26/B28/B66	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

5.1.4. Rx Sensitivity

Table 35: Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)	3GPP
	Primary	
GSM850	-108.6	-102.0
EGSM900	-108.4	-102.0
DCS1800	-108.1	-102.0
PCS1900	-108.3	-102.0
LTE-FDD B1 (10 MHz)	-98.2	-96.3
LTE-FDD B2 (10 MHz)	-98.9	-94.3
LTE-FDD B3 (10 MHz)	-99.0	-93.3
LTE-FDD B4 (10 MHz)	-98.2	-96.3
LTE-FDD B5 (10 MHz)	-99.3	-94.3
LTE-FDD B7 (10 MHz)	-96.3	-94.3
LTE-FDD B8 (10 MHz)	-99.2	-93.3
LTE-FDD B12 (10 MHz)	-98.0	-93.3
LTE-FDD B13 (10 MHz)	-99.1	-93.3
LTE-FDD B17 (10 MHz)	-97.5	-93.3
LTE-FDD B18 (10 MHz)	-99.0	-96.3
LTE-FDD B19 (10 MHz)	-99.5	-96.3

LTE-FDD B20 (10 MHz)	-98.9	-93.3
LTE-FDD B25 (10 MHz)	-98.3	-92.8
LTE-FDD B26 (10 MHz)	-98.9	-93.8
LTE-FDD B28 (10 MHz)	-99.4	-94.8
LTE-FDD B66 (10 MHz)	-98.1	-96.5
LTE-TDD B34 (10 MHz)	-99.0	-96.3
LTE-TDD B38 (10 MHz)	-99	-96.3
LTE-TDD B39 (10 MHz)	-99.7	-96.3
LTE-TDD B40 (10 MHz)	-99.2	-96.3
LTE-TDD B41 (10 MHz)	-98.6	-94.3

5.1.5. Reference Design

A reference design of ANT_MAIN and ANT_BT/WIFI_SCAN is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

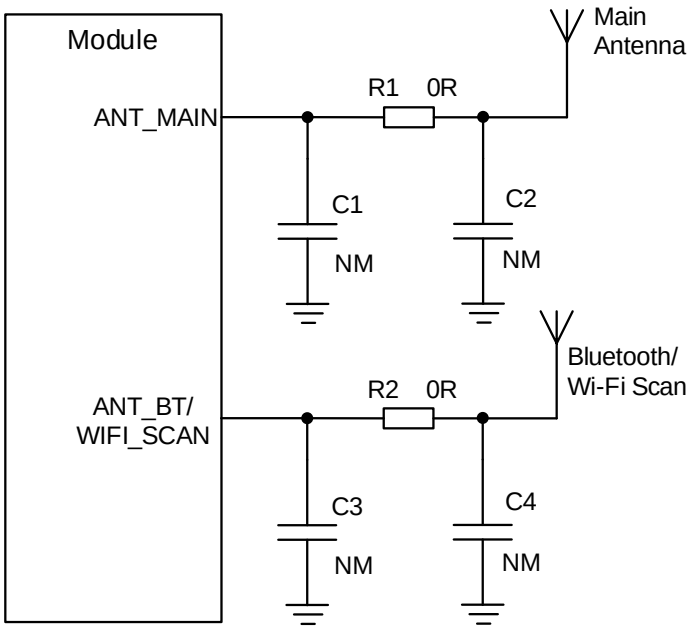


Figure 31: Reference Circuit of RF Antennas

NOTE

1. To improve receiver sensitivity, ensure that the clearance among antennas is appropriate.
2. Place the π-type matching components (R1, C1, C2 and R2, C3, C4) to antennas as close as possible.

5.2. GNSS (Optional)

GNSS information of the module is as follows:

- Supports GPS, GLONASS, BDS, Galileo, QZSS positioning system.
- Supports NMEA 0183 protocol and outputs NMEA sentences via USB interface (data update rate for positioning: 1 Hz).
- The module's GNSS function is OFF by default. It must be enabled via *ql_gnss_switch()*. See ***document [10]*** for details.

5.2.1. Antenna Interface & Frequency Bands

The following tables list the pin definition and frequency of the GNSS antenna interface respectively.

Table 36: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω characteristic impedance. If unused, keep it open.

Table 37: GNSS Frequency (Unit: MHz)

Type	Frequency
GPS	1575.42 ±1.023
GLONASS	1597.5–1605.8
Galileo	1575.42 ±2.046
BDS	1561.098 ±2.046
QZSS	1575.42 ±1.023

5.2.2. GNSS Performance

Table 38: GNSS Performance

Parameter	Description	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-145	dBm
	Reacquisition		-160	
	Tracking		-159	
TTFF	Cold start @ open sky	Autonomous	28	s
	Warm start @ open sky	Autonomous	28	
	Hot start @ open sky	Autonomous	4	
Accuracy	CEP-50	Autonomous @ open sky	2.5	m

.

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

A reference design of GNSS antenna is shown as below:

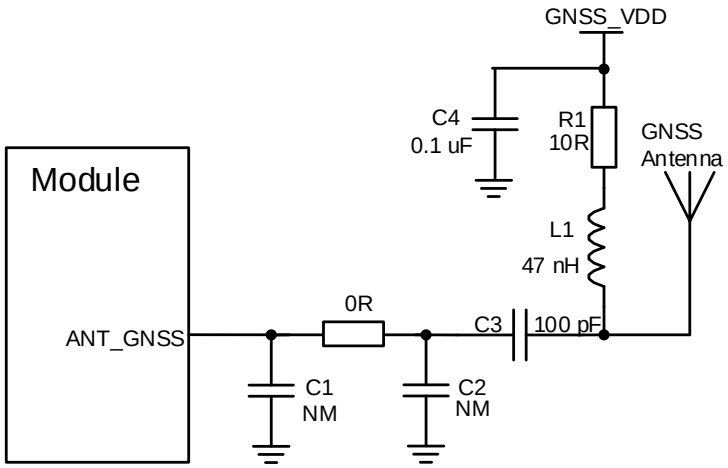


Figure 32: Reference Circuit of GNSS Antenna

NOTE

1. An external LDO can be selected to supply power GNSS_VDD according to the active antenna requirement. The supply power GNSS_VDD is recommended 3.3 V @ 30 mA.
2. The GNSS_VDD circuit (C4, R1, L1) is not needed if you select a passive antenna.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

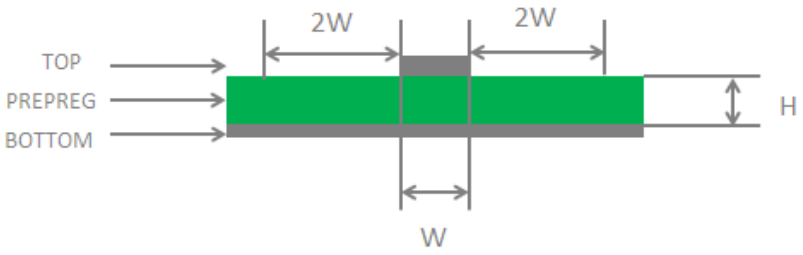


Figure 33: Microstrip Design on a 2-layer PCB

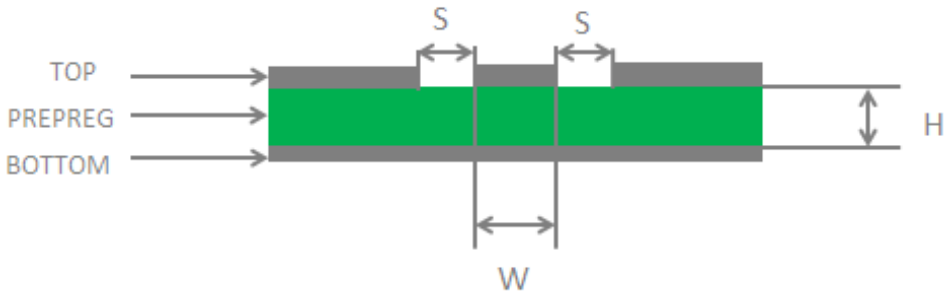


Figure 34: Coplanar Waveguide Design on a 2-layer PCB

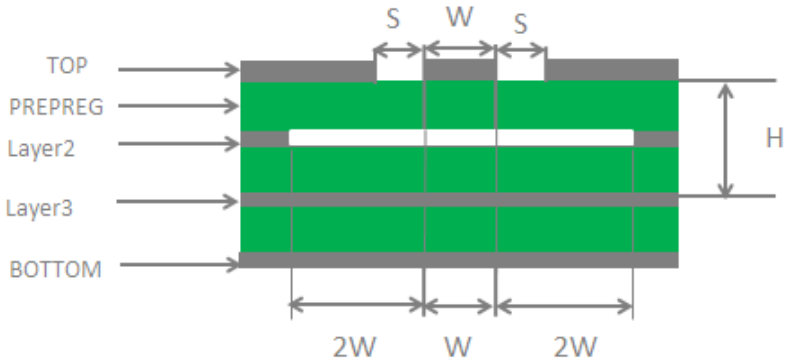


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

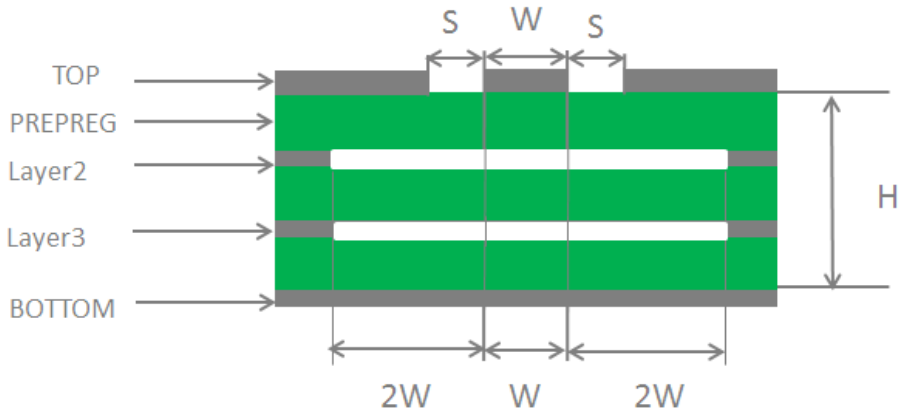


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [11]***.

5.4. Requirements for Antenna Design

Table 39: Requirements for Antenna Design

Type	Requirement
GNSS (Optional)	Frequency range: 1559–1609 MHz RHCP or linear polarization VSWR: ≤ 2 (Typ.) Isolation from main antenna: > 40 dB
	For passive antenna usage: Passive antenna gain: > 0 dBi
	For active antenna usage: Active antenna noise coefficient: < 1.5 dB Active antenna gain: > 0 dBi Active antenna embedded LNA gain: < 17 dB
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max. input power: 50 W Input impedance: 50 Ω Cable insertion loss: < **1 dB:** LB (< 1 GHz) < **1.5 dB:** MB (1–2.3 GHz) < **2 dB:** HB (> 2.3 GHz)

5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

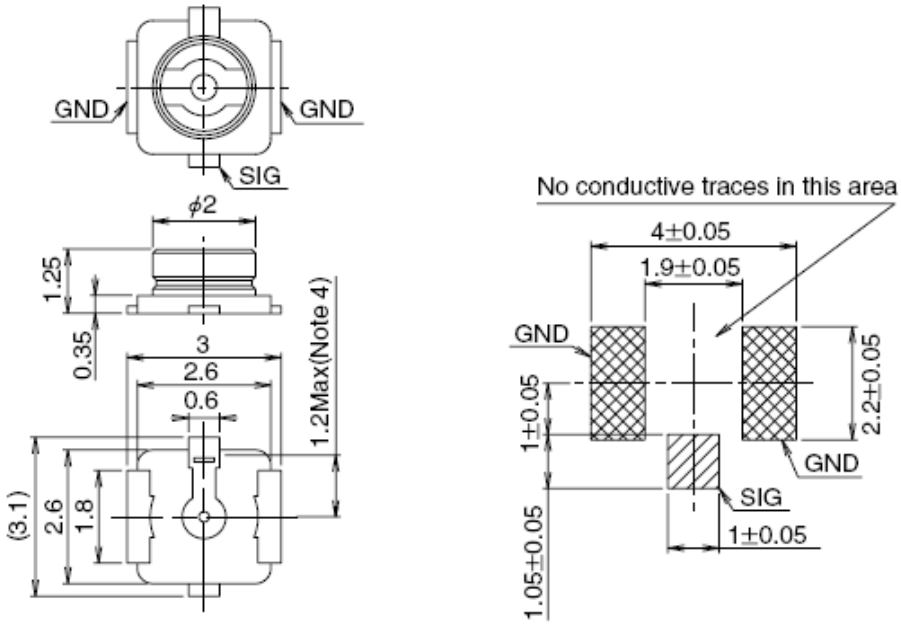


Figure 37: Dimensions of Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

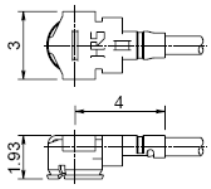
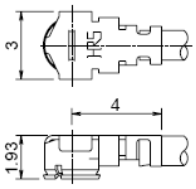
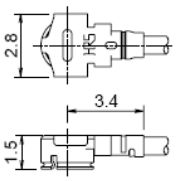
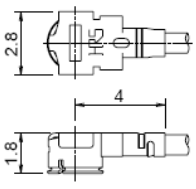
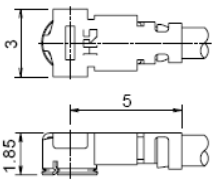
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 38: Specifications of Mated Plugs

The following figure describes the space factor of mated connector.

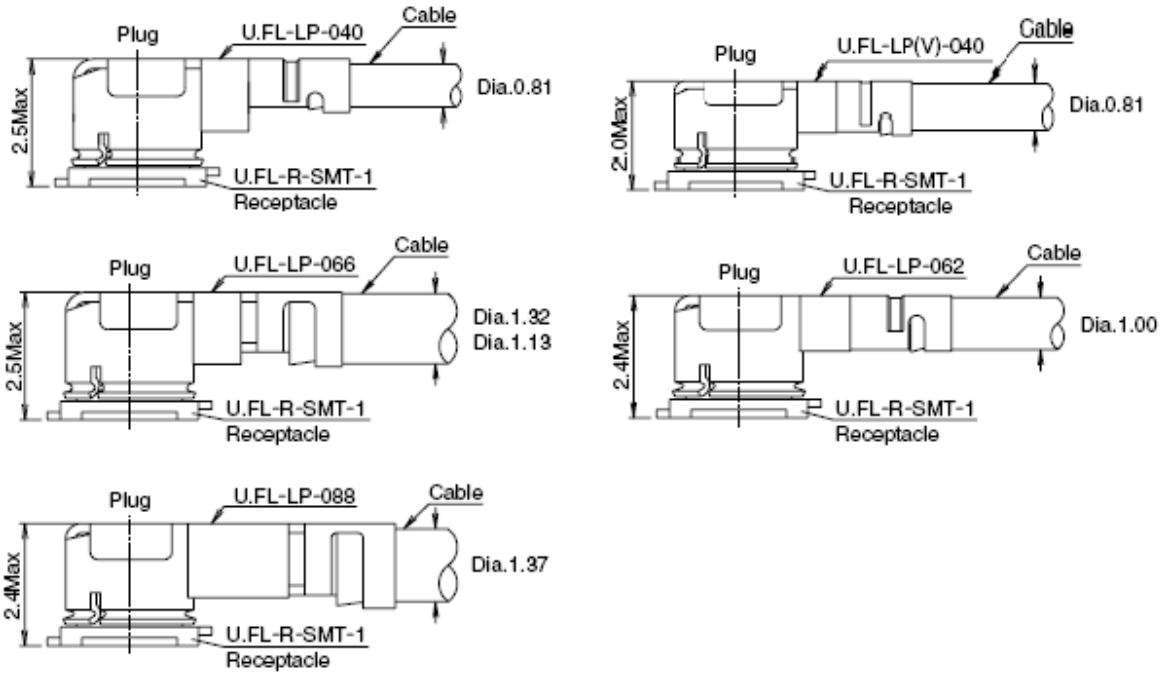


Figure 39: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 40: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	1.0	A
Peak Current of VBAT_RF	-	2.5	A
Voltage on Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT	V
Voltage at ADC1	0	VBAT	V

6.2. Power Supply Ratings

Table 41: Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum	3.3	3.8	4.3	V

		and maximum values.				
	Voltage drop during transmitting burst	Maximum power control level	-	-	400	mV
I_{VBAT}	Peak supply current	Maximum power control level	-	1.7	2.5	A
USB_VBUS	USB connection detect	-	3.5	5.0	5.25	V

6.3. Power Consumption

Table 42: Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	34	μA
Sleep state	Minimum functionality mode (USB disconnected)	1.4	mA
	Minimum functionality mode (USB connected)	2.5	mA
	Airplane mode (USB disconnected)	1.5	mA
	Airplane mode (USB connected)	2.6	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.3	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.8	mA
	EGSM900 @ DRX = 5 (USB connected)	3.3	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.6	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.3	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.8	mA
	DCS1800 @ DRX = 5 (USB connected)	3.3	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.6	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.9	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.1	mA
	LTE-FDD @ PF = 64 (USB connected)	3.6	mA

	LTE-FDD @ PF = 128 (USB disconnected)	1.7	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.5	mA
	LTE-TDD @ PF = 32 (USB disconnected)	3.0	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.1	mA
	LTE-TDD @ PF = 64 (USB connected)	3.6	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.7	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.5	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	14.1	mA
	EGSM900 @ DRX = 5 (USB connected)	30	mA
	LTE-FDD @ PF = 64 (USB disconnected)	14.2	mA
	LTE-FDD @ PF = 64 (USB connected)	30.2	mA
	LTE-TDD @ PF = 64 (USB disconnected)	14.3	mA
	LTE-TDD @ PF = 64 (USB connected)	30.2	mA
LTE data transfer	LTE-FDD B1 @ 22.93 dBm	773	mA
	LTE-FDD B2 @ 22.93 dBm	604	mA
	LTE-FDD B3 @ 22.86 dBm	718	mA
	LTE-FDD B4 @ 22.93 dBm	683	mA
	LTE-FDD B5 @ 23.51 dBm	677	mA
	LTE-FDD B7 @ 22.93 dBm	855	mA
	LTE-FDD B8 @ 22.79 dBm	669	mA
	LTE-FDD B12 @ 22.93 dBm	613	mA
	LTE-FDD B13 @ 22.93 dBm	623	mA
	LTE-FDD B17 @ 22.93 dBm	614	mA
	LTE-FDD B18 @ 22.93 dBm	661	mA
	LTE-FDD B19 @ 22.93 dBm	663	mA
	LTE-FDD B20 @ 22.93 dBm	712	mA

	LTE-FDD B25 @ 22.93 dBm	642	mA
	LTE-FDD B26 @ 22.93 dBm	688	mA
	LTE-FDD B28 @ 22.93 dBm	666	mA
	LTE-FDD B66 @ 22.93 dBm	673	mA
	LTE-TDD B34 @ 23.32 dBm	280	mA
	LTE-TDD B38 @ 23.29 dBm	450	mA
	LTE-TDD B39 @ 23.15 dBm	268	mA
	LTE-TDD B40 @ 22.97 dBm	386	mA
	LTE-TDD B41 @ 23.06 dBm	402	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.95 dBm	234	mA
	GSM850 3DL/2UL @ 30.94 dBm	338	mA
	GSM850 2DL/3UL @ 29.02 dBm	396	mA
	GSM850 1DL/4UL @ 27.03 dBm	417	mA
	EGSM900 4DL/1UL @ 32.27 dBm	230	mA
	EGSM900 3DL/2UL @ 31.01 dBm	378	mA
	EGSM900 2DL/3UL @ 29.20 dBm	447	mA
	EGSM900 1DL/4UL @ 27.41 dBm	488	mA
	DCS1800 4DL/1UL @ 30.95 dBm	189	mA
	DCS1800 3DL/2UL @ 28.76 dBm	272	mA
	DCS1800 2DL/3UL @ 26.64 dBm	310	mA
	DCS1800 1DL/4UL @ 24.35 dBm	322	mA
	PCS1900 4DL/1UL @ 30.17 dBm	168	mA
	PCS1900 3DL/2UL @ 28.08 dBm	238	mA
	PCS1900 2DL/3UL @ 26.13 dBm	276	mA
	PCS1900 1DL/4UL @ 24.10 dBm	288	mA
GSM voice call	GSM850 PCL = 5 @ 32.88 dBm	239	mA

	GSM850 PCL = 12 @ 18.87 dBm	90	mA
	GSM850 PCL = 19 @ 4.77 dBm	63	mA
	EGSM900 PCL = 5 @ 32.72 dBm	257	mA
	EGSM900 PCL = 12 @ 19.35 dBm	99	mA
	EGSM900 PCL = 19 @ 4.82 dBm	64	mA
	DCS1800 PCL = 0 @ 30.35 dBm	188	mA
	DCS1800 PCL = 7 @ 16.39 dBm	80	mA
	DCS1800 PCL = 15 @ 1.29 dBm	61	mA
	PCS1900 PCL = 0 @ 30.06 dBm	172	mA
	PCS1900 PCL = 7 @ 16.01 dBm	78	mA
	PCS1900 PCL = 15 @ 1.29 dBm	61	mA

6.4. Digital I/O Characteristics

Table 43: 1.8 V I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	Input high voltage	0.7 × VDDIO	VDDIO + 0.2
V_{IL}	Input low voltage	-0.3	0.3 × VDDIO
V_{OH}	Output high voltage	VDDIO - 0.2	-
V_{OL}	Output low voltage	-	0.2

Table 44: (U)SIM Low-voltage I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
USIM_VDD	Power supply	1.62	1.98
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD

V_{IL}	Input low voltage	0	0.2 × USIM_VDD
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD
V_{OL}	Output low voltage	0	0.15 × USIM_VDD

Table 45: (U)SIM High-voltage I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
USIM_VDD	Power supply	2.9	3.3
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD
V_{IL}	Input low voltage	0	0.15 × USIM_VDD
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD
V_{OL}	Output low voltage	0	0.15 × USIM_VDD

Table 46: SDIO High-voltage I/O Requirements

Parameter	Description	Min.	Max.
V_{IH}	Input high voltage	0.7 × VDDIO	-
V_{IL}	Input low voltage	-	0.15 × VDDIO
V_{OH}	Output high voltage	2.4 V	VDDIO
V_{OL}	Output low voltage	0	0.3 V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the electrostatics discharge characteristics of the module.

Table 47: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 48: Operating and Storage Temperatures (Unit: ºC)

Parameter	Min.	Typ.	Max.
Operating Temperature Range [5]	-35	+25	+75
Extended Operation Range [6]	-40	+25	+85
Storage Temperature Range	-40	+25	+90

[5] Within operating temperature range, the module meets 3GPP specifications.
[6] Within extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

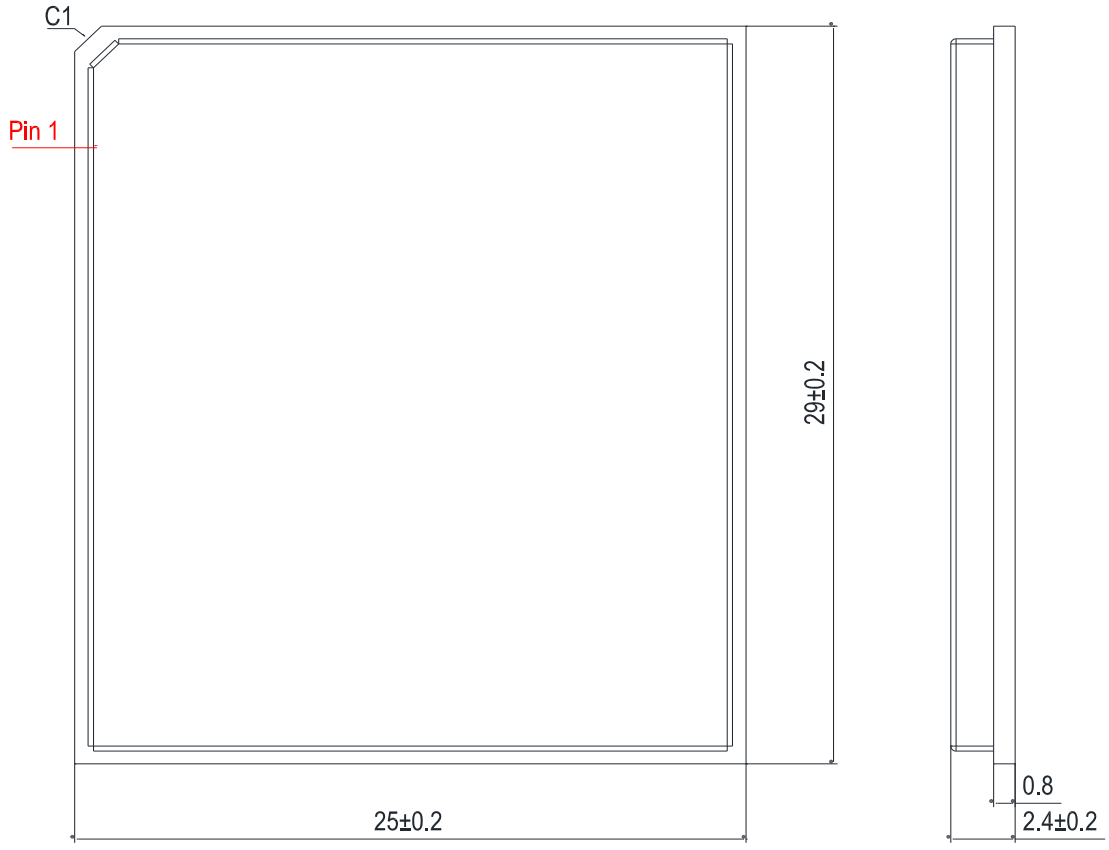


Figure 40: Module Top and Side Dimensions (Unit: mm)

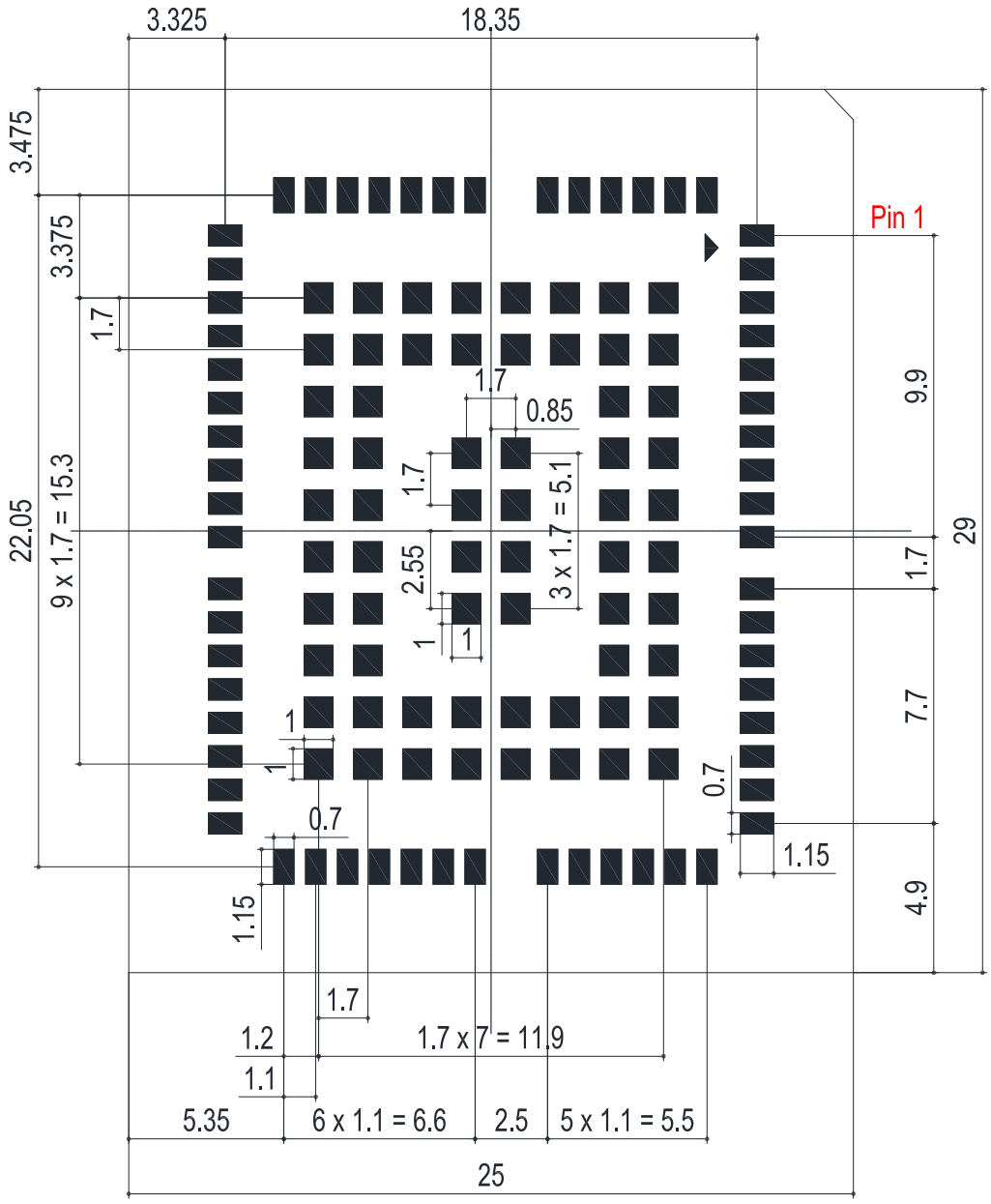


Figure 41: Bottom Dimension (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

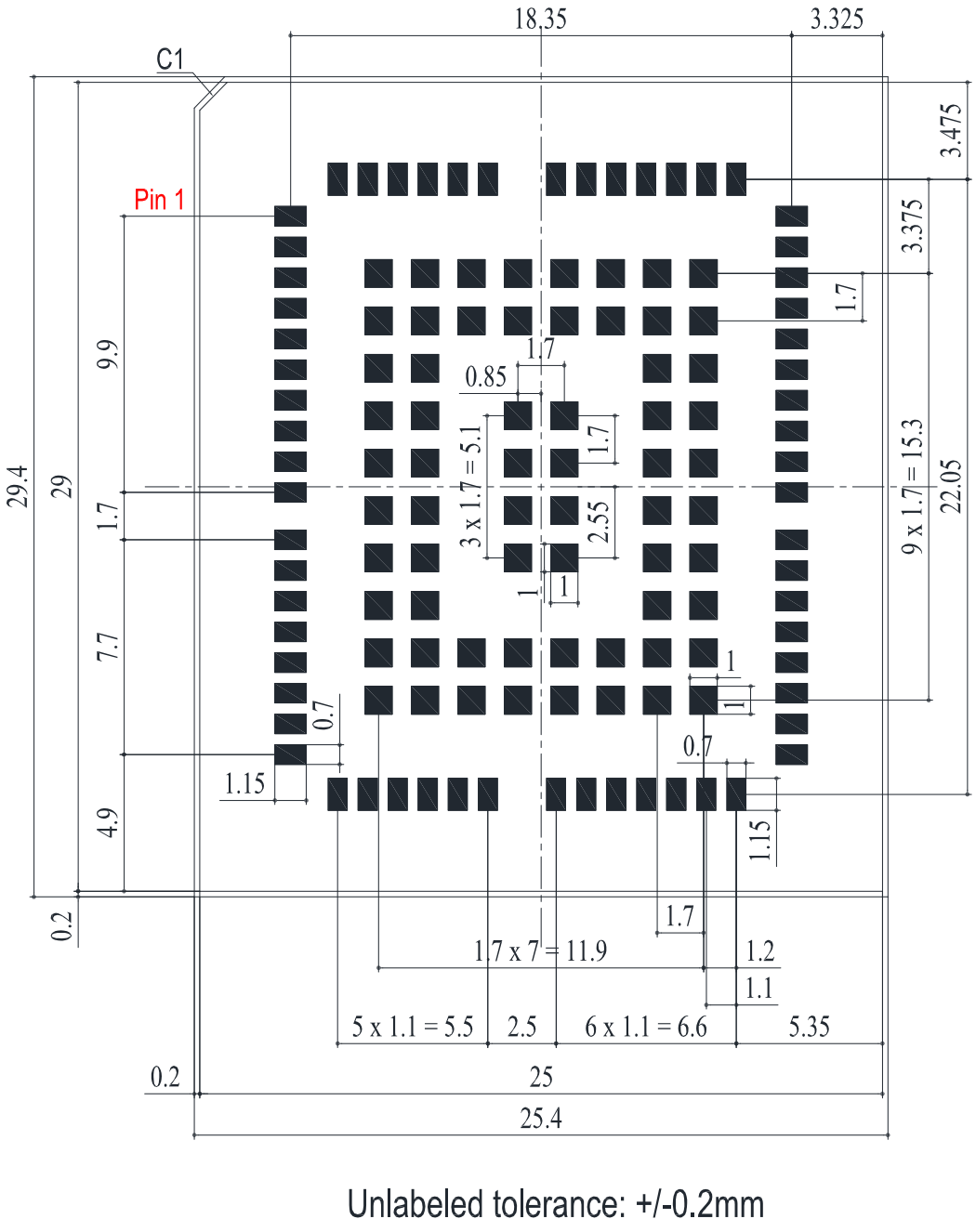


Figure 42: Recommended Footprint (Top View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

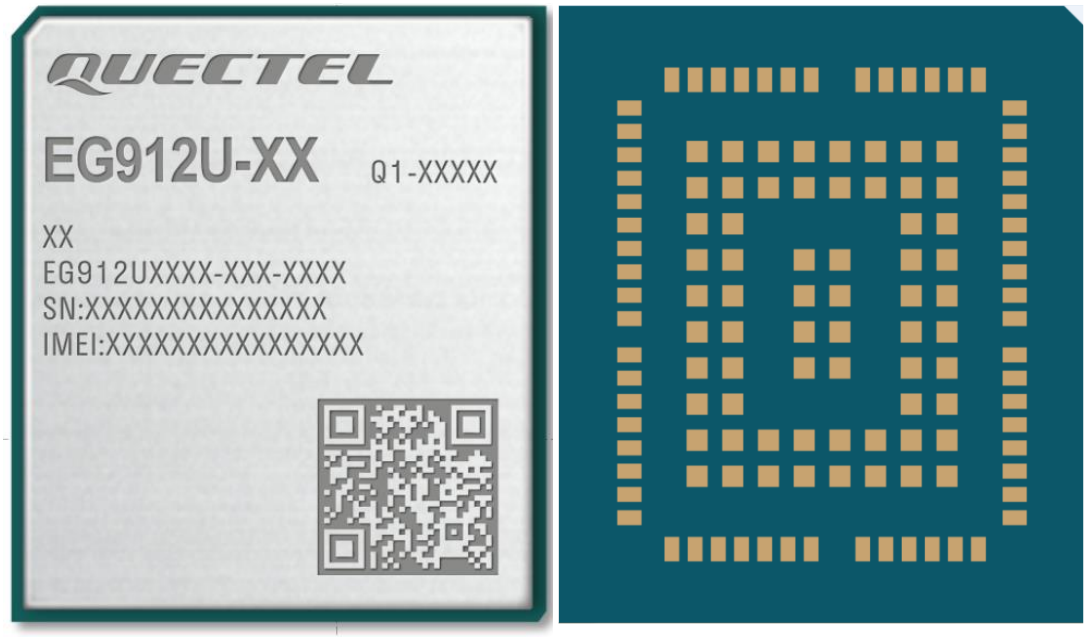


Figure 43: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing, and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [7] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[7] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [12]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

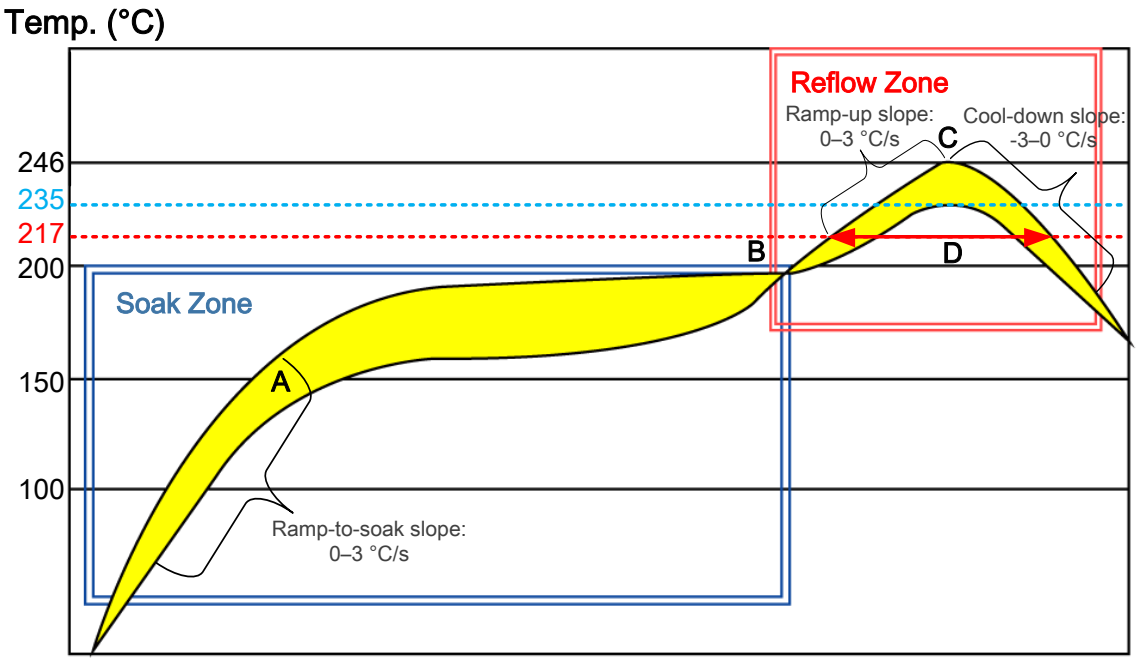


Figure 44: Recommended Reflow Soldering Thermal Profile

Table 49: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [12]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

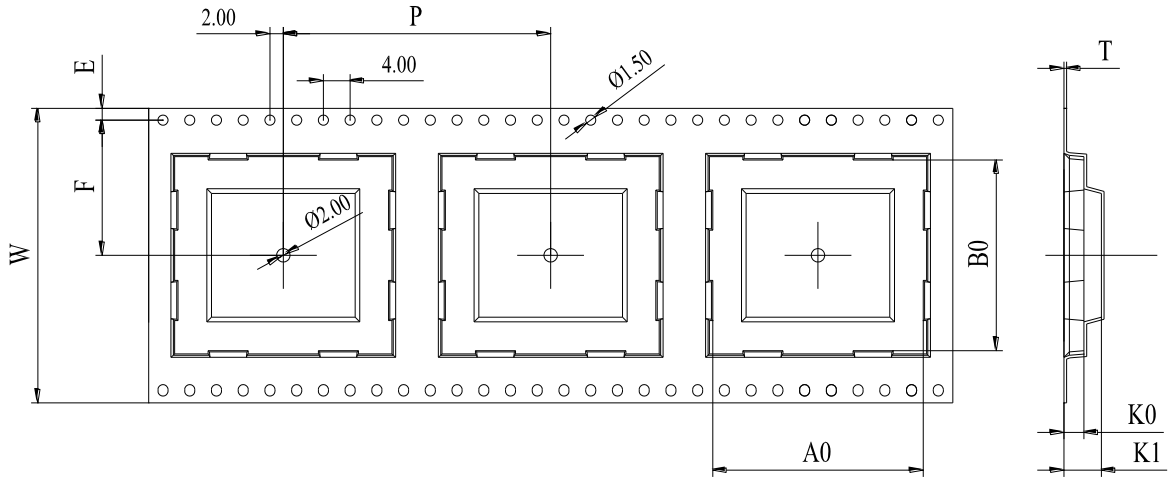


Figure 45: Carrier Tape Dimension Drawing

Table 50: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	25.5	29.5	3.2	5.8	20.2	1.75

8.3.2. Plastic Reel

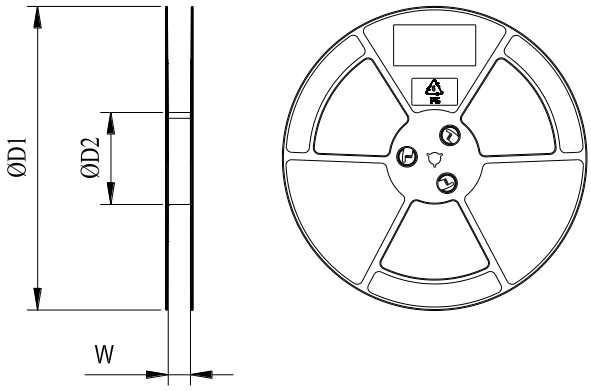


Figure 46: Plastic Reel Dimension Drawing

Table 51: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

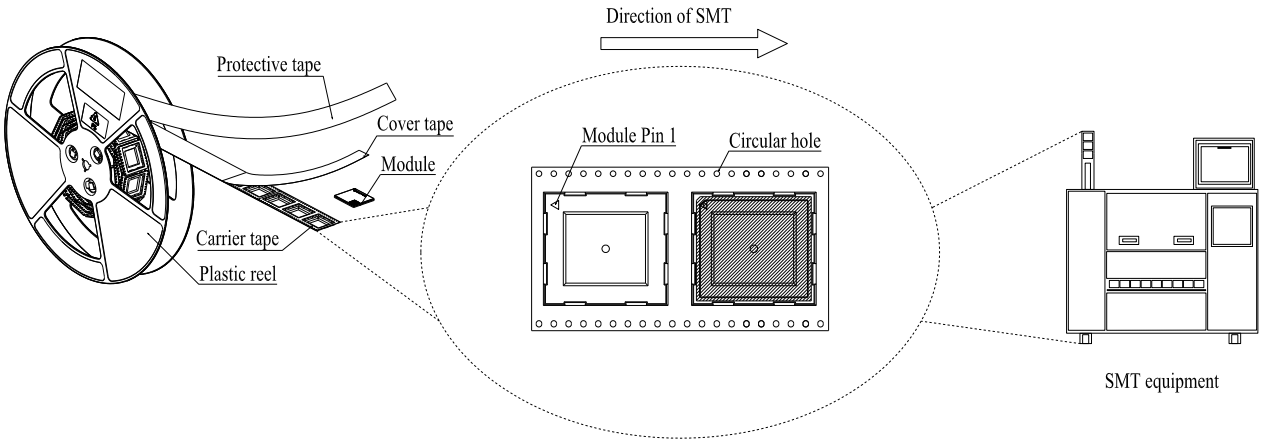
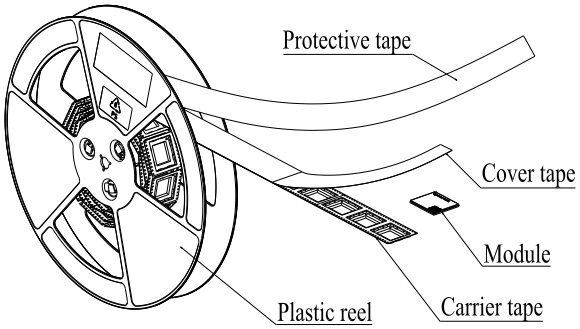


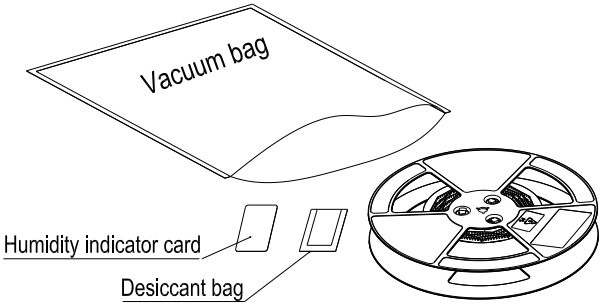
Figure 47: Mounting Direction

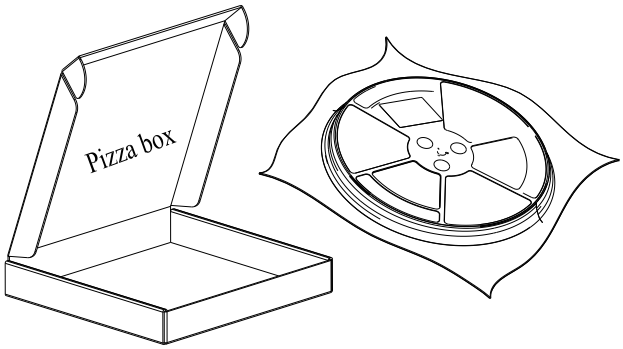
8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

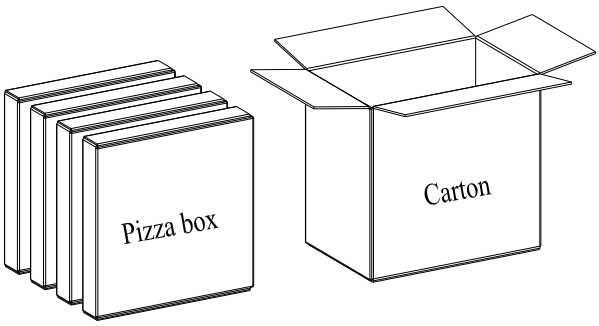


Figure 48: Packaging Process

9 Appendix References

Table 52: Related Documents

Document Name	
[1]	Quectel_EG912U-GL_QuecOpen_GPIO_Configuration
[2]	Quectel_LTE_OPEN_EVB_User_Guide
[3]	Quectel_EC200U&EG91xU_Series_QuecOpen_Device_Management_API_Reference_Manual
[4]	Quectel_EC200U&EG91xU_Series_QuecOpen_ Low_Power_Consumption_API_ Reference_Manual
[5]	Quectel_EC200U&EG91xU_Series_QuecOpen_PSM_Application_Note
[6]	Quectel_EC200U&EG91xU_Series_QuecOpen_Booting&Shutdown_Development_Guide
[7]	Quectel_EC200U&EG91xU_Series_QuecOpen_(U)SIM_API_Reference_Manual
[8]	Quectel_EC200U&EG91xU_Series_QuecOpen_ADC_Development_Guide
[9]	Quectel_EG912U-GL_QuecOpen_Reference_Design
[10]	Quectel_EC200U_Series&EG912U-GL_GNSS_ API_Reference_Manual
[11]	Quectel_RF_Layout_Application_Note
[12]	Quectel_Module_SMT_Application_Note

Table 53: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
AMR-WB	Adaptive Multi-Rate Wideband

AP	Application Processor
API	Application Programming Interface
BDS	BeiDou Navigation Satellite System
bps	bit(s) per second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection Multiplexing
CS	Coding Scheme
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DMA	Direct Memory Access
DRX	Discontinuous Reception
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FDD	Frequency Division Duplex
FILE	File Protocol
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP-SSL: FTP over SSL/FTP Secure
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Global Navigation Satellite System (Russia)

GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GPS	Global Positioning System
GRFC	General RF Control
GSM	Global System for Mobile Communications
HB	High Band
HR	Half Rate
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IMT-2000	International Mobile Telecommunications 2000
I/O	Input/Output
LB	Low Band
LCM	Liquid Crystal Monitor
LDO	Low-dropout Regulator
LGA	Land Grid Array
LNA	Low-Noise Amplifier
LTE	Long-Term Evolution
MB	Medium Band
MCU	Microcontroller Unit
ME	Mobile Equipment
MLCC	Multi-layer Ceramic Capacitor
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Levels
NITZ	Network Identity and Time Zone/Network Informed Time Zone

NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NTP	Network Time Protocol
PA	Power Amplifier
PAM	Power Amplifier Module
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PING	Packet Internet Groper
PMU	Power Management Unit
PPP	Point-to-Point Protocol
PSM	Power Saving Mode
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
RTS	Ready To Send/Request to Send
SAW	Surface Acoustic Wave
SDIO	Secure Digital Input/Output
SMS	Short Message Service
SMT	Surface Mount Technology
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SPI	Serial Peripheral Interface

SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TVS	Transient Voltage Suppressor
Tx	Transmit/Transmission
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio