EG912N-EN QuecOpen Reference Design

LTE Standard Module Series

Version: 1.0

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Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2022-08-16	Dylan LIU	Creation of the document
1.0	2023-05-19	Dylan LIU	First official release

Contents

1 Reference Design

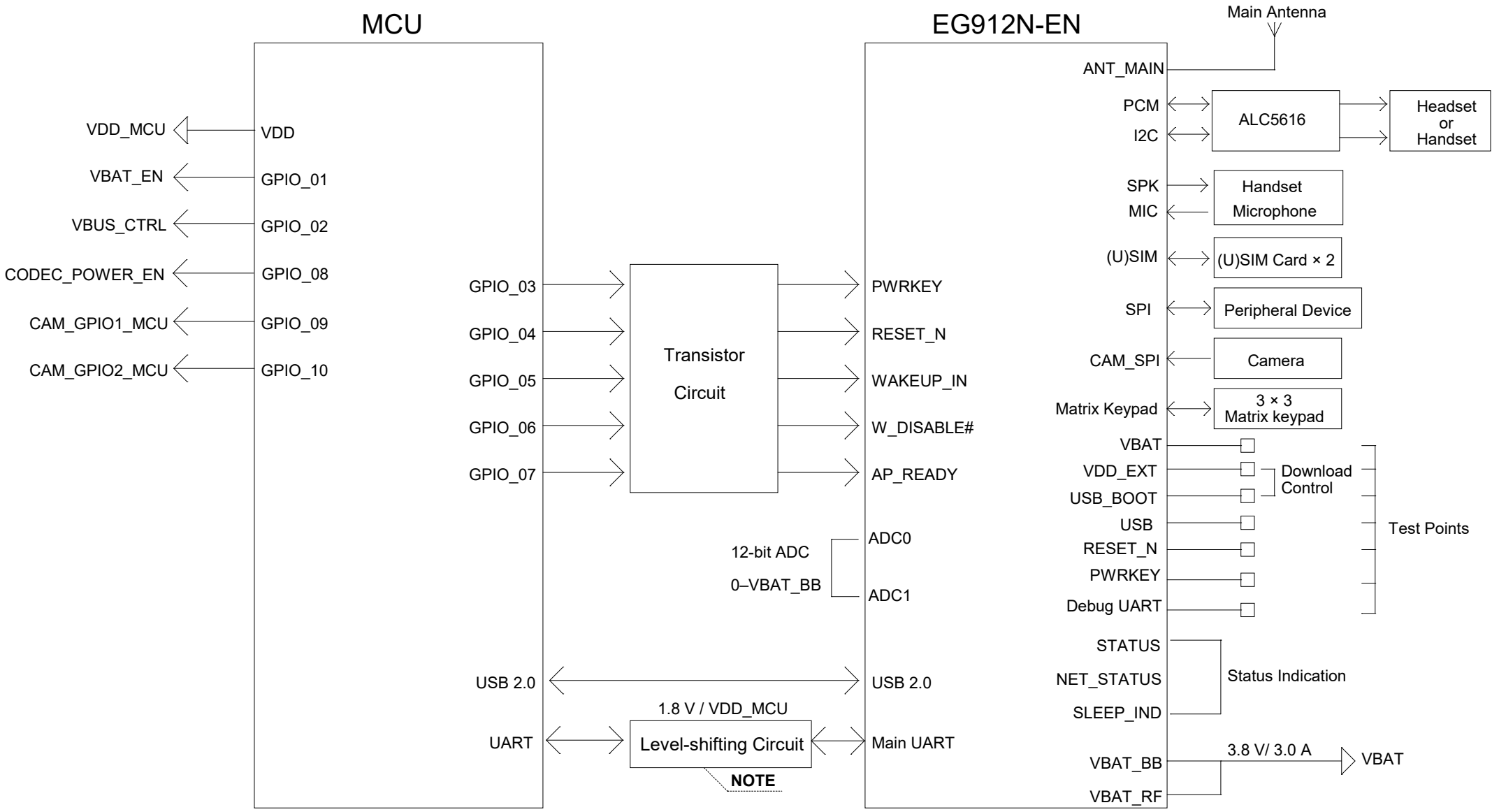
1.1. Introduction

This document provides the reference design for Quectel EG912N-EN module in QuecOpen® solution.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



NOTE:

A level-shifting circuit or a voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.

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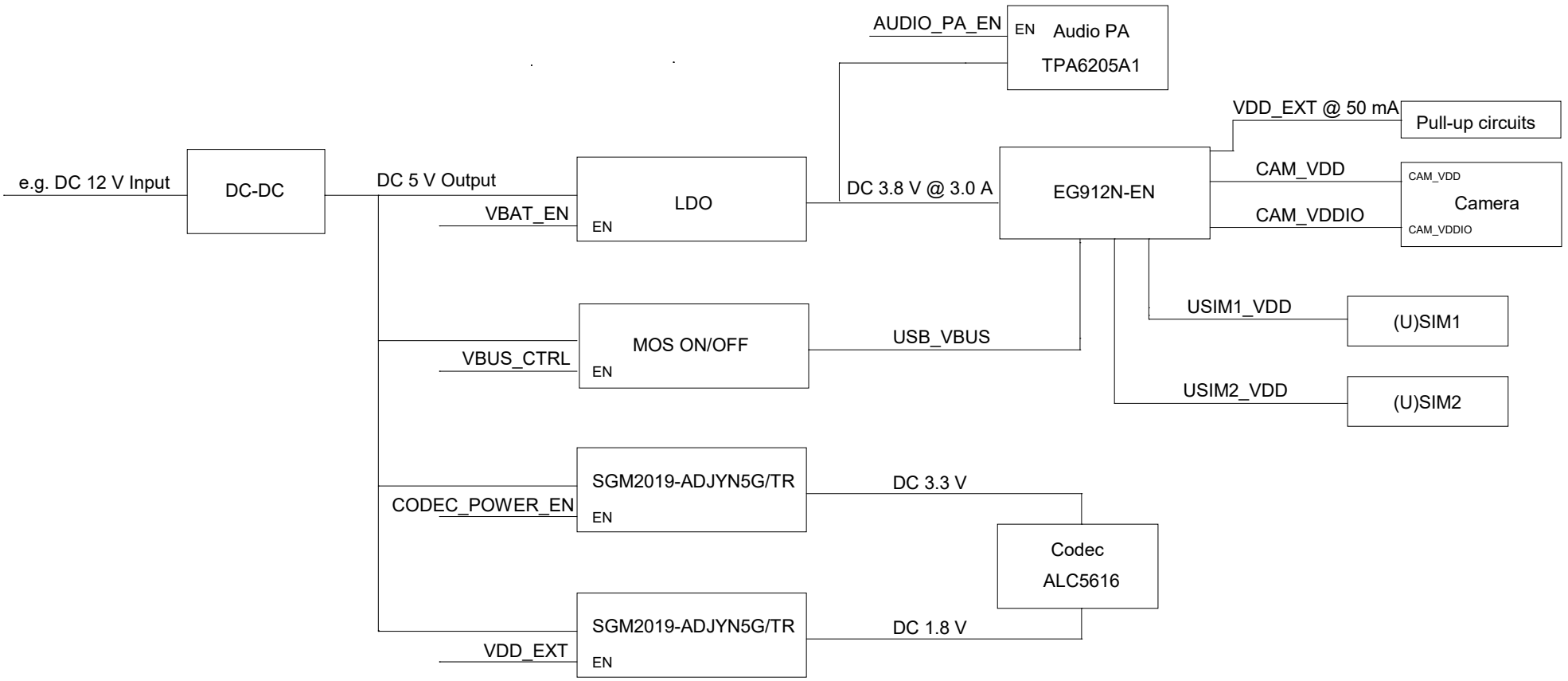
Power System Block Diagram



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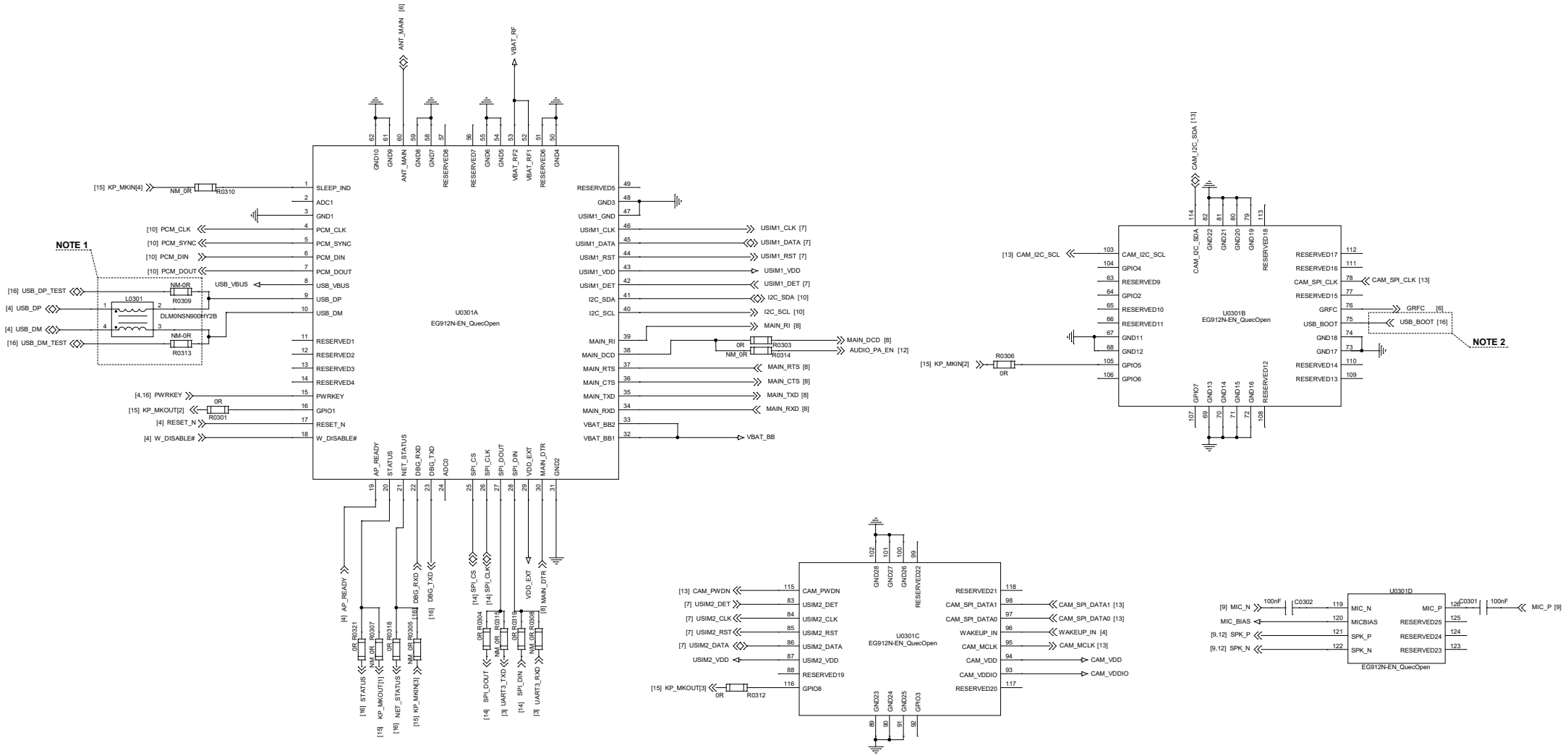
Module Interfaces



NOTE:

1. A common mode choke L0301 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the test points must be reserved for upgrading the firmware over USB interface and the extra stubs of the trace should be minimized. L0301 and the two resistors R0309 and R0313 should be placed close to the module to ensure the integrity of USB signal.
2. USB_BOOT cannot be pulled up to high level before the module starts up successfully.
3. All GND pins should be connected to the ground, and unused and RESERVED pins should be kept open.
4. Ensure there is a complete reference ground plane below the module, and the ground plane should be placed as close to the module layer as possible. Other traces cannot be routed on the first layer below the module. At least four-layer design is recommended.

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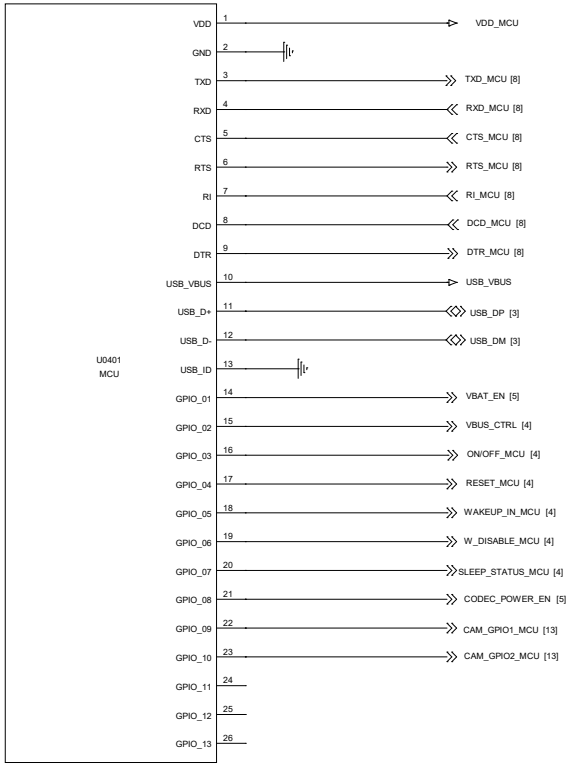
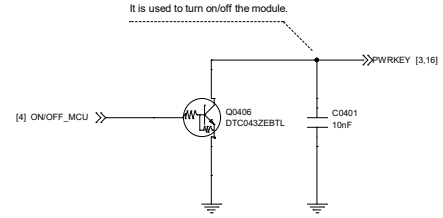
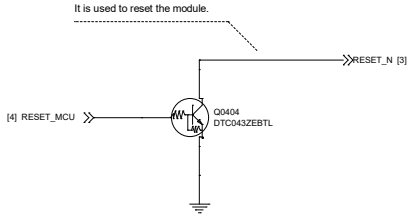
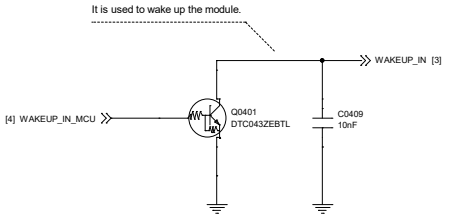
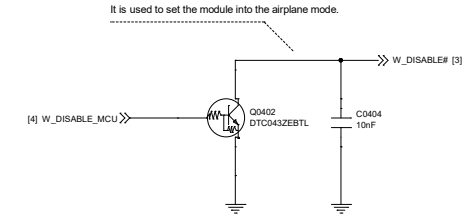
MCU Interfaces

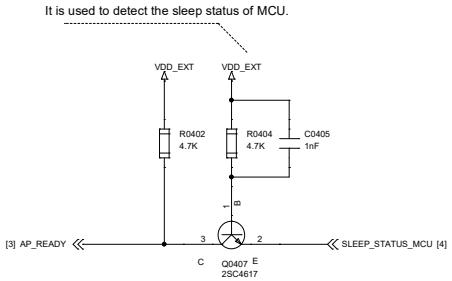


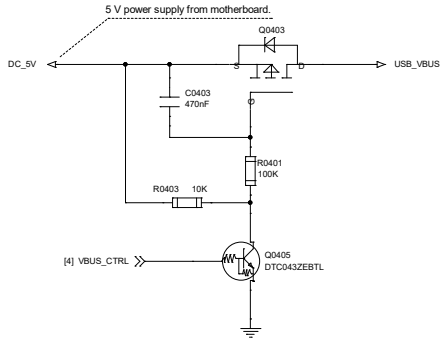












NOTE:

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V. If the power domain of GPIO interfaces of U0401 is also 1.8 V, then the related level-shifting circuit is not needed.
2. The USB 2.0 interface of the module only serves as a slave device and supports full-speed and high-speed modes. To communicate with the USB interface, MCU needs to support USB host mode or OTG function.
   The USB_VBUS of the module should be powered by an external power supply for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the GPIO pins which are at low level by default of MCU as the control pins for PWRKEY and RESET_N of the module. Ensure that the load capacitance does not exceed 10 nF on PWRKEY and RESET_N.

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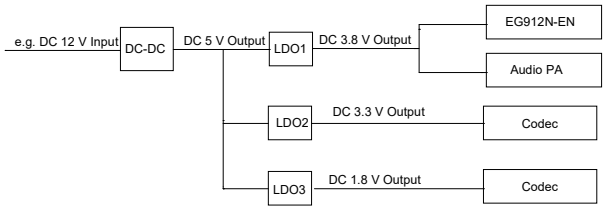
Power Supply Design

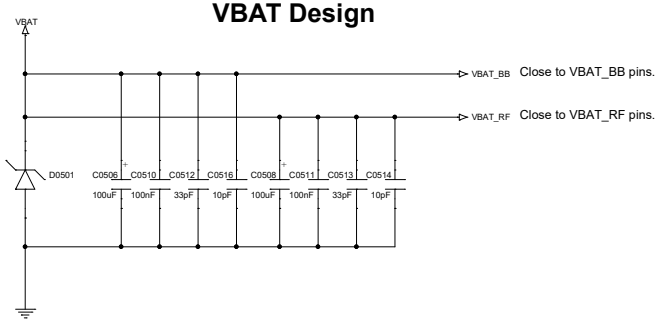
DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to 5.0 V, and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V to power the module, audio PA and Codec.

The supply current of the module must be at least 3.0 A.



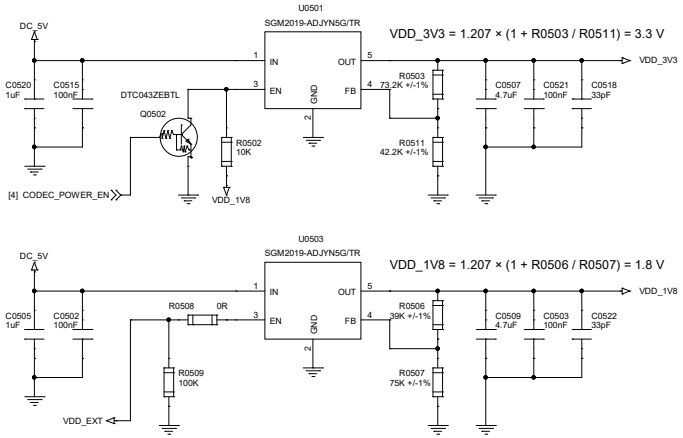
VBAT Design



NOTE:

1. The power supply should be able to provide sufficient current of at least 3.0 A for the module.
2. The VBAT trace should be connected to VBAT_BB and VBAT_RF pins in a star configuration.
3. The width of VBAT_BB trace should not be less than 1 mm; and the width of VBAT_RF trace should not be less than 2 mm.
4. The recommended operating voltage of VBAT ranges from 3.4 V to 4.3 V, and the typical voltage is 3.8 V.

Power Supply for Codec



NOTE:

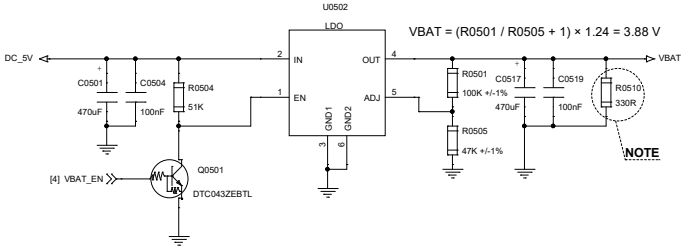
1. VDD_EXT and CODEC_POWER_EN are used to turn on/off VDD_1V8 and VDD_3V3 respectively.
2. The following power-up/down sequences should be followed to ensure the audio codec works normally.

   Power-up sequence: power up VDD_1V8 first, and then VDD_3V3.

   Power-down sequence: power down VDD_3V3 first, and then VDD_1V8.

LDO Application

When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



NOTE:

The recommended load current should be greater than 10 mA.

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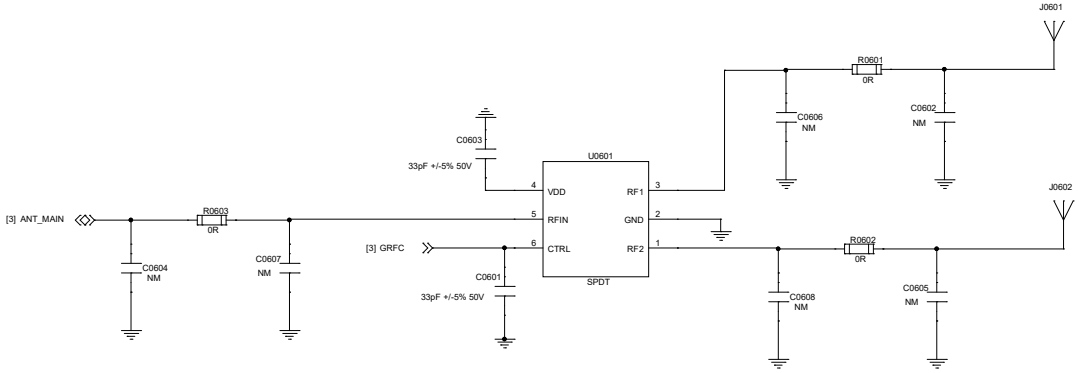
Antenna Interface Design



NOTE:

1. The signle-ended impedance of the RF antenna is 50 Ω.
2. It is recommended to reserve a Π-type matching circuit.

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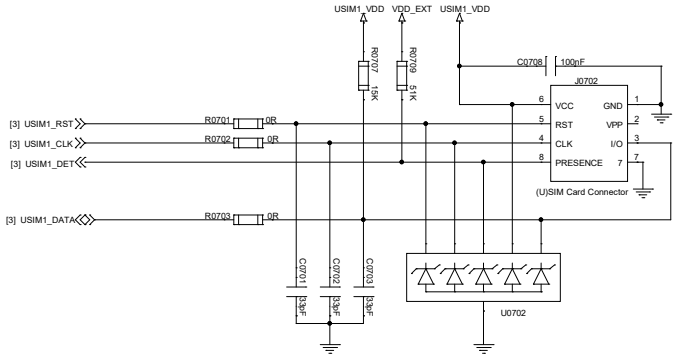
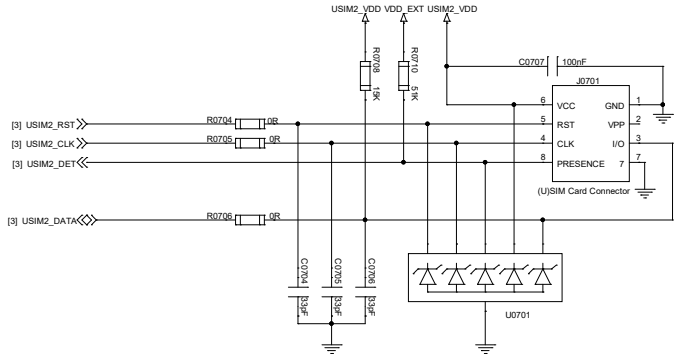
(U)SIM Interface Design

(U)SIM1



(U)SIM2



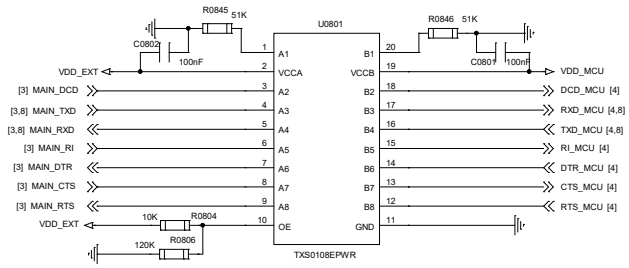
NOTE:

1. U0701 and U0702 are recommended to be used to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.
2. The pull-up resistors R0707 and R0708 can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.
3. R0701–R0706 are used for debugging, and C0701–C0706 are used for filtering out RF interference.
4. The capacitance of C0707 and C0708 should be less than 1 μF and they should be placed close to the (U)SIM card connector.
5. The GND of the (U)SIM card connector is recommended to be connected to the GND layer directly .
6. For more information about the layout of (U)SIM interface, refer to *Quectel_EG912N-EN_QuecOpen_Hardware_Design.*

UART Interfaces Design

UART Level-shifting Circuit - Transistor Solution

UART Level-shifting Circuit - IC Solution



NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter one.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, refer to the datasheet of TXS0108EPWR.
3. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps.The capacitors C0803 and C0804 of 1 nF can improve the signal quality.
4. MAIN_RTS and MAIN_DTR level-shifting circuits are similar to that of the MAIN_RXD.
   MAIN_CTS, MAIN_RI and MAIN_DCD level-shifting circuits are similar to that of the MAIN_TXD.

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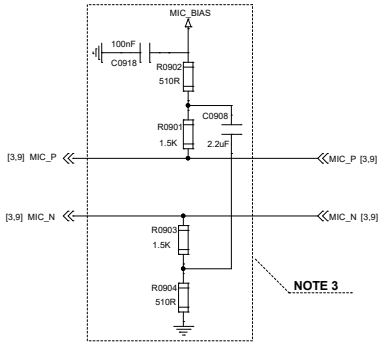
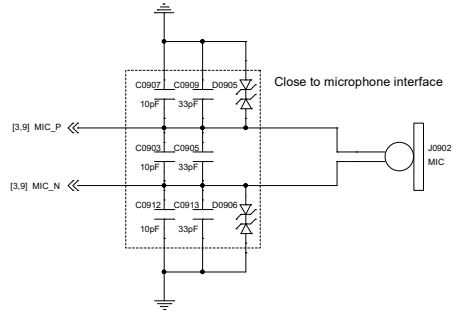
Analog Audio Design

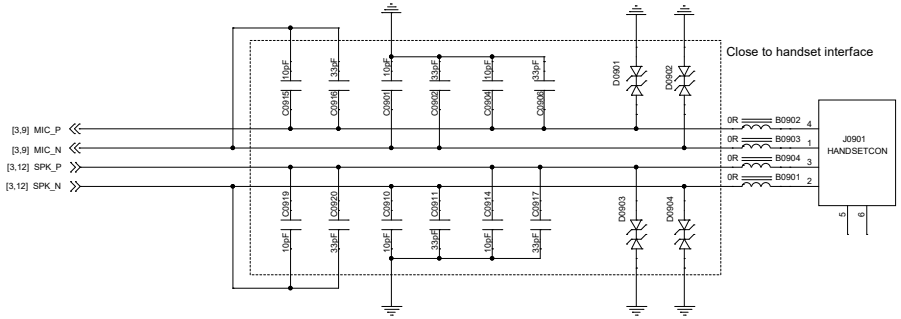
Microphone Bias Circuit



Microphone Application



Handset Application



NOTE:

1. Both the MIC and SPK signal traces need to be routed as differential pairs.
2. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noises.
3. An external micbias circuit must be added when using electret microphone.
4. It is recommended to use 10 pF and 33 pF capacitors to filter RF interference.

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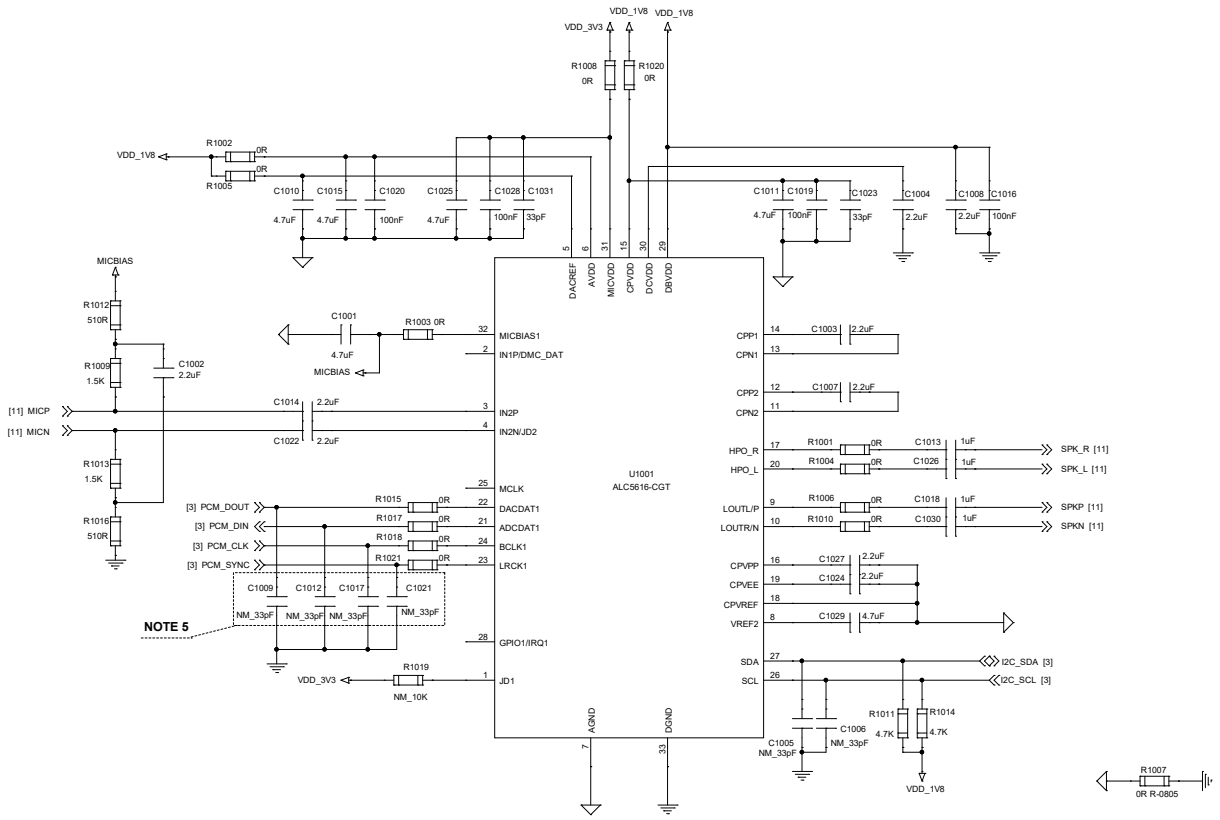
Audio Codec Design (ALC5616)



NOTE:

1. ALC5616 power-up sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD → MICVDD → software initialization.
2. ALC5616 power-down sequence: disable Codec function by software → MICVDD → DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.
3. The module will automatically initialize the Codec via I2C interface after it is turned on successfully, so all power supplies for the Codec need to be powered up before that.
4. Pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805. For more details, see Sheet "Audio Codec Interface Design".
5. The 33 pF capacitors of the signal pins should be reserved, and be used according to the actual debugging situation.
6. For more details, see the datasheet of ALC5616.

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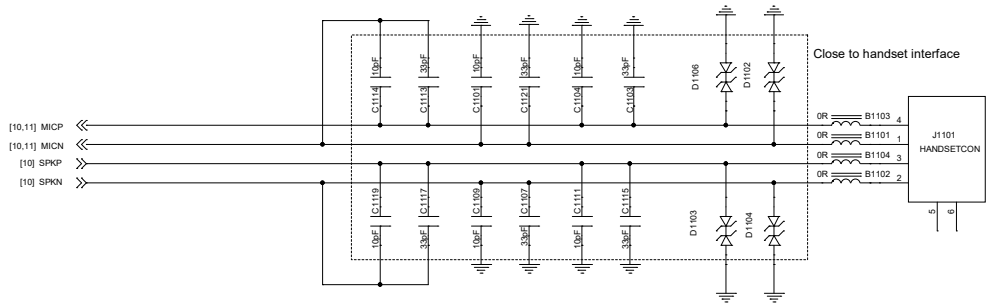
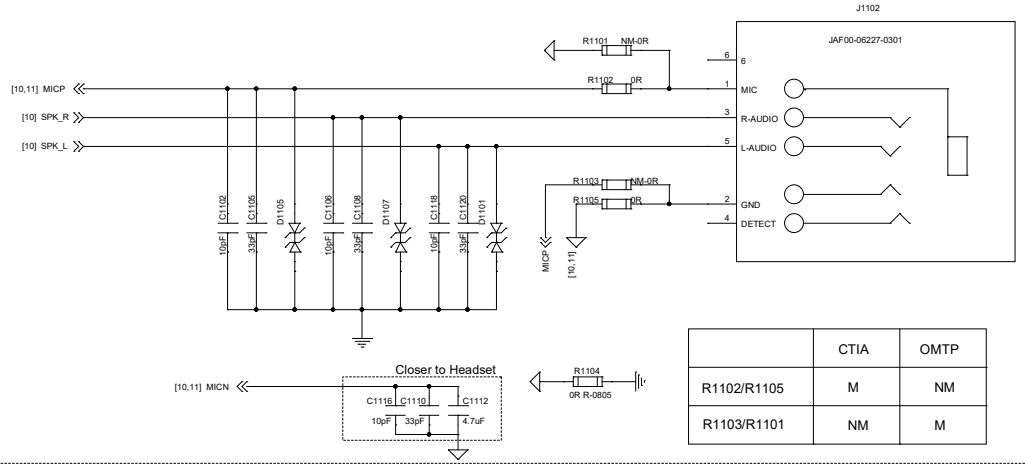
Audio Codec Interface Design

Handset Application



Headset Application



	CTIA	OMTP
R1102/R1105	M	NM
R1103/R1101	NM	M

NOTE:

1. The Codec analog output can drive handset and headset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.
2. In handset application, route the MIC and SPK signal traces as differential pairs respectively.
3. In headset application, route the MIC signal traces as a differential pair.
4. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noises such as clock and DC-DC signals.
5. Pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805 (short-circuit through single point grounding).

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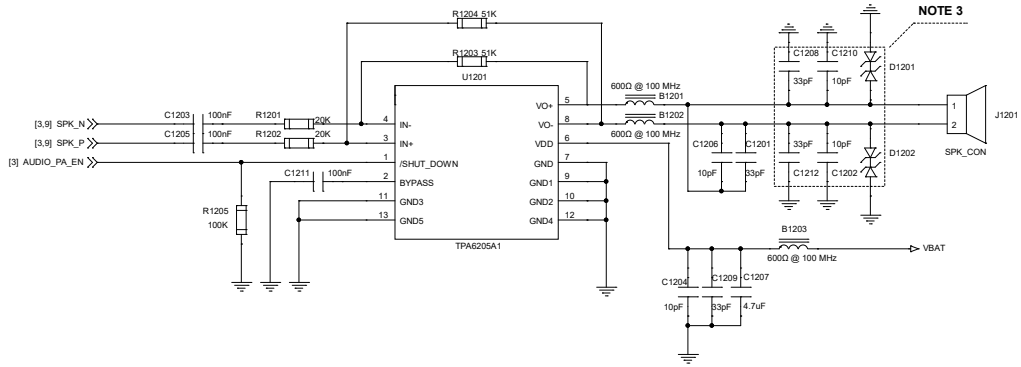
Analog Audio Design (Audio Power Amplifier)



NOTE:

1. SPK_P and SPK_N are differential output channels that can be used for external audio amplifier.

   It is recommended to use GPIO pins of the module to control the enable pin of the audio power amplifier to eliminate POP noise, and the selected GPIO pin should be at low level by default, such as MAIN_DCD. For more information about AUDIO_PA_EN, contact Quectel Technical Support.

2. The type of power amplifier in this design is for reference only. Select the appropriate audio power amplifier according to actual needs.
3. Filter capacitors and ESD protection components should be placed close to the loudspeaker.
4. The selection of ESD protection components is related to the selection of audio power amplifier. Ensure that the output voltage of audio power amplifier is within the maximum reverse working voltage range of ESD protection components under normal working condition, so as to avoid damage to ESD protection components .

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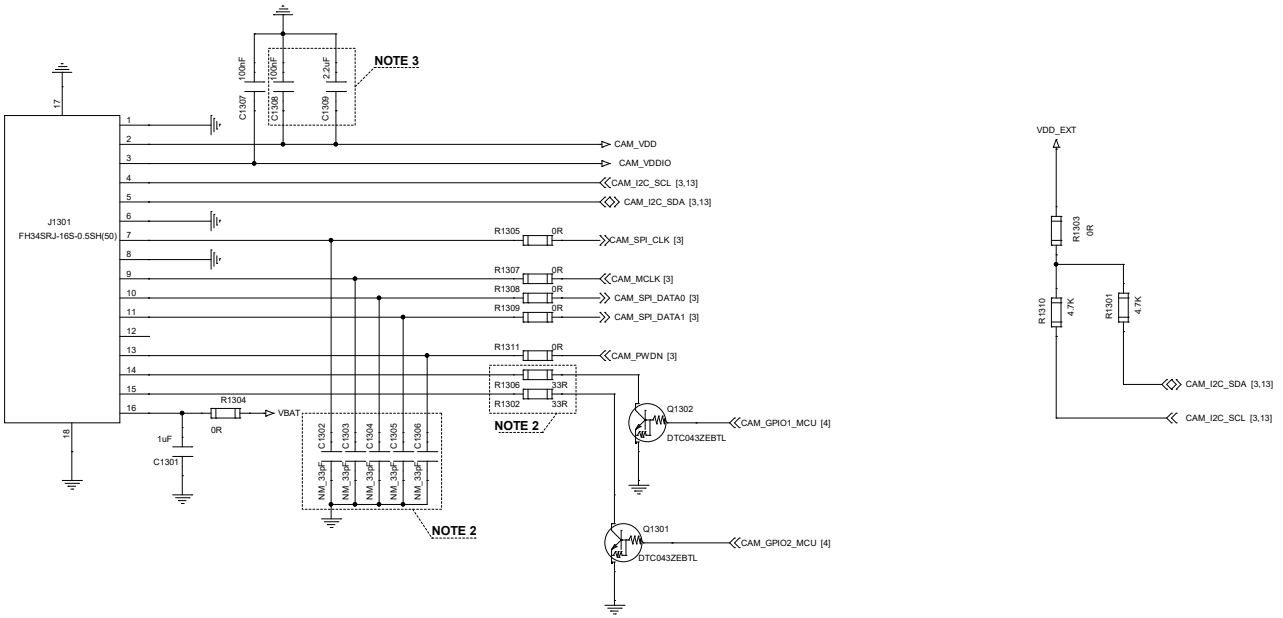
Camera Interface Design



NOTE:

1. By controlling the triode switching circuit, CAM_GPIO1_MCU controls the cathode of the positioning light of the camera, and CAM_GPIO2_MCU controls the cathode of the supplement light of the camera.
   It is recommended to select GPIO pins which are in pull-down status by default as the two control pins.
2. The 33 pF capacitors of the signal pins are reserved, and they can be used according to the actual debugging situation.
   The values of current limiting resistors of positioning light and supplement light (R1302 and R1306) should be varied according to brightness requirements.
3. The capacitor of the CAM_VDD power supply should be connected to the GND layer directly, otherwise there may be power noise resulting in abnormalities such as white dots on the preview screen.

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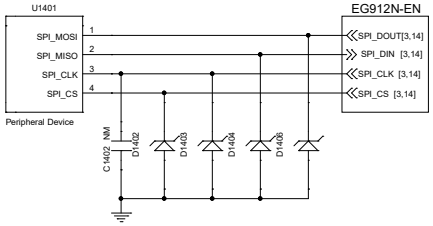
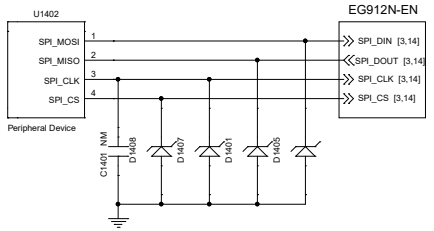
SPI Interface Design

Module As Master



Module As Slave



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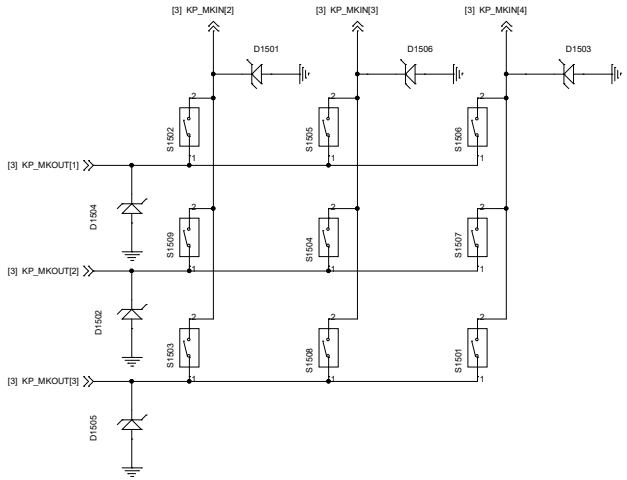
Matrix Keypad Interface Design



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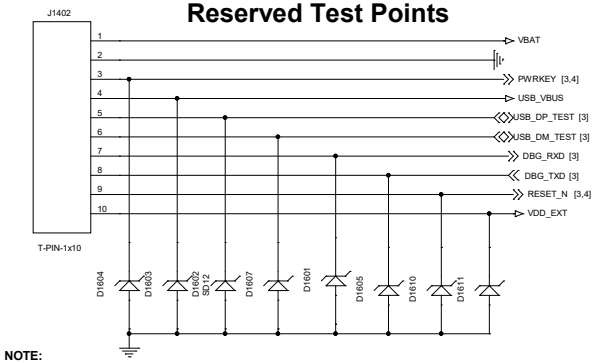
Other Designs

Indicators

NOTE:

1. For more details about STATUS and NET_STATUS, refer to *Quectel_EG912N-EN_QuecOpen_Hardware_Design*.
2. If the low current consumption is required when your device is in sleep mode, replace the power supply VBAT of the STATUS and NET_STATUS indicators with external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

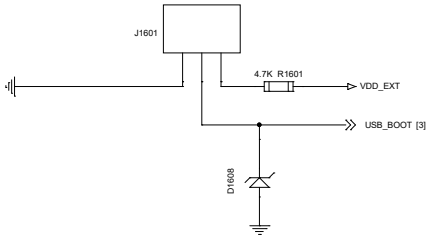
Reserved Test Points



NOTE:

1. Test points for both USB and debug UART interfaces are reserved for catching logs.
2. Test points for USB interface can also be reserved for firmware upgrade.
3. The junction capacitance of the ESD protection components on USB data lines should be less than 2 pF.
4. The debug UART interface supports 1.8 V power domain, and a voltage-level translator should be used if the power domain of your application is 3.3 V.

USB_BOOT Interface



NOTE:

1. Ensure to reserve the USB_BOOT interface design and test points.
2. Before the module is turned on, pull up USB_BOOT to 1.8 V, or short-circuit VDD_EXT and USB_BOOT, and the module will enter emergency download mode. In this mode, the module supports firmware upgrade over USB interface.

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