EG912N-EN QuecOpen Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Revision	Date	Author	Description
-	2022-08-16	Dylan LIU/Jeff SHEN/ Sharon LI	Creation of the document
1.0	2023-06-25	Dylan LIU/Jeff SHEN/ Sharon LI	First official release

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines the EG912N-EN module in QuecOpen® solution and describes its air interfaces and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up wireless applications with the module.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

The module is an SMD module with compact packaging, which is engineered to meet most of the demands of M2M applications, for instance:

- OTT
- CPE
- PoC
- POS
- Tracker
- Data card
- Security system
- Industrial PDA
- Metering

Table 2: Brief Introduction

EG912N-EN	
Packaging type	LGA
Pin counts	126 pins
Dimensions	(25.0 ±0.2) mm × (29.0 ±0.2) mm × (2.4 ±0.2) mm
Weight	Approx. 3.5 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

	EG912N-EN
LTE-FDD	B1/B3/B5/B7/B8/B20/B28/B31/B72
GSM	EGSM900/DCS1800

2.2. Key Features

Table 4: Key Features

Features	Details
Power Supply	● Supply voltage: 3.4–4.3 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM card and ME; ME by default
USB Interface	● Compliant with USB 2.0 specifications (slave mode only), with transmission rates up to 480 Mbps ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial driver for Windows 7/8/8.1/10/11, Linux 2.6–5.18 and Android 4.x–13.x systems
USB_BOOT Interface	Supports one emergency download interface
(U)SIM Interface	Supports (U)SIM card: 1.8/3.0 V
UART	**Main UART:** ● Used for data transmission and AT command communication ● Baud rate: 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for log output ● Baud rate: 115200 bps **Auxiliary UART:** ● Used for communication with peripherals ● Baud rate: 115200 bps by default ● Multiplexed from SPI_DOUT and SPI_DIN, or MAIN_CTS and MAIN_RTS
Audio Features	● Supports one digital audio interface: PCM interface ● Supports one analog input and one analog output ● GSM: HR/FR/EFR/AMR ● LTE: AMR/AMR-WB ● Supports echo cancellation and noise suppression
PCM Interface	● Used for audio function with external codec ● Supports 16-bit linear data format ● Supports short frame synchronization ● Supports master mode

I2C Interface	● One I2C interface ● Comply with I2C bus specification version
ADC Interfaces	Supports two Analog-to-Digital Converter (ADC) interfaces
Camera Interface	● Provides one camera interface ● Supports up to 0.3 MP ● Supports single data line or dual data line transmission of SPI
SPI	Supports master and slave modes, with clock rates up to 26 MHz
Matrix Keypad Interface	Supports 3 × 3 matrix keypad interface
Network Indication	NET_STATUS to indicate network connectivity status
Antenna Interface	● Main antenna interface (ANT_MAIN) ● 50 Ω impedance
Transmitting Power	● EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800: Class 1 (30 dBm ±2 dB) ● EGSM900 8-PSK: Class E2 (27 dBm ±3 dB) ● DCS1800 8-PSK: Class E2 (26 dBm ±3 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Supports up to 3GPP Rel-9 non-CA Cat 1 FDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● FDD: Max. 10 Mbps (DL)/5 Mbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1–4 ● Max. 85.6 Kbps (DL)/85.6 Kbps (UL) **EDGE:** ● Supports EDGE multi-slot class 12 ● Supports GMSK and 8-PSK for different MCS ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 236.8 kbps (DL)/236.8 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP*/NTP/NITZ/FTP/HTTP/PING/CMUX*/HTTPS /FTPS/SSL/FILE/MQTT/MMS*/SMTP*/SMTPS* protocols ● Supports PAP and CHAP protocols
Temperature Range	● Operating temperature range [1]: -35 °C to +75 °C ● Extended temperature range [2]: -40 °C to +85 °C ● Storage temperature range: -40 °C to +90 °C

[1] Within the operating temperature range, the module meets 3GPP specifications.
[2] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

Firmware Upgrade	Use USB interface or DFOTA to upgrade
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- RAM & Flash
- Radio frequency
- Peripheral interfaces

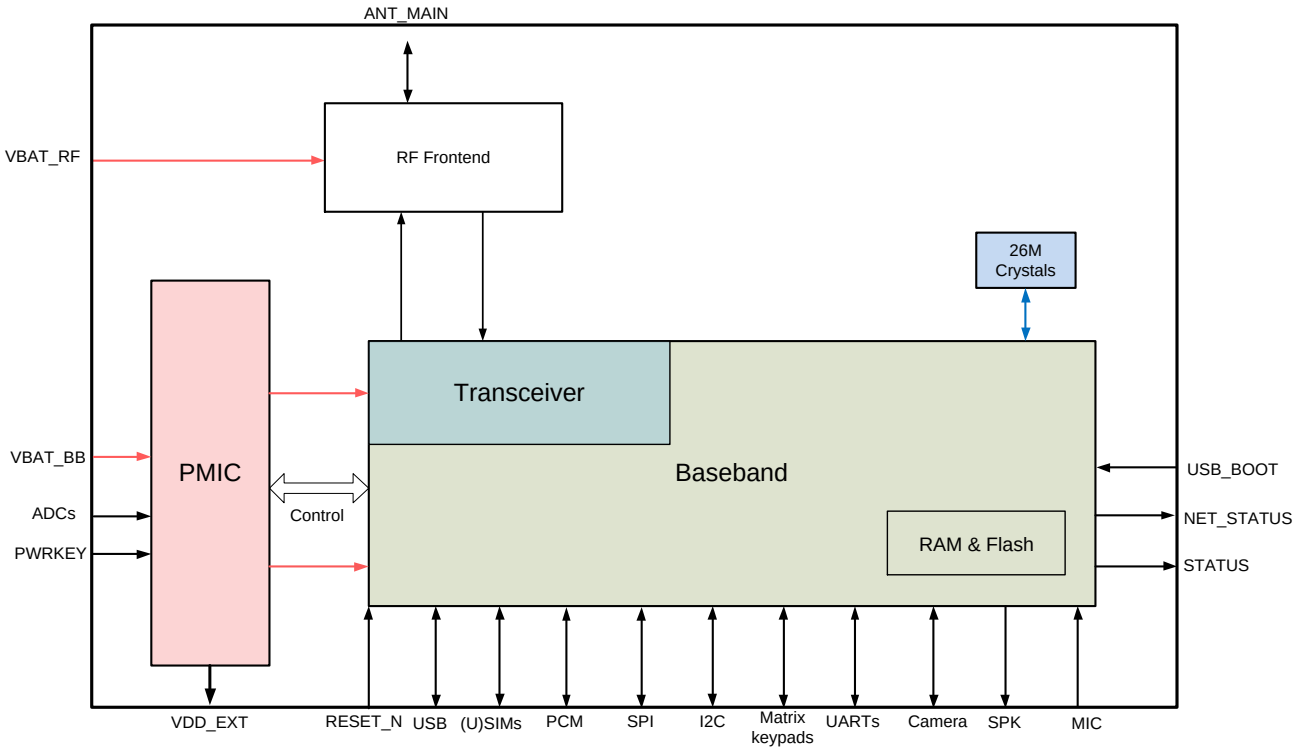


Figure 1: Functional Diagram

2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

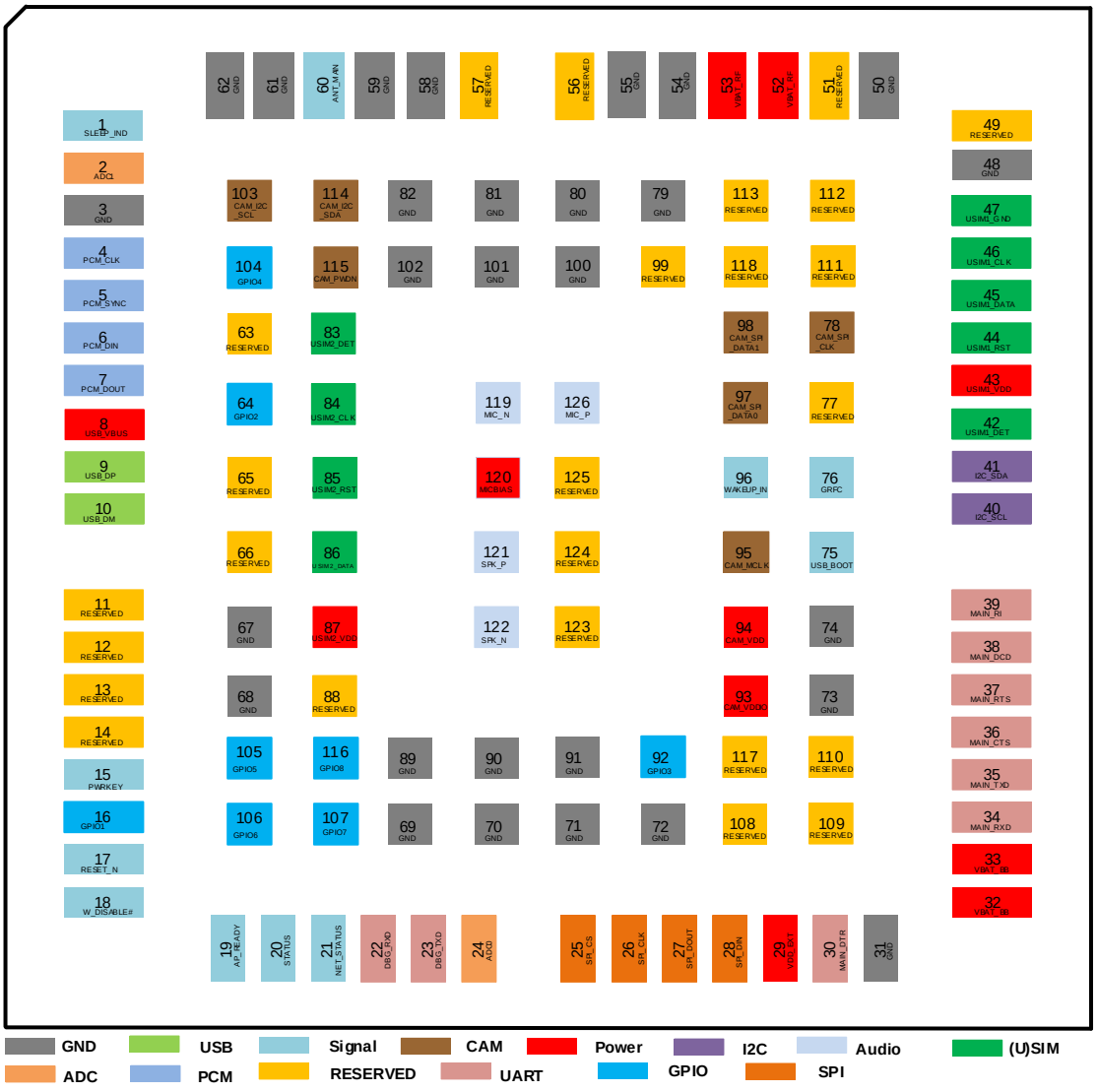


Figure 2: Pin Assignment (Top View)

NOTE

1. All GND pins should be connected to ground, and keep unused and RESERVED pins open.
2. USB_BOOT cannot be pulled up to high level before the module starts up successfully.
3. Ensure that there is a complete reference ground plane under the module, and the plane should be placed as close to the module layer as possible. Ensure that there is no other traces on the first layer under the module. And at least a 4-layer board design is recommended.

2.5. Pin Description

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current, etc.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.4 V Vnom = 3.8 V	External power supply must be provided with sufficient current of at least 0.8 A. It is recommended to add a TVS diode externally. A test point is recommended to be reserved.
VBAT_RF	52, 53	PI	Power supply for the module's RF part		External power supply must be provided with sufficient current of at least 2.2 A. It is

					recommended to add a TVS diode externally. A test point is recommended to be reserved.
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
Turn On/Off/Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module	V_{IL}max = 0.5 V	VBAT power domain. A test point is recommended to be reserved.
RESET_N	17	DI	Reset the module		Active low. 1.8 V power domain. A test point is recommended to be reserved if unused.
Indication Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicate the module's operation status	1.8 V	If unused, keep them open.
NET_STATUS	21	DO	Indicate the module's network activity status		
SLEEP_IND	1	DO	Indicate the module's sleep mode		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V	A test point must be reserved.

				Vnom = 5.0 V	
USB_DP	9	AIO	USB differential data (+)		Requires differential impedance of 90 Ω. USB 2.0 compliant. Test points must be reserved.
USB_DM	10	AIO	USB differential data (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V	If unused, keep it open.
USIM1_VDD	43	PO	(U)SIM1 card power supply	1.8/3.0 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_RST	44	DO	(U)SIM1 card reset		
USIM1_DATA	45	DIO	(U)SIM1 card data		
USIM1_CLK	46	DO	(U)SIM1 card clock		
USIM1_GND	47	-	Specified ground for (U)SIM1		Connect to main GND of the PCB
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	1.8 V	If unused, keep it open.
USIM2_CLK	84	DO	(U)SIM2 card clock	1.8/3.0 V	
USIM2_RST	85	DO	(U)SIM2 card reset		
USIM2_DATA	86	DIO	(U)SIM2 card data		
USIM2_VDD	87	PO	(U)SIM2 card power supply		Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_DTR	30	DI	Main UART data terminal ready	1.8 V	If unused, keep them open.
MAIN_RXD	34	DI	Main UART receive		

MAIN_TXD	35	DO	Main UART transmit		
MAIN_CTS	36	DO	Clear to send signal from the module		Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	37	DI	Request to send signal to the module		Connect to MCU's RTS. If unused, keep it open.
MAIN_DCD	38	DO	Main UART data carrier detect		If unused, keep them open.
MAIN_RI*	39	DO	Main UART ring indication		
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART receive	1.8 V	Test points must be reserved.
DBG_TXD	23	DO	Debug UART transmit		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	40	OD	I2C serial clock		An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK	4	DO	PCM clock	1.8 V	If unused, keep them open.
PCM_SYNC	5	DO	PCM data frame sync		
PCM_DIN	6	DI	PCM data input		
PCM_DOUT	7	DO	PCM data output		
Camera Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CAM_MCLK	95	DO	Master clock of camera	1.8 V	If unused, keep it open.

CAM_I2C_SCL	103	OD	I2C clock of camera		Pull each of them up to 1.8 V power domain with external resistors. If unused, keep them open.
CAM_I2C_SDA	114	OD	I2C data of camera		
CAM_SPI_CLK	78	DI	SPI clock of camera		If unused, keep them open.
CAM_SPI_DATA0	97	DI	SPI data bit 0		
CAM_SPI_DATA1	98	DI	Camera SPI data bit 1 of camera		
CAM_PWDN	115	DO	Power down of camera		
CAM_VDD	94	PO	Analog power supply of camera	Vnom = 2.8 V	Power supply of camera. If unused, keep them open.
CAM_VDDIO	93	PO	Digital power supply of camera	Vnom = 1.8 V	
SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	25	DIO	SPI chip select	1.8 V	If unused, keep them open. When the module is used as master device, SPI_CS and SPI_CLK pins are output signals; when the module is used as slave device, SPI_CS and SPI_CLK pins are input signals.
SPI_CLK	26	DIO	SPI clock		
SPI_DOUT	27	DO	SPI data output		
SPI_DIN	28	DI	SPI data input		
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface		50 Ω impedance.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0 V–VBAT_BB	If unused, keep them open.
ADC1	2	AI			

Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	75	DI	Force the module into emergency download mode	1.8 V	Active high. A test point is recommended to be reserved.
W_DISABLE#*	18	DI	Airplane mode control		Pull-up by default. In low voltage level, the module can enter airplane mode.
WAKEUP_IN*	96	DI	Wake up the module		If unused, keep them open.
AP_READY*	19	DI	Application processor ready		
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MICBIAS	120	PO	Bias voltage output for microphone		If unused, keep them open.
MIC_N	119	AI	Microphone analog input (-)		
MIC_P	126	AI	Microphone analog input (+)		
SPK_P	121	AO	Analog audio differential output (+)		The interface can drive 32 Ω earpiece with power rate at 37 mW @ THD = 1 %. It can also be used to drive external power amplifier devices if the output power rate cannot meet the demand. If unused, keep them open.
SPK_N	122	AO	Analog audio differential output (-)		
Antenna Tuner Control Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC	76	DO	Generic RF controller		If unused, keep it open.
GPIO Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GPIO1	16	DIO	General-purpose input/output	1.8 V	If unused, keep them open.
GPIO2	64	DIO			
GPIO3	92	DIO			
GPIO4	104	DIO			
GPIO5	105	DIO			
GPIO6	106	DIO			
GPIO7	107	DIO			
GPIO8	116	DIO			
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	11–14, 49, 51, 56, 57, 63, 65, 66, 77, 88, 99, 108–113, 117, 118, 123–125				Keep them open.

NOTE

For more information about GPIO, see ***document [2]*** for details.

2.6. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (LTE OPEN EVB) with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module is registered on the network and ready to send and receive data.
	Voice/Data	Network connection is ongoing. Power consumption is decided by the network setting and data transmission rate.
Minimum Functionality Mode	*ql_dev_set_modem_fun()* can set the module to a minimum functionality mode. Both RF function and (U)SIM card will be invalid.	
Airplane Mode	*ql_dev_set_modem_fun()* can set the module to airplane mode. RF function will be invalid.	
Sleep Mode	Power consumption of the module will be reduced to a minimal level. The module can still receive paging, SMS, voice call and TCP/UDP data from network.	
Power Down Mode	PMIC shuts down the power supply. Software is not active. However, operating voltage connected to VBAT_BB/RF remains applied.	

NOTE

For more details about AT command, see ***document [2]***.

3.2. Sleep Mode

With DRX technology, power consumption of the module can be reduced to a minimal level.

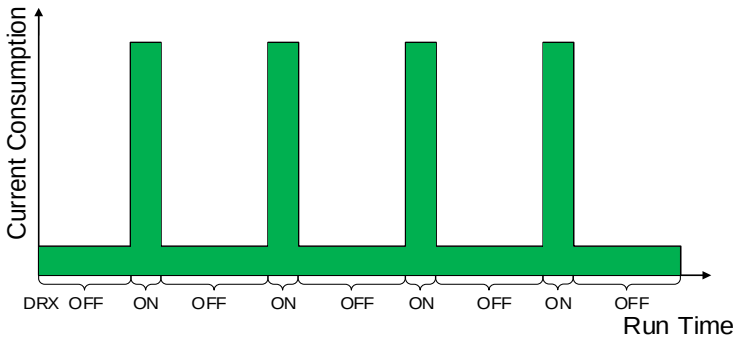


Figure 3: DRX Run Time and Current Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

The following three conditions should be met to set the module into sleep mode.

- Enable sleep function through *ql_autosleep_enable()*.
- All GPIOs which can be configured as interrupt wake-up function are in non-wake-up state.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

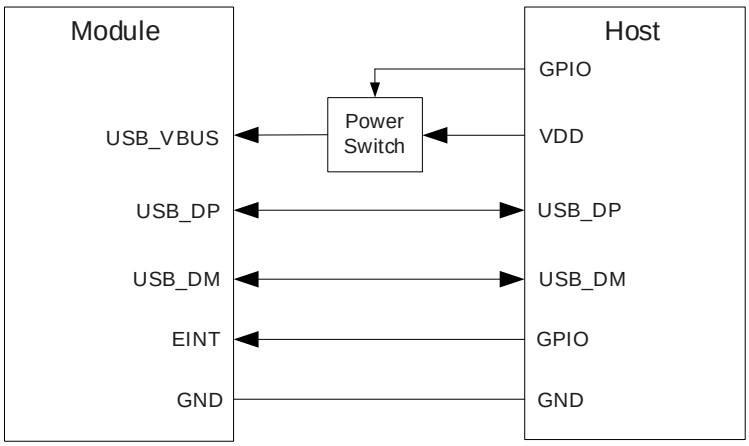


Figure 4: Sleep Mode Application without Suspend Function

You can wake up the module by turning on the power switch to power the USB_VBUS or by using GPIO to interrupt the module.

NOTE

1. Pay attention to the level matching shown in dotted line between the module and the host in the circuit diagrams.
2. For more information about the API, see ***document [3]*** for details.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following way.

Software:

ql_dev_set_modem_fun() provides choices of the functionality level through setting parameter *function* into 0, 1 or 4.

- *QL_DEV_MODEM_MIN_FUN*: Minimum functionality (disable RF function and (U)SIM function).
- *QL_DEV_MODEM_FULL_FUN*: Full functionality (default).
- *QL_DEV_MODEM_DISBLE_TRANSMIT_AND_RECEIVE_RF_CIRCUITS*: Airplane mode (disable RF transmitter and receiver circuits).

NOTE

For more information about the API, see ***document [2]*** for details.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides four VBAT pins dedicated to the connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for RF part.
- Two VBAT_BB pins for baseband part.

Table 8: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	External power supply must be provided with sufficient current of at least 0.8 A. It is recommended to add a TVS diode externally. A test point is recommended to be reserved.
VBAT_RF	52, 53	PI	Power supply for the module's RF part	External power supply must be provided with sufficient current of at least 2.2 A. It is recommended to add a TVS diode externally. A test point is recommended to be reserved.

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of at least 3 A. If the voltage drops between input and output is not too high, it is suggested to use an LDO for the module. If the voltage difference is large, then a buck converter is suggested to use.

The following figure illustrates a reference design for +5 V input power source.

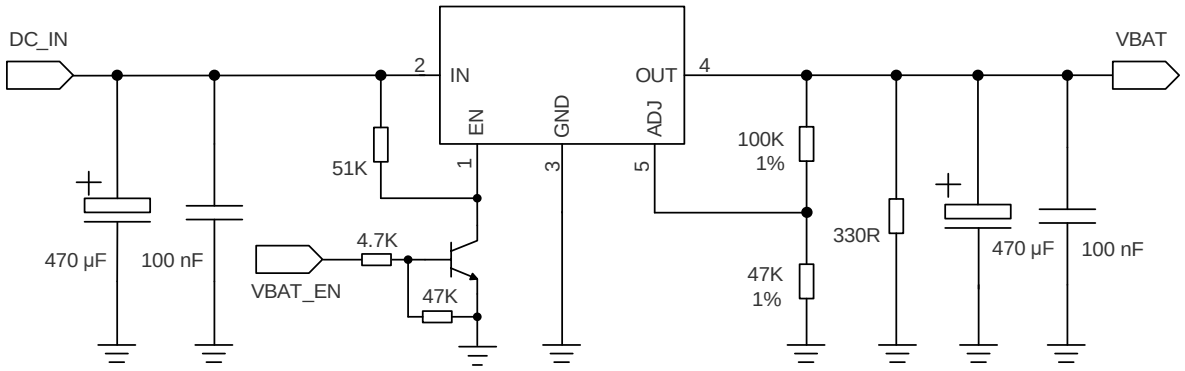


Figure 5: Reference Design of Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not cut off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.4 V to 4.3 V. Please make sure the input voltage will never drop below 3.4 V.

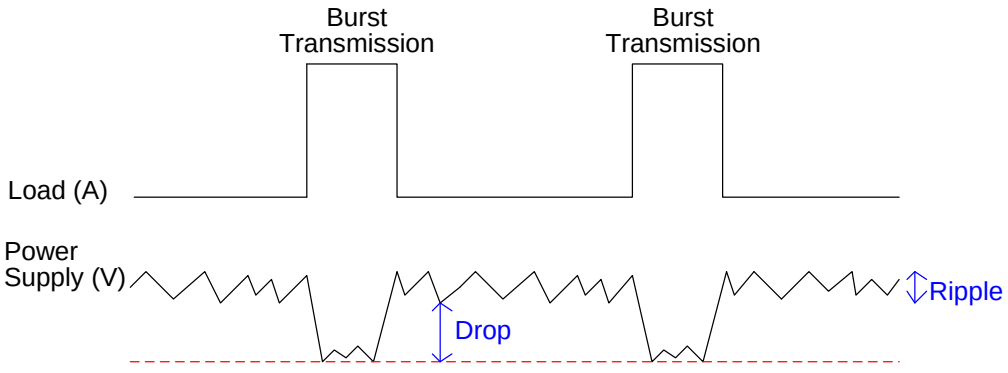


Figure 6: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 μF with low ESR (ESR ≤ 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved with ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source and can be expanded to two sub paths with the star configuration. The width of VBAT_BB trace should not be less than 1 mm. The width of VBAT_RF trace should not be less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, to ensure the stability of the power supply, it is necessary to add a high-power TVS diode at the front end of the power supply. Reference circuit is shown as below:

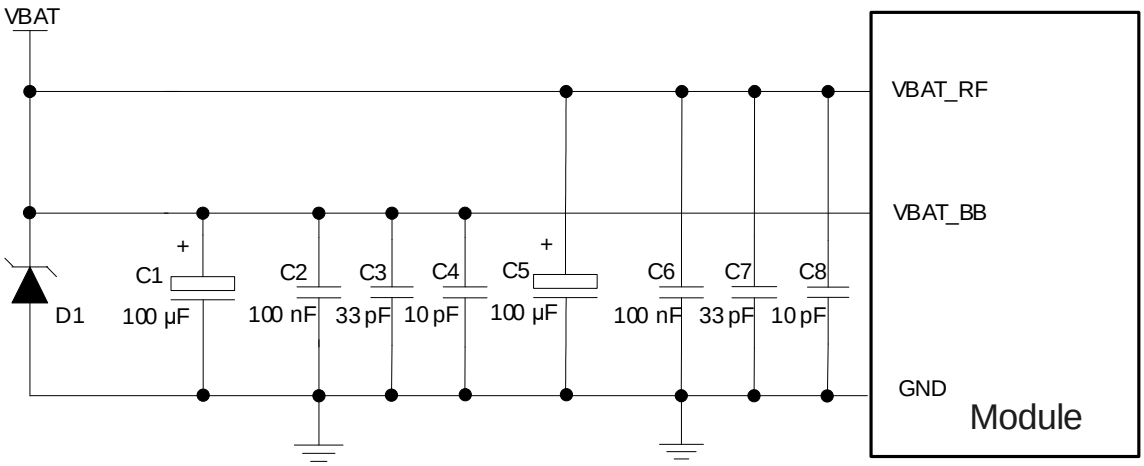


Figure 7: Reference Design of Power Supply

3.5. Turn On

3.5.1. Turn on with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	VBAT power domain. A test point is recommended to be reserved.

When the module is in power down mode, it can be turned on and enter normal operation mode by driving the PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

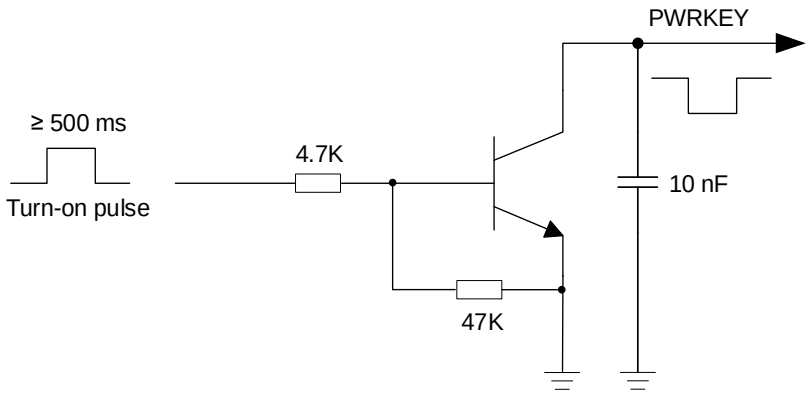


Figure 8: Reference Circuit of Turing on with Driving Circuit

Another way to control the PWRKEY is by using a button directly. When pressing the button, an electrostatic strike may be generated from finger. Therefore, a TVS diode shall be placed near the button for ESD protection.

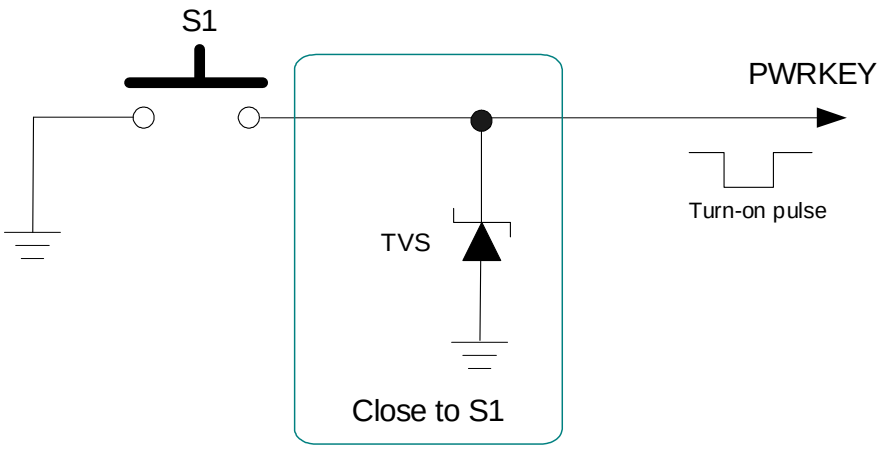


Figure 9: Reference Circuit of Turning on with a Button

The turn-on scenario is illustrated in the following figure.

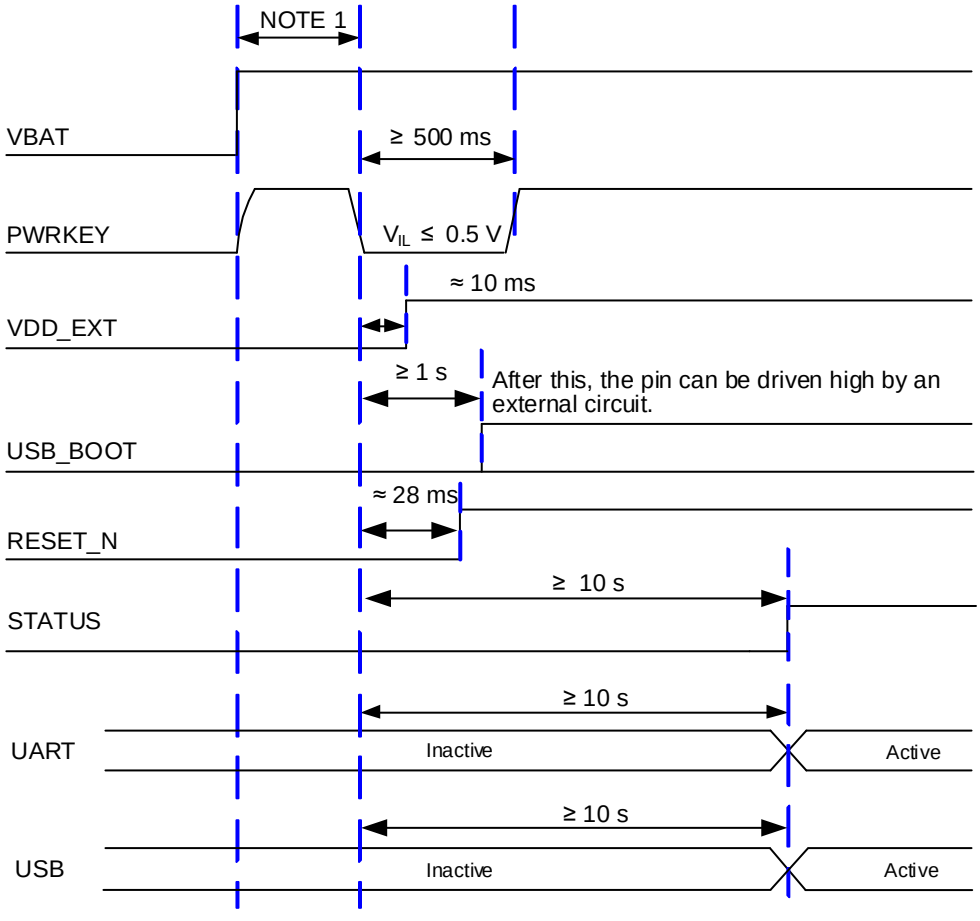


Figure 10: Timing Sequence of Turning on with PWRKEY

NOTE

1. Ensure that VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to turn on automatically while does not need turn-off function, PWRKEY can be driven low directly to GND with a recommended 4.7 kΩ resistor.

3.6. Turn Off

3.6.1. Turn off with PWRKEY

Driving the PWRKEY to a low-level voltage for at least 650 ms, then the module will execute power-down procedure after the PWRKEY is released.

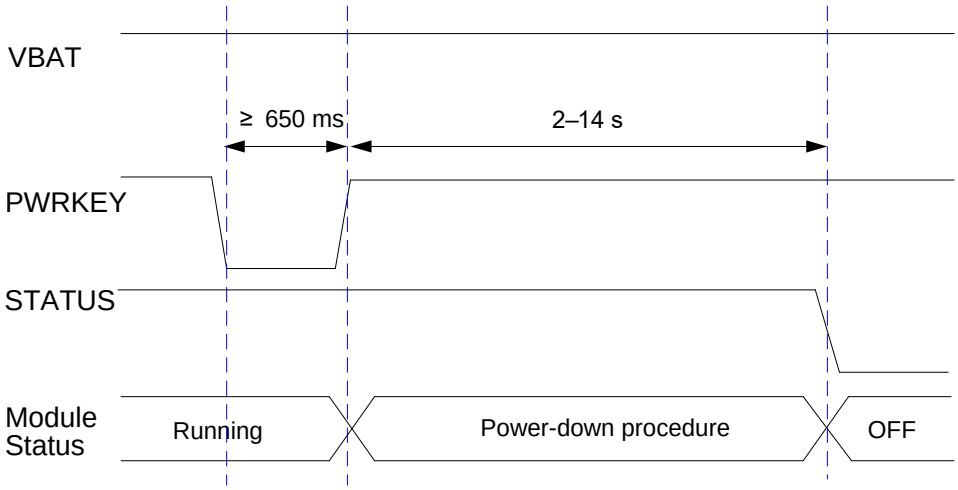


Figure 11: Timing Sequence of Turning off with PWRKEY

3.6.2. Turn off with API

It is also a safe way to use the *ql_power_down()* to turn off the module, which is similar to turning off the module via PWRKEY pin. See ***document [4]*** for details about the API.

NOTE

1. To avoid corrupting the data in the internal flash, do not cut off the power supply when the module works normally. Only after turning offthe module with PWRKEY or API, can you cut off the power supply.
2. When turning off module with the API, keep PWRKEY at high level. Otherwise, the module will be turned on automatically again after successfully turn-off.

3.7. Reset

Driving the RESET_N low for at least 300 ms and then releasing it can reset the module. RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Reset the module	Active low. 1.8 V power domain. A test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

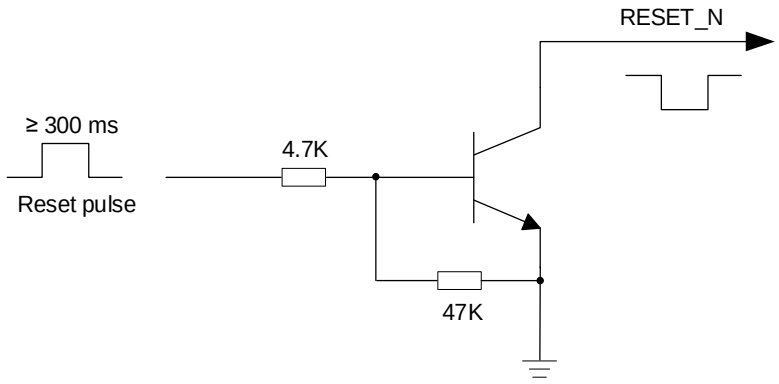


Figure 12: Reference Circuit of RESET_N with Driving Circuit

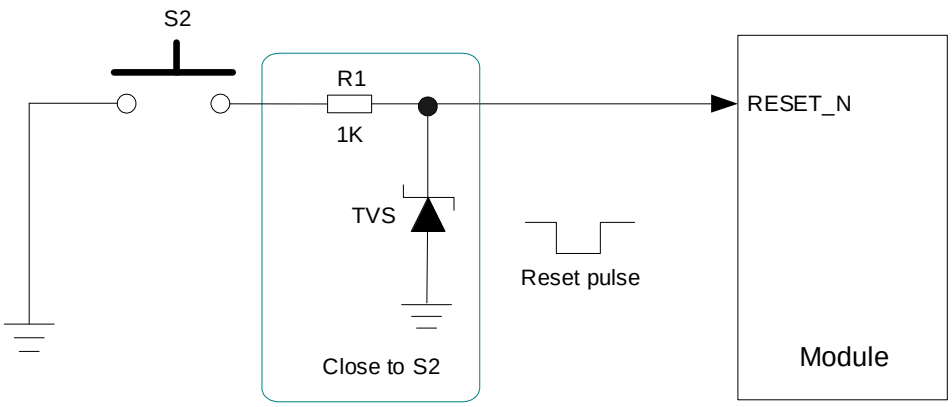


Figure 13: Reference Design Circuit of RESET_N with a Button

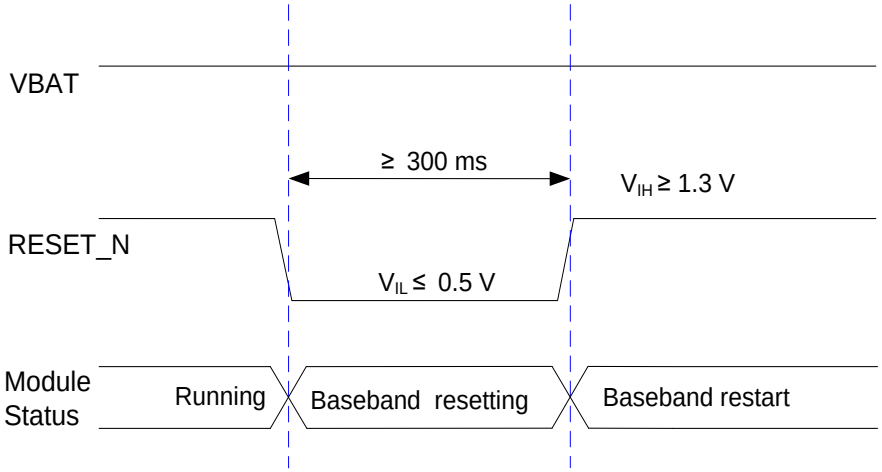


Figure 14: Timing Sequence of RESET_N

NOTE

1. Ensure that the capacitance on PWRKEY and RESET_N does not exceed 10 nF.
2. RESET_N only resets the internal baseband chip of the module and does not reset the power management chip.
3. Use RESET_N only when you fail to turn off the module with the API and PWRKEY.

4 Application Interfaces

4.1. USB Interface

The module provides one USB interface, which complies with USB 2.0 specifications, and supports high-Speed (480 Mbps) and full-Speed (12 Mbps) on USB 2.0. Only slave mode is supported. The USB interface can be used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	A test point must be reserved.
USB_DP	9	AIO	USB differential data (+)	Requires differential impedance of 90 Ω. USB 2.0 compliant. Test points must be reserved.
USB_DM	10	AIO	USB differential data (-)	

Reserve test points for debugging and firmware upgrading in your designs.

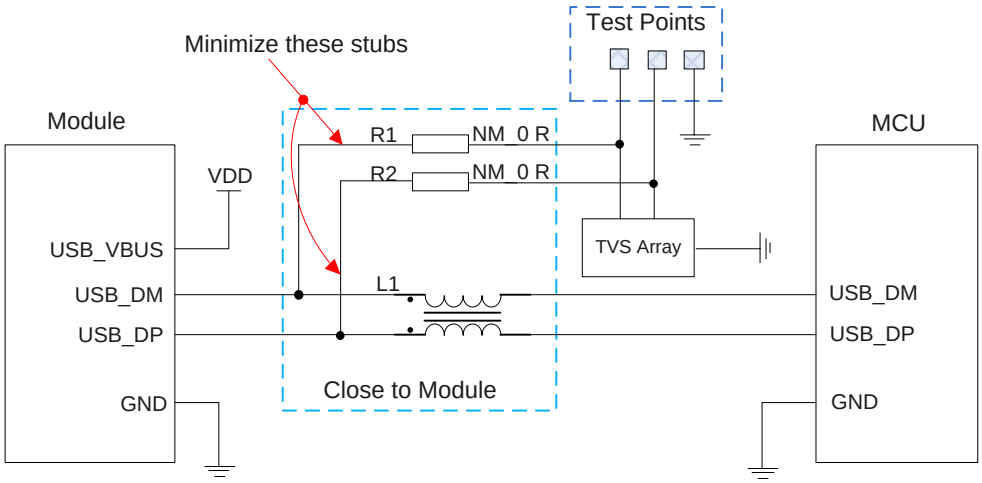


Figure 15: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU in order to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. To ensure the integrity of USB data trace signal, L1, R1 and R2 components must be placed close to the module, and resistors R1 and R2 should be placed close to each other. The extra stubs of trace should be kept as short as possible.

The following principles should be complied with when designing the USB interface to meet USB specifications.

- The impedance of USB differential trace is 90 Ω. Route USB differential traces in the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Do not route signal traces under VBAT traces, crystal-oscillators, magnetic devices, sensitive circuits and provide clearance from RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Pay attention to the selection of the ESD protection component on the USB data traces. Its parasitic capacitance should not exceed 2 pF and should be placed as close as possible to the USB interface.

For more details about the USB specifications, please visit http://www.usb.org/home.

4.2. USB_BOOT

The module provides a USB_BOOT pin. You can pull it up to 1.8 V or short-circuit VDD_EXT and USB_BOOT before turning on the module, thus the module will enter emergency download mode when it is turned on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 12: Pin Definition of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module into emergency download mode	1.8 V power domain. Active high. A test point is recommended to be reserved.

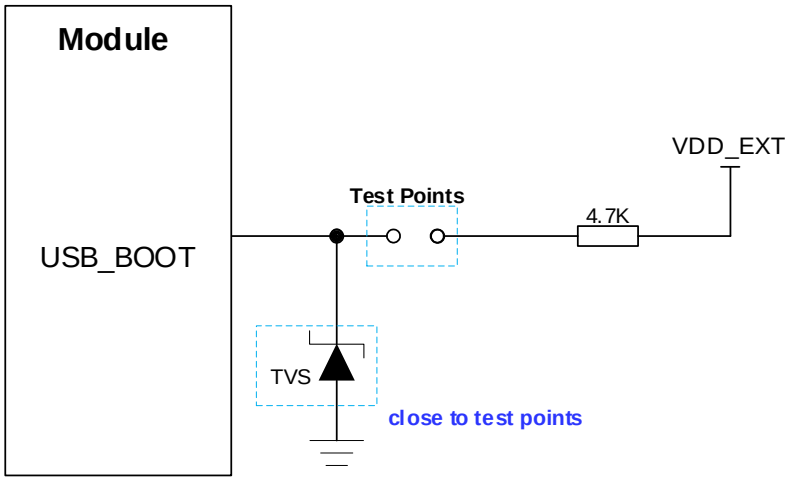


Figure 16: Reference Circuit of USB_BOOT

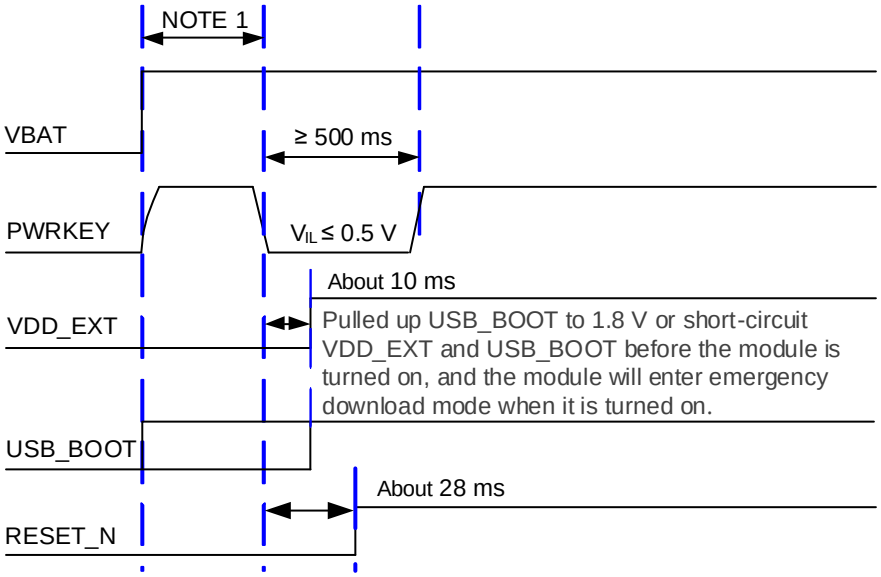


Figure 17: Timing Sequence for Entering Emergency Download Mode

NOTE

1. Ensure that VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low should be at least 30 ms.
2. When using MCU to control module to enter the emergency download mode, follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Connect the test points as shown in ***Figure 16*** can manually force the module to enter emergency download mode.

4.3. (U)SIM Interfaces

The circuit of (U)SIM interfaces meet ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported.

Table 13: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_GND	47	-	Specified ground for (U)SIM1	Connect to main GND of the PCB.
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_DATA	86	DIO	(U)SIM2 card data	
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.

The module supports USIM card hot-plug detection via the USIM_DET pin and both high- and low- level detections are supported. The function is disabled by default.

The following figure illustrates a reference design for (U)SIM card interface with an 8-pin (U)SIM card connector.

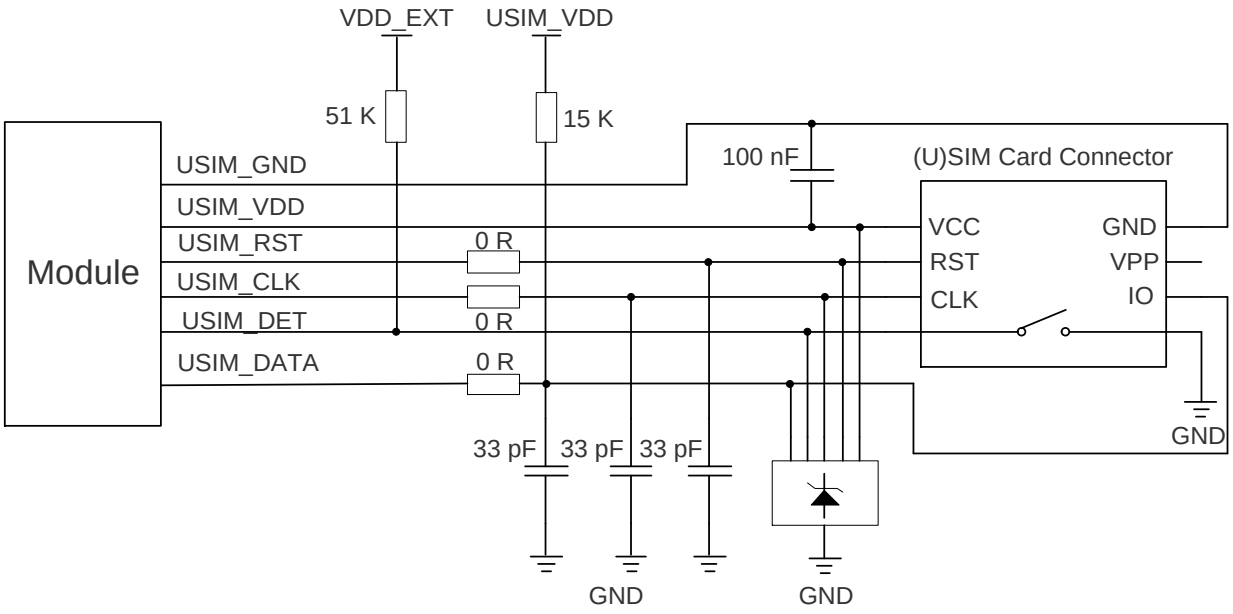


Figure 18: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card hot-plug detection function is not needed, keep USIM_DET open.

A reference design for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

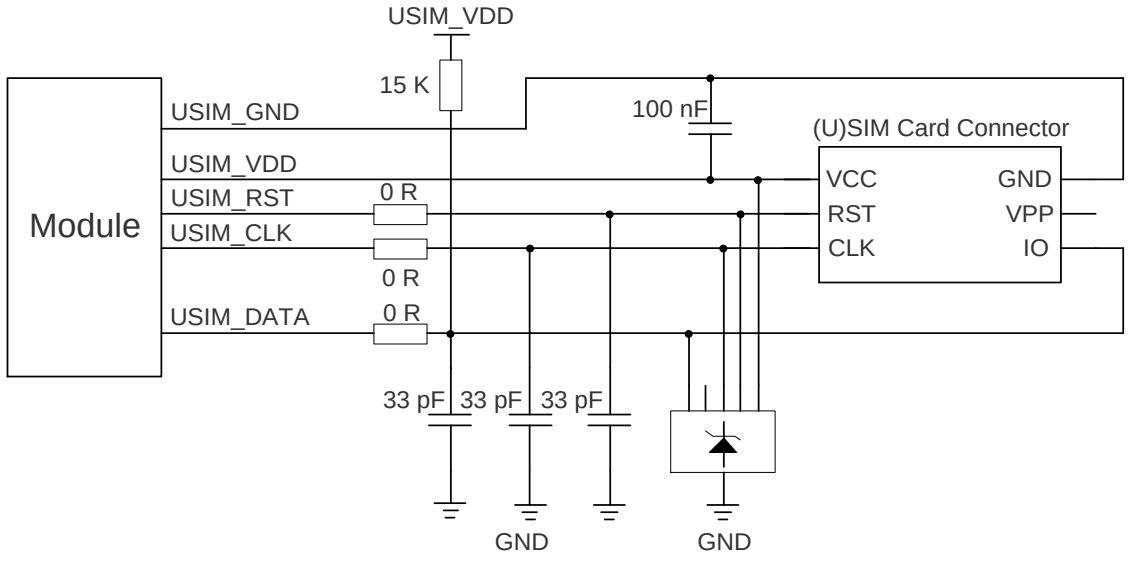


Figure 19: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in the (U)SIM circuit design:

- Place (U)SIM card connector close to the module. Keep the trace length less than 200 mm if possible. Keep (U)SIM card signals away from RF and power signals.
- Ensure the bypass capacitor between USIM_VDD and USIM_GND less than 1 μF, and place it close to the (U)SIM card connector.
- Ensure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential. If the ground is complete on your PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS array of which parasitic capacitance should be less than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The 33 pF capacitors in parallel on USIM_DATA, USIM_CLK and USIM_RST lines are used for filtering RF interference.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the USIM card connector.

4.4. UART

The module provides three UART: Main UART, debug UART and auxiliary UART, among which the auxiliary UART function can be realized by multiplexing SPI_DOUT and MAIN_CTS, or SPI_DIN and MAIN_RTS. The following shows their features:

Table 14: UART Information

UART types	Supported Baud rates	Default Baud rates	Functions
Main UART	4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps and 1 Mbps	115200 bps	Data transmission and AT command communication
Debug UART	115200 bps	115200 bps	Log output
Auxiliary UART	4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps and 1 Mbps	115200 bps	Communication with peripherals

Table 15: Pin Definition of UART

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
MAIN_DTR	30	-	DI	Main UART data terminal ready	1.8 V power domain. If unused, keep them open.
MAIN_RXD	34	-	DI	Main UART receive	
MAIN_TXD	35	-	DO	Main UART transmit	
MAIN_CTS	36	-	DO	Clear to send signal from the module	1.8 V power domain. Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	37	-	DI	Request to send signal to the module	1.8 V power domain. Connect to MCU's RTS. If unused, keep it open.
MAIN_DCD	38	-	DO	Main UART data carrier detect	1.8 V power domain. If unused, keep them open.
MAIN_RI*	39	-	DO	Main UART ring indication	
DBG_RXD	22	-	DI	Debug UART receive	1.8 V power domain. Test points must be reserved.
DBG_TXD	23	-	DO	Debug UART transmit	
SPI_DOUT/ MAIN_CTS	27/36	UART3_TXD	DO	Auxiliary UART transmit	1.8 V power domain. If unused, keep them open.
SPI_DIN/ MAIN_RTS	28/37	UART3_RXD	DI	Auxiliary UART receive	

The module provides 1.8 V UART. A voltage-level translator should be used between the module and MCU's UART if the application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by *Texas Instruments* is recommended.

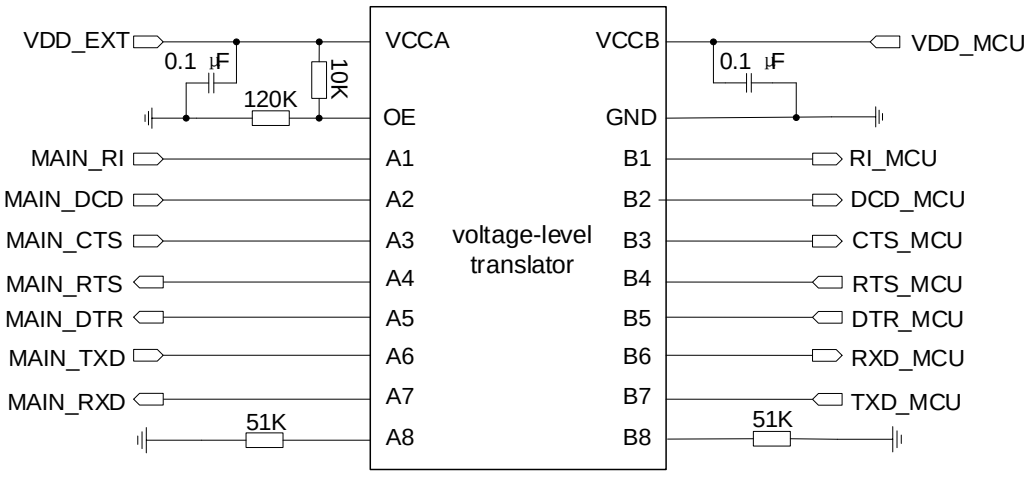


Figure 20: Reference Circuit with a Voltage-level Translator

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, please refer to that shown in solid lines, but pay attention to the direction of connection.

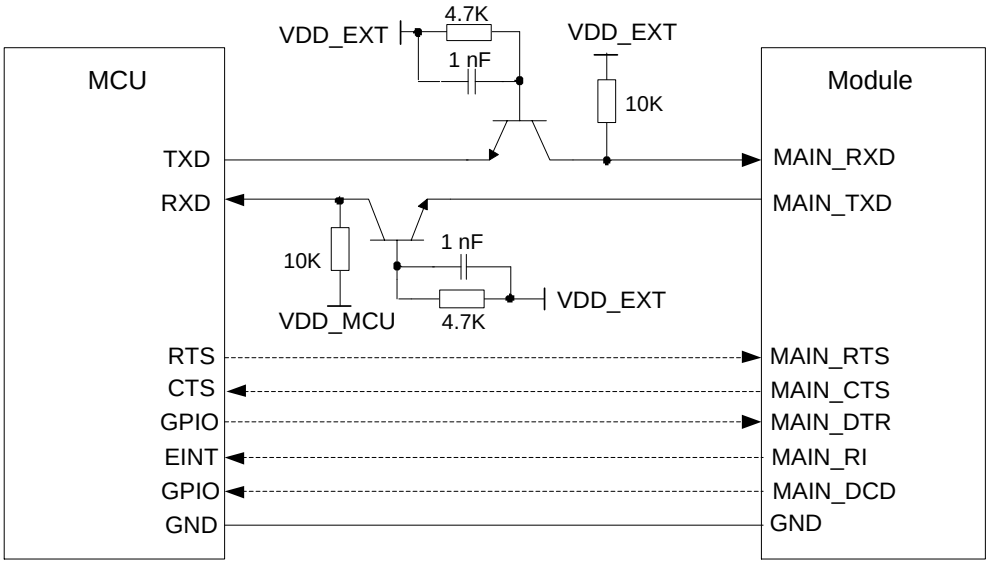


Figure 21: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to MCU's CTS, and the module's RTS is connected to MCU's RTS.
3. For details about multiplexing information, see ***document [5]***.

4.5. PCM and I2C Interfaces

The module provides one PCM interface and one I2C interface.

Table 16: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_CLK	4	DO	PCM clock	1.8 V power domain. If unused, keep them open.
PCM_SYNC	5	DO	PCM data frame sync	
PCM_DIN	6	DI	PCM data input	
PCM_DOUT	7	DO	PCM data output	

Table 17: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	40	OD	I2C serial clock	An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data	

PCM interface supports short frame mode, module can only be used as the master device.

The module supports 16-bit linear encoding format. The following figure is the short frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 2048 kHz).

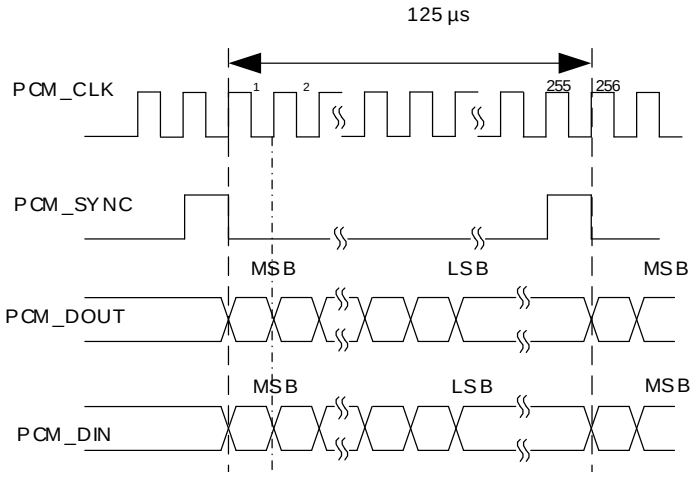


Figure 22: Timing of Short Frame Mode

In short frame mode, data is sampled on the falling edge of PCM_CLK, and sent on the rising edge. The falling edge of PCM_SYNC represents the high effective bit. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz, and 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

The default configuration is short frame mode, PCM_CLK = 2048 kHz, PCM_SYNC =8 kHz.

The following figure shows a reference design of I2C and PCM interfaces with an external codec IC.

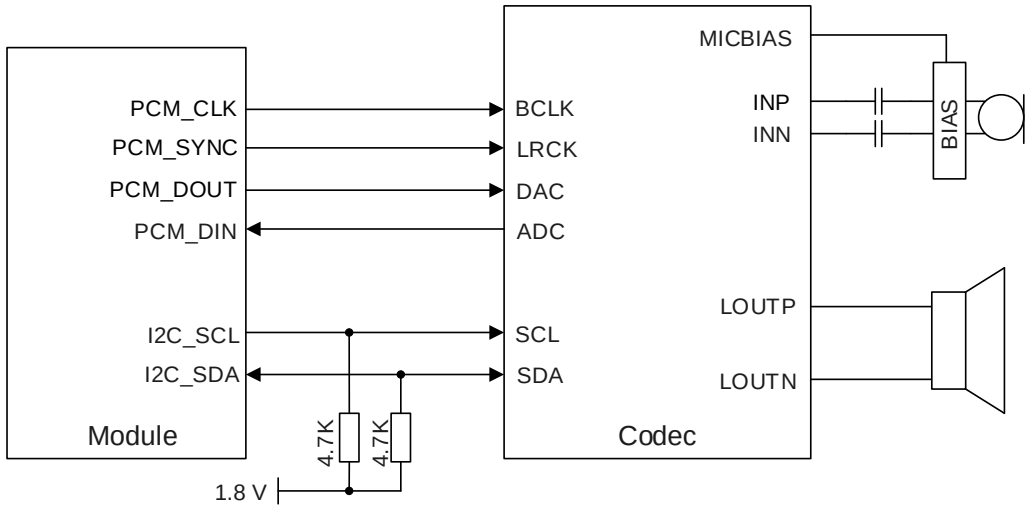


Figure 23: Reference Circuit of PCM and I2C Application with Audio Codec

NOTE

1. It is recommended to reserve an RC (R = 0 Ω, C = 33 pF) circuit on the PCM lines, especially for PCM_CLK.
2. The module can only be used as a master device in applications related to PCM and I2C interfaces.

4.6. Analog Audio Interfaces

The module provides one analog input channel and one analog output channel.

Table 18: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MICBIAS	120	PO	Bias voltage output for microphone	If unused, keep them open.
MIC_P	126	AI	Microphone analog input (+)	
MIC_N	119	AI	Microphone analog input (-)	
SPK_P	121	AO	Analog audio differential output (+)	The interface can drive 32 Ω earpiece with power rate at 37 mW @ THD = 1 %. It can also be used to drive
SPK_N	122	AO	Analog audio differential output (-)	

	external power amplifier devices if the output power rate cannot meet the demand. If unused, keep them open.

- AI channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- AO channels are differential output channels, which can be applied for output of earpiece.

4.6.1. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) for filtering out RF interference, thus reducing noise. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required. The filter capacitor on the PCB should be placed as close as possible to the audio device or audio interface, and the wiring should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To decrease signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces cannot be parallel, and they should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

4.6.2. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure.

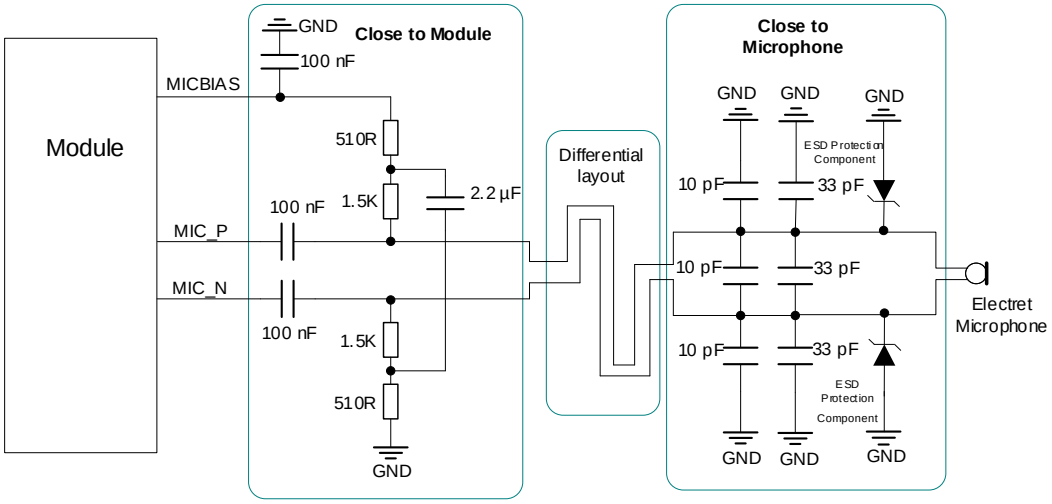


Figure 24: Reference Circuit for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD protection components used for protecting the MIC.

4.6.3. Earpiece and Loudspeaker Interface Design

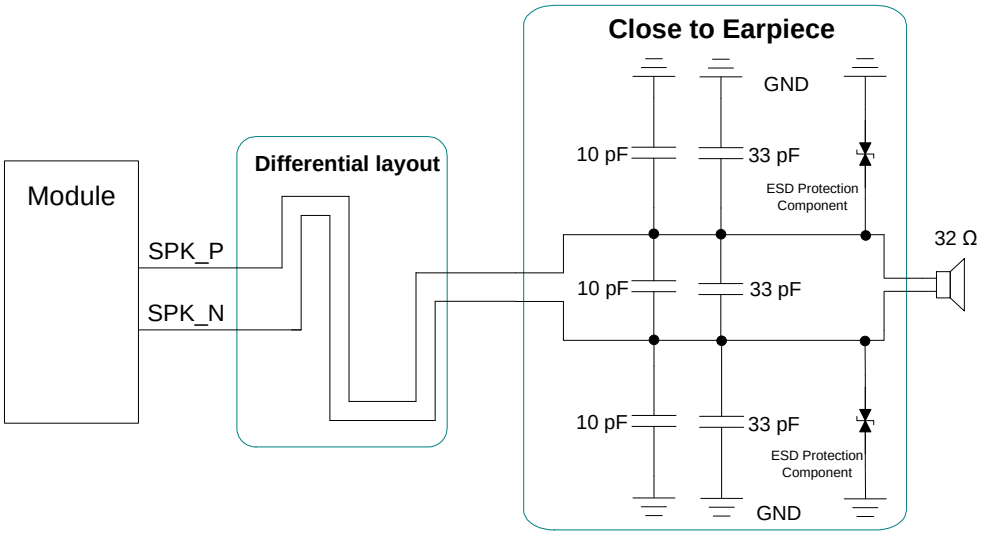


Figure 25: Reference Circuit for Earpiece Interface

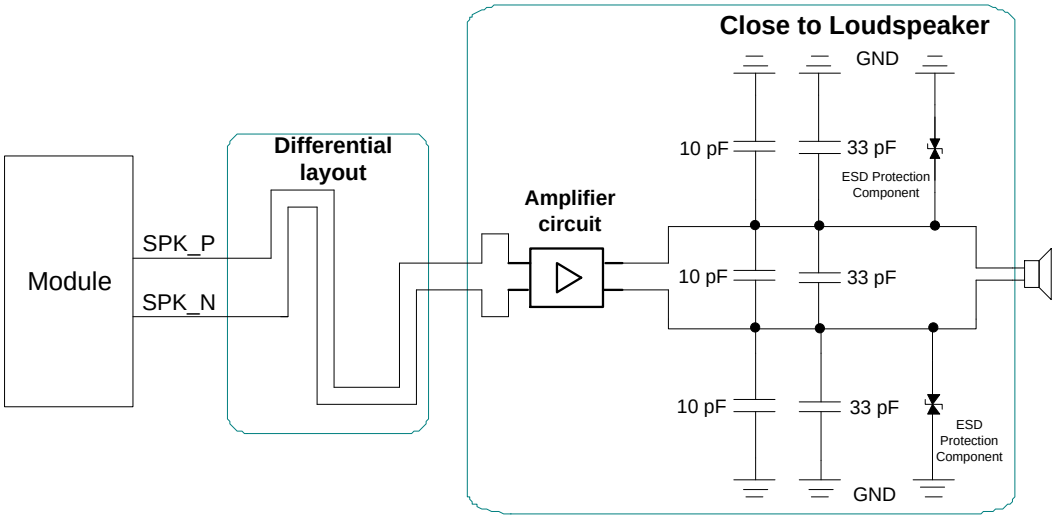


Figure 26: Reference Circuit of External Audio Amplifier Output

For differential input and output audio power amplifiers, please visit http://www.ti.com to obtain the required devices. There are also many audio power amplifiers with the same performance to choose from on the market.

4.7. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. You can use the *ql_adc_read()* to read the voltage value of the ADC. See ***document [6]*** for details about the API.

To improve the accuracy of ADC, surround the trace of ADC with ground.

Table 19: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	2	AI		

Table 20: Characteristics of ADC Interface

Name	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	VBAT_BB	V
ADC1 Voltage Range	0	-	VBAT_BB	V
ADC Resolution	-	12	-	bits

NOTE

1. The input voltage of ADC should not exceed its voltage range.
2. It is prohibited to directly supply any voltage to ADC interface when the module is not powered by the VBAT.
3. If the collected voltage is greater than VBAT_BB, it is recommended to use a resistor divider circuit input for the ADC pin. When designing it, reserve a 1 nF capacitor at both ends of the grounding divider resistor. The capacitor is not mounted by default.

4.8. Camera Interface

The module provides one camera interface, supports up to 0.3 MP and supports single data line or dual data line transmission of SPI.

Table 21: Pin Definition of Camera Interface

Pin Name	Pin No.	I/O	Description	Comment
CAM_MCLK	95	DO	Master clock of camera	1.8 V power domain. If unused, keep it open.
CAM_I2C_SCL	103	OD	I2C clock of camera	Pull each of them up to 1.8 V power domain with external resistors. If unused, keep them open.
CAM_I2C_SDA	114	OD	I2C data of camera	
CAM_SPI_CLK	78	DI	SPI clock of camera	1.8 V power domain. If unused, keep them open.
CAM_SPI_DATA0	97	DI	SPI data 0 of camera	
CAM_SPI_DATA1	98	DI	SPI data 1 of camera	
CAM_PWDN	115	DO	Power down of camera	

CAM_VDD	94	PO	Analog power supply of camera	Power supply of camera. If unused, keep them open.
CAM_VDDIO	93	PO	Digital power supply of camera	

4.9. SPI

The module provides one SPI which supports master and slave modes with a maximum clock frequency up to 26 MHz.

Table 22: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CS	25	DIO	SPI chip select	1.8 V power domain. If unused, keep them open. When the module is used as master device, SPI_CS and SPI_CLK pins are output signals; when the module is used as slave device, SPI_CS and SPI_CLK pins are input signals.
SPI_CLK	26	DIO	SPI clock	
SPI_DOUT	27	DO	SPI data output	
SPI_DIN	28	DI	SPI data input	

The following figure shows reference circuits of SPI.

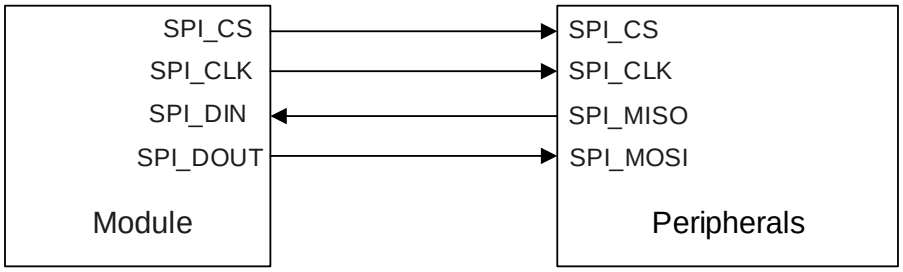


Figure 27: Reference Circuit of SPI (Module as Master Device)

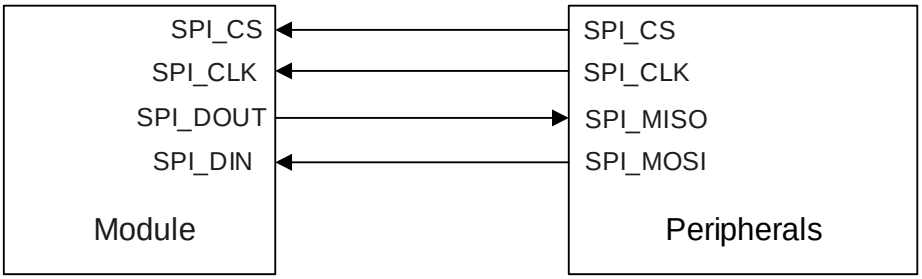


Figure 28: Reference Circuit of SPI (Module as Slave Device)

4.10. Matrix Keypad Interfaces

The module supports 3 × 3 matrix keypad interface, which can be multiplexed by STATUS, SLEEP_IND, NET_STATUS and GPIO interfaces.

Table 23: Pin Definition of Matrix Keypad Interfaces

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
SLEEP_IND	1	KP_MKIN[4]	DI	Matrix keypad input 4	1.8 V power domain. If unused, keep them open.
GPIO1	16	KP_MKOUT[2]	DO	Matrix keypad output 2	
STATUS	20	KP_MKOUT[1]	DO	Matrix keypad output 1	
NET_STATUS	21	KP_MKIN[3]	DI	Matrix keypad input 3	
GPIO5	105	KP_MKIN[2]	DI	Matrix keypad input 2	
GPIO8	116	KP_MKOUT[3]	DO	Matrix keypad output 3	

NOTE

1. KP_MKIN can be used with KP_MKOUT flexibly, such as KP_MKIN[1] used with KP_MKOUT[2].
2. For more information, see ***document [5]***.

4.11. Indication Signal

Relative interfaces' pin descriptions are here as follows:

Table 24: Pin Definition of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	21	DO	Indicate the module's network activity status	1.8 V power domain. If unused, keep them open.
STATUS	20	DO	Indicate the module's operation status	

4.11.1. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides one network indication pin: NET_STATUS. The following tables describe pin definition and logic level changes in different network status.

Table 25: Working State of the Network Connection Status/Activity Indication

Pin Name	Status	Description
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transmission is ongoing
	Always High	Voice calling

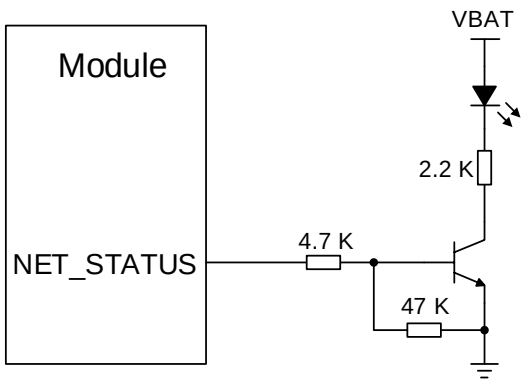


Figure 29: Reference Circuit of the Network Status Indication

4.11.2. STATUS

The STATUS pin indicates the module's operation status. It will output high level when module is turned on successfully.

A reference circuit is shown as below.

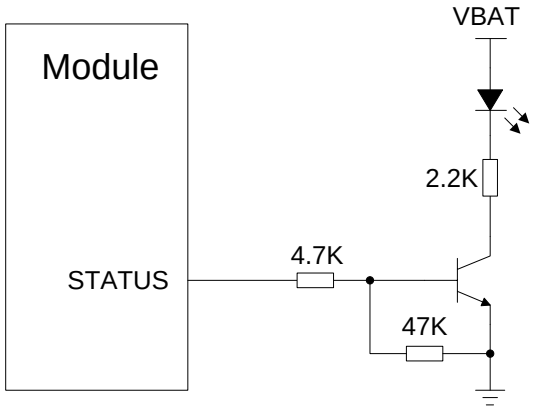


Figure 30: Reference Circuits of STATUS

4.12. GPIOs

The module provides eight general GPIOs, which can be configured as general GPIO or other functions. For details, see ***document [5]***.

Table 26: Pin Definition of GPIOs

Pin Name	Pin No.	I/O	Description	Comment
GPIO1	16	DIO	General-purpose input/output	1.8 V power domain. If unused, keep them open.
GPIO2	64	DIO	General-purpose input/output	
GPIO3	92	DIO	General-purpose input/output	
GPIO4	104	DIO	General-purpose input/output	
GPIO5	105	DIO	General-purpose input/output	
GPIO6	106	DIO	General-purpose input/output	

GPIO7	107	DIO	General-purpose input/output
GPIO8	116	DIO	General-purpose input/output

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

Table 27: Pin Definition of Cellular Network Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance.

NOTE

Only passive antennas are supported.

Table 28: Operating Frequency of EG912N-EN

Operating Frequency	Transmit (MHz)	Receive (MHz)
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690

LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803
LTE-FDD B31	452.5–457.5	462.5–467.5
LTE-FDD B72	451–456	461–466

5.1.2. Transmitting Power

Table 29: RF Transmitting Power

Frequency Bands	Max.	Min.
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B7/B8/B20/B28/B31/B72	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots Tx mode, the maximum output power is reduced by 4.0 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

5.1.3. Receiver Sensitivity

The following table shows conducted RF receiver sensitivity of the module.

Table 30: Conducted RF Receiver Sensitivity of EG912N-EN

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO	
EGSM900	-108 dBm	-	-	-102 dBm
DCS1800	-107 dBm	-	-	-102 dBm
LTE-FDD B1 (10 MHz)	-98 dBm	-	-	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98 dBm	-	-	-93.3 dBm
LTE-FDD B5 (10 MHz)	-98 dBm	-	-	-94.3 dBm
LTE-FDD B7 (10 MHz)	-97 dBm	-	-	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98 dBm	-	-	-93.3 dBm
LTE-FDD B20 (10 MHz)	-96.5 dBm	-	-	-93.3 dBm
LTE-FDD B28 (10 MHz)	-97.5 dBm	-	-	-94.8 dBm
LTE-FDD B31 (5 MHz)	-97.5 dBm	-	-	-92.8 dBm
LTE-FDD B72 (5 MHz)	-96.5 dBm	-	-	-92.8 dBm

5.1.4. Reference Design

The module provides one RF antenna interfaces for antenna connection.

It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (C1, R1, and C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

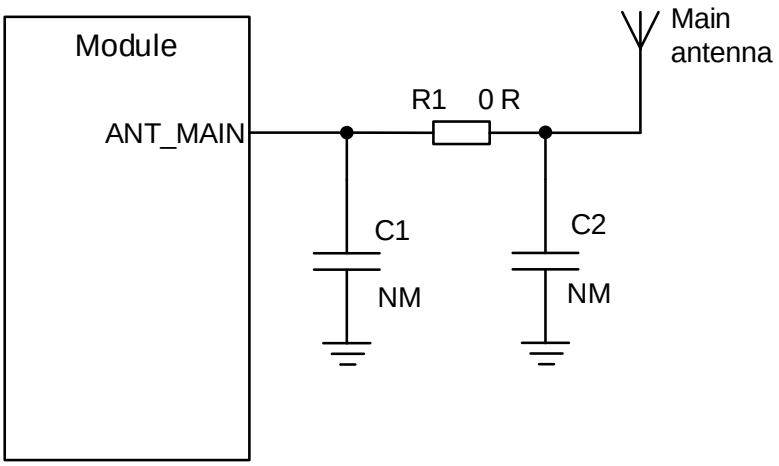


Figure 31: Reference Circuit for RF Antenna Interface

5.2. Reference Design of RF Routing

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

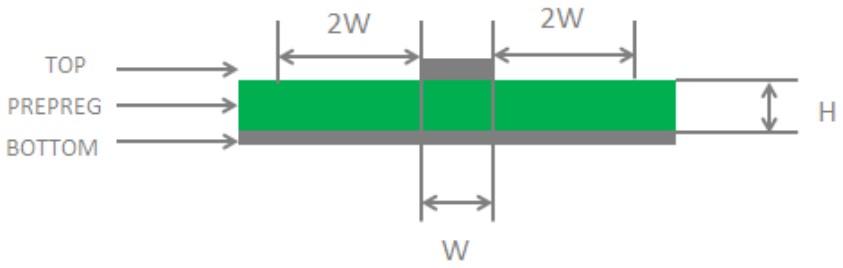


Figure 32: Microstrip Design on a 2-layer PCB

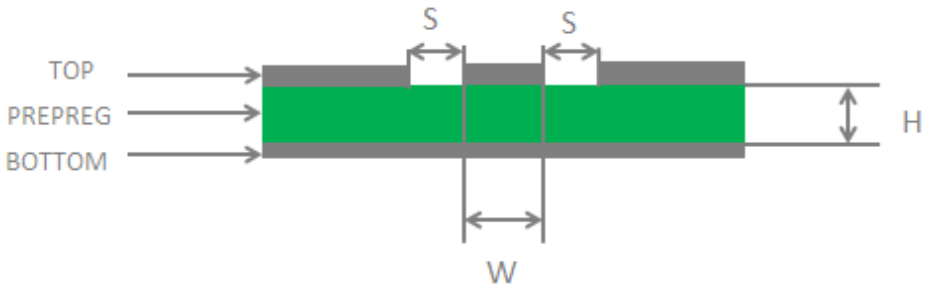


Figure 33: Coplanar Waveguide Design on a 2-layer PCB

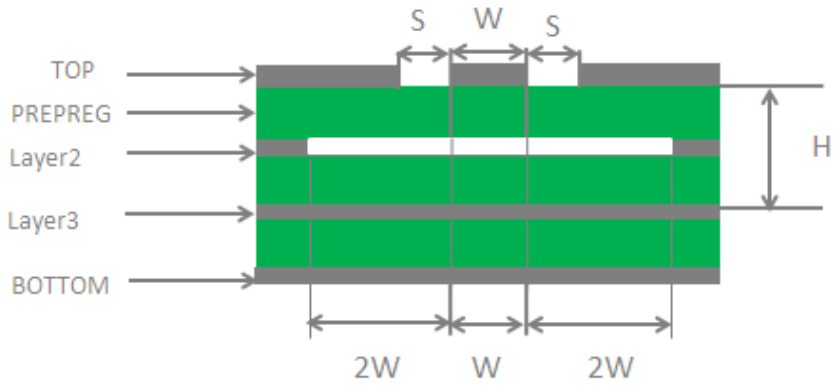


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

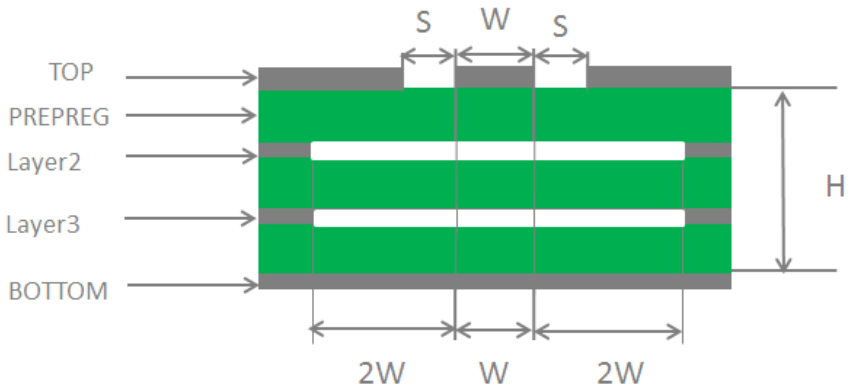


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [7]***.

5.3. Requirements for Antenna Design

Table 31: Requirements for Antenna Design

Antenna Type	Requirements
GSM/LTE	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Gain: 1 dBi ● Max input power: 50 W ● Input impedance: 50 Ω ● Polarization: Vertical ● Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

5.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

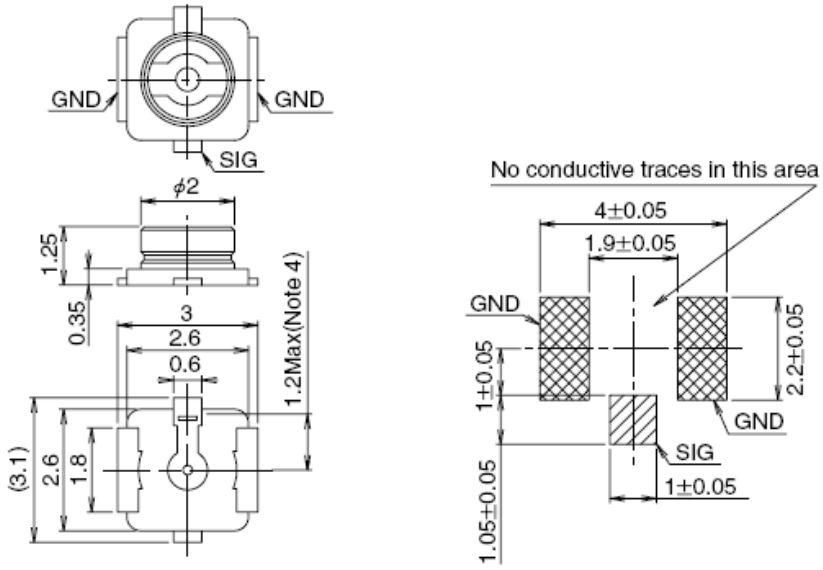


Figure 36: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

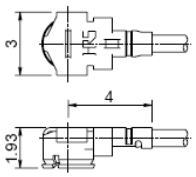
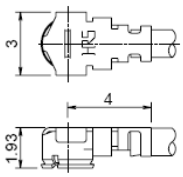
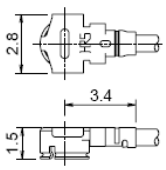
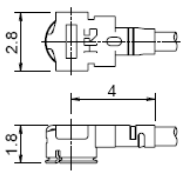
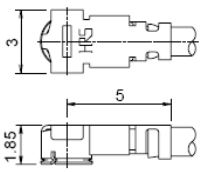
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 37: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

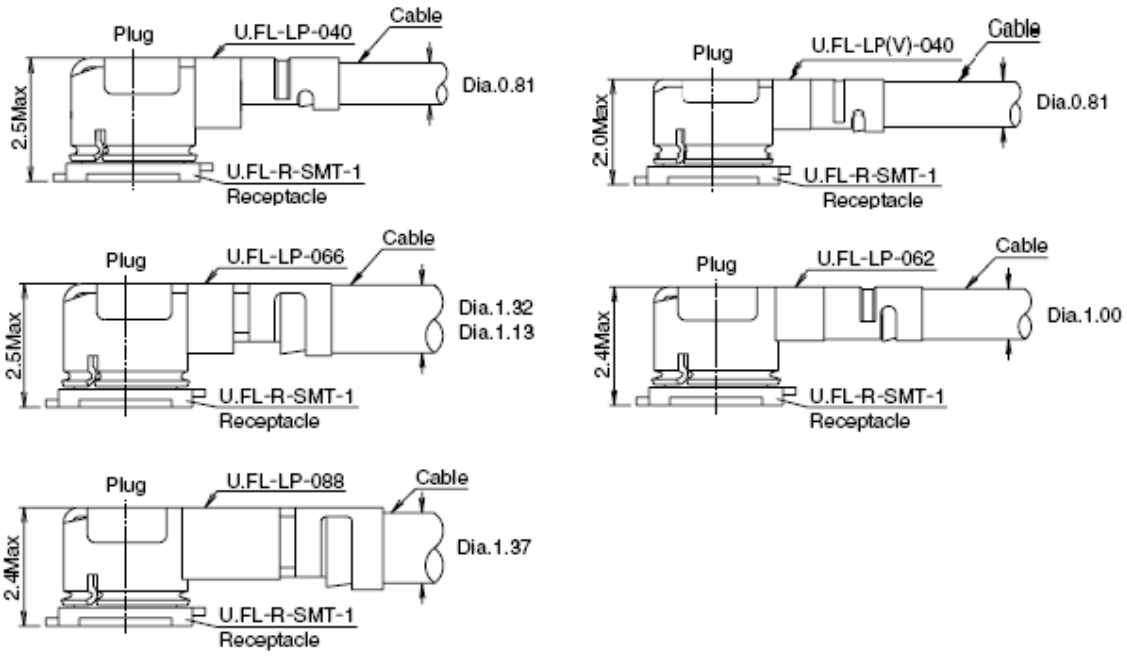


Figure 38: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Table 32: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	2.2	A
Voltage on Digital Pins	-0.3	2.3	V

6.2. Power Supply Ratings

Table 33: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values	3.4	3.8	4.3	V
	Voltage drop during transmitting burst	AT maximum power control level	-	-	400	mV
I_{VBAT}	Peak supply current	AT maximum power control level	-	2.0	2.5	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

6.3. Power Consumption

Table 34: Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	29	μA
Sleep state	Minimum Functionality Mode (USB disconnected)	0.69	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.00	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.37	mA
	EGSM900 @ DRX = 5 (USB suspend)	1.50	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.15	mA
	DCS1800 @ DRX = 2 (USB disconnected)	1.76	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.26	mA
	DCS1800 @ DRX = 5 (USB suspend)	1.38	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.09	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.71	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.26	mA
	LTE-FDD @ PF = 64 (USB suspend)	1.43	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.04	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.94	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	20.10	mA
	EGSM900 @ DRX = 5 (USB connected)	29.28	mA
	LTE-FDD @ PF = 64 (USB disconnected)	20.04	mA
	LTE-FDD @ PF = 64 (USB connected)	29.18	mA
GPRS data transmission	EGSM900 4DL/1UL @ 32.43 dBm	243	mA
	EGSM900 3DL/2UL @ 32.37 dBm	435	mA
	EGSM900 2DL/3UL @ 30.83 dBm	525	mA

	EGSM900 1DL/4UL @ 28.99 dBm	578	mA
	DCS1800 4DL/1UL @ 30.22 dBm	154	mA
	DCS1800 3DL/2UL @ 30.17 dBm	264	mA
	DCS1800 2DL/3UL @ 28.62 dBm	318	mA
	DCS1800 1DL/4UL @ 26.53 dBm	336	mA
EDGE data transmission	EGSM900 4DL/1UL @ 26.92 dBm	150	mA
	EGSM900 3DL/2UL @ 26.92 dBm	256	mA
	EGSM900 2DL/3UL @ 25.18 dBm	313	mA
	EGSM900 1DL/4UL @ 23.30 dBm	353	mA
	DCS1800 4DL/1UL @ 26.31 dBm	120	mA
	DCS1800 3DL/2UL @ 26.35 dBm	199	mA
	DCS1800 2DL/3UL @ 24.54dBm	251	mA
	DCS1800 1DL/4UL @ 22.69 dBm	295	mA
LTE data transmission	LTE-FDD B1	518.77	mA
	LTE-FDD B3	528.30	mA
	LTE-FDD B5	472.56	mA
	LTE-FDD B7	459.75	mA
	LTE-FDD B8	428.98	mA
	LTE-FDD B20	515.66	mA
	LTE-FDD B28	405.87	mA
	LTE-FDD B31	562.22	mA
	LTE-FDD B72	592.15	mA
GSM voice call	EGSM900 PCL = 5 @ 32.58 dBm	255	mA
	EGSM900 PCL = 12 @ 19.66 dBm	97	mA
	EGSM900 PCL = 19 @ 5.41 dBm	60	mA
	DCS1800 PCL = 0 @ 30.26 dBm	162	mA

	DCS1800 PCL = 7 @ 17.24 dBm	76	mA
	DCS1800 PCL = 15 @ 1.24 dBm	56	mA

6.4. Digital I/O Characteristic

Table 35: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	0.7 × VDDIO	VDDIO + 0.2	V
V_{IL}	Input low voltage	-0.3	0.3 × VDDIO	V
V_{OH}	Output high voltage	VDDIO – 0.2	-	V
V_{OL}	Output low voltage	-	0.2	V

Table 36: (U)SIM Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{IL}	Input low voltage	0	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.15 × USIM_VDD	V

Table 37: (U)SIM High-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{IL}	Input low voltage	0	0.15 × USIM_VDD	V
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.15 × USIM_VDD	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

ESD characteristics of the module's pins are as follows:

Table 38: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 39: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [3]	-35	+25	+75	°C
Extended Temperature Range [4]	-40	-	+85	°C
Storage temperature range	-40	-	+95	°C

[3] Within operating temperature range, the module meets 3GPP specifications.
[4] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

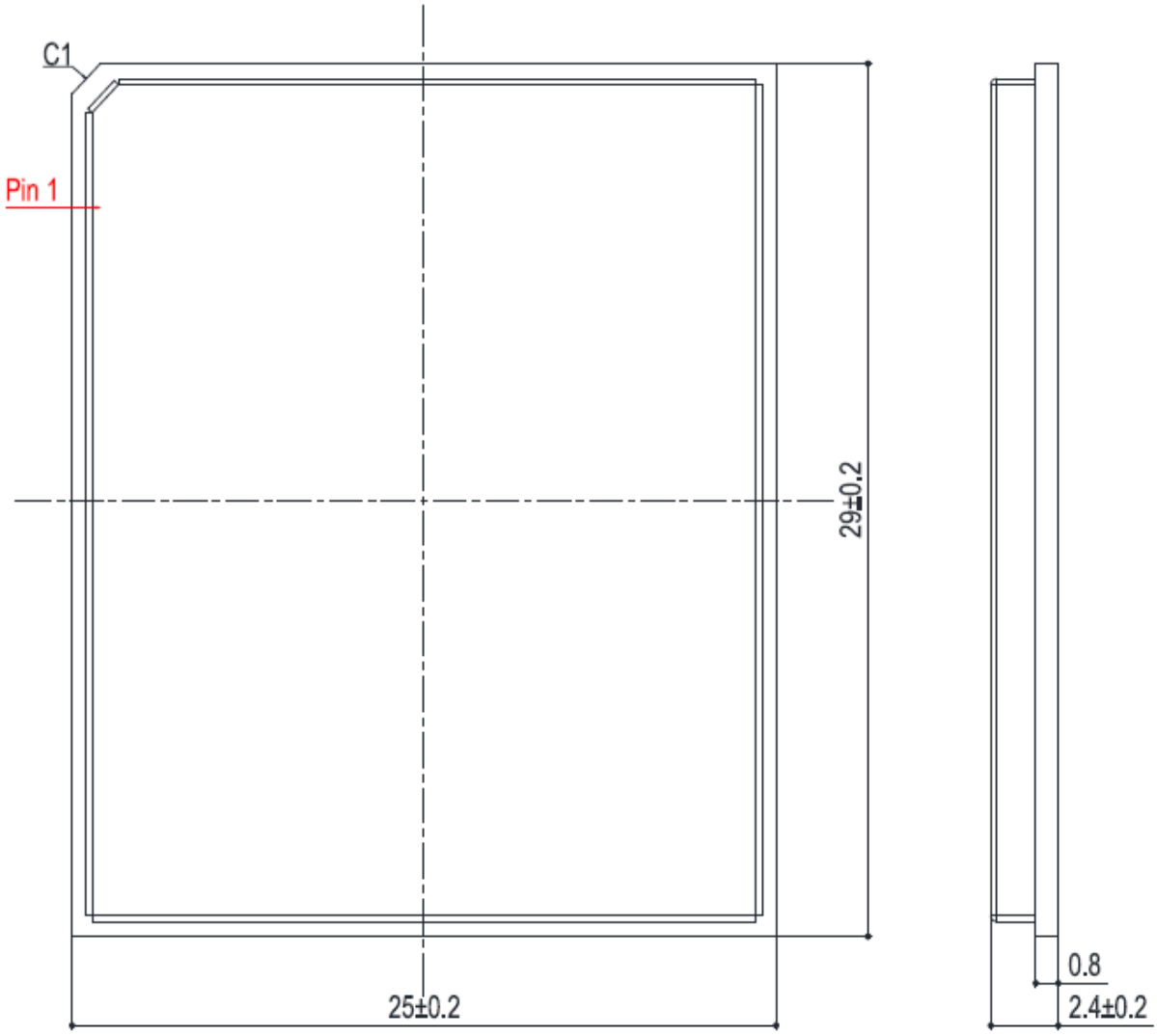


Figure 39: Module Top and Side Dimensions (Unit: mm)

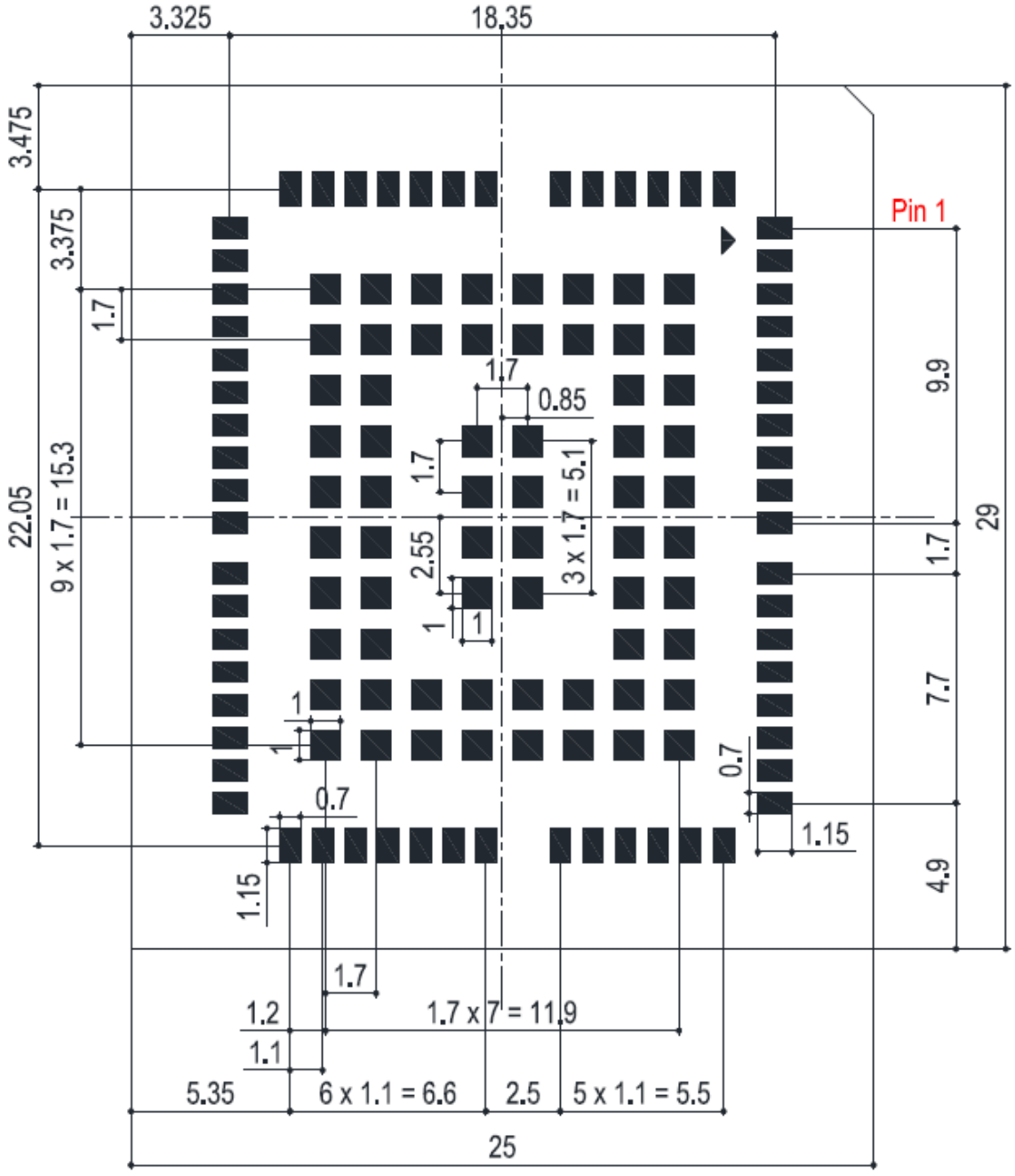


Figure 40: Module Bottom Dimensions (Bottom View, Unit: mm)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

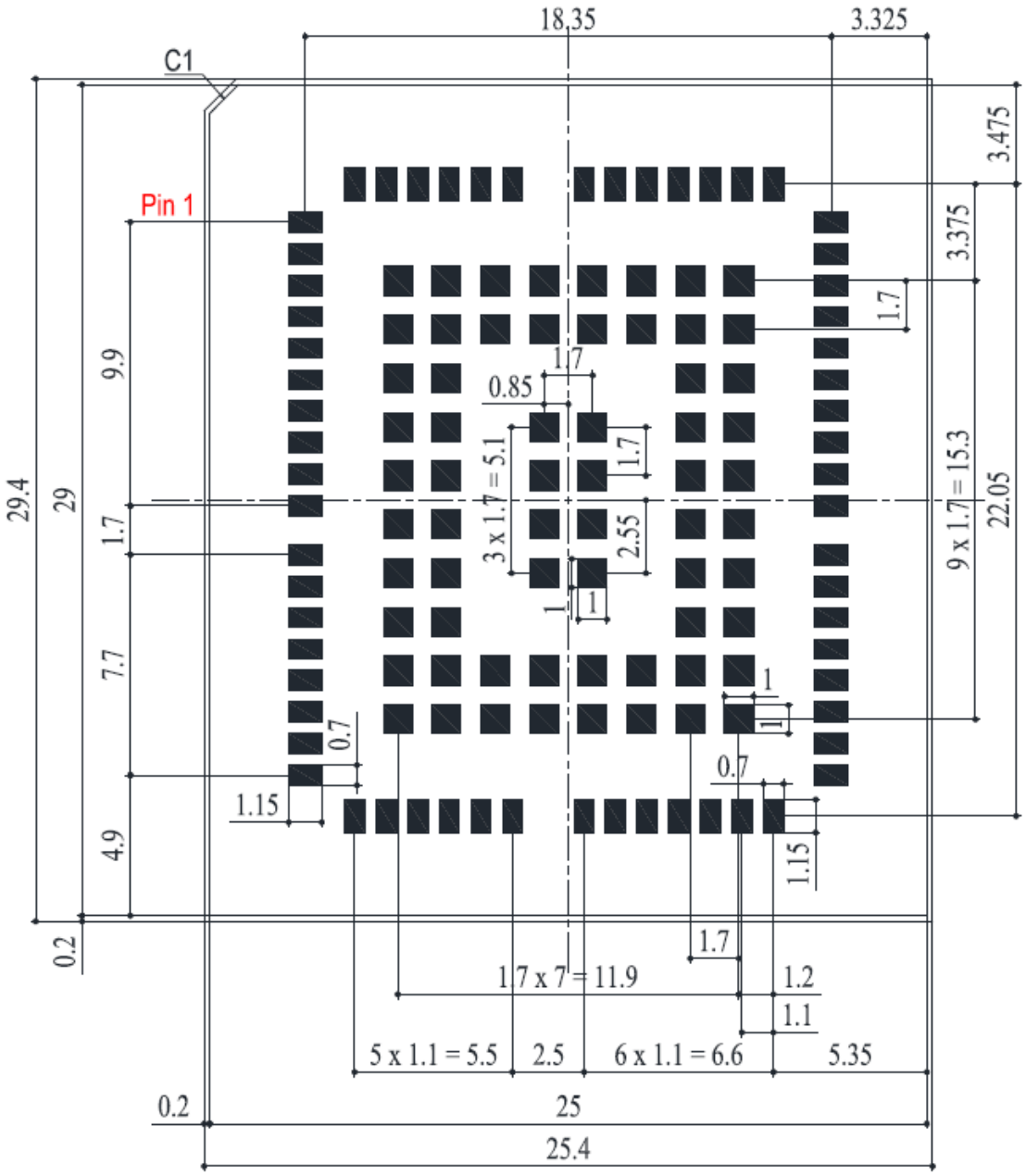


Figure 41: Recommended Footprint (Top View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

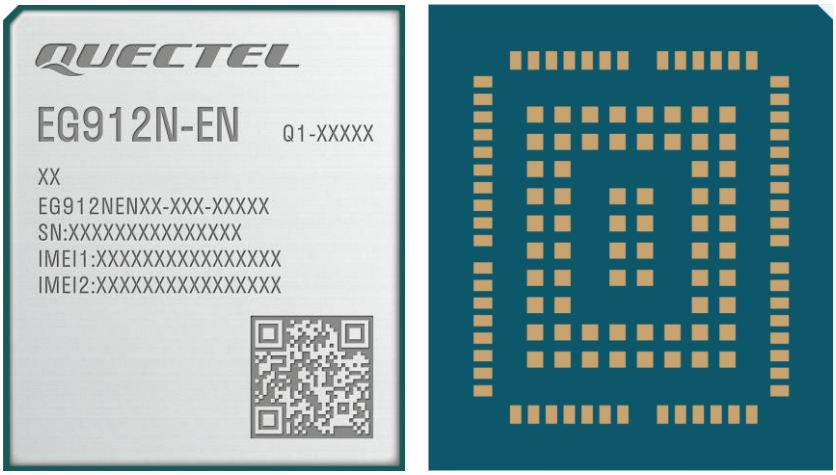


Figure 42: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [5] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[5] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [8]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

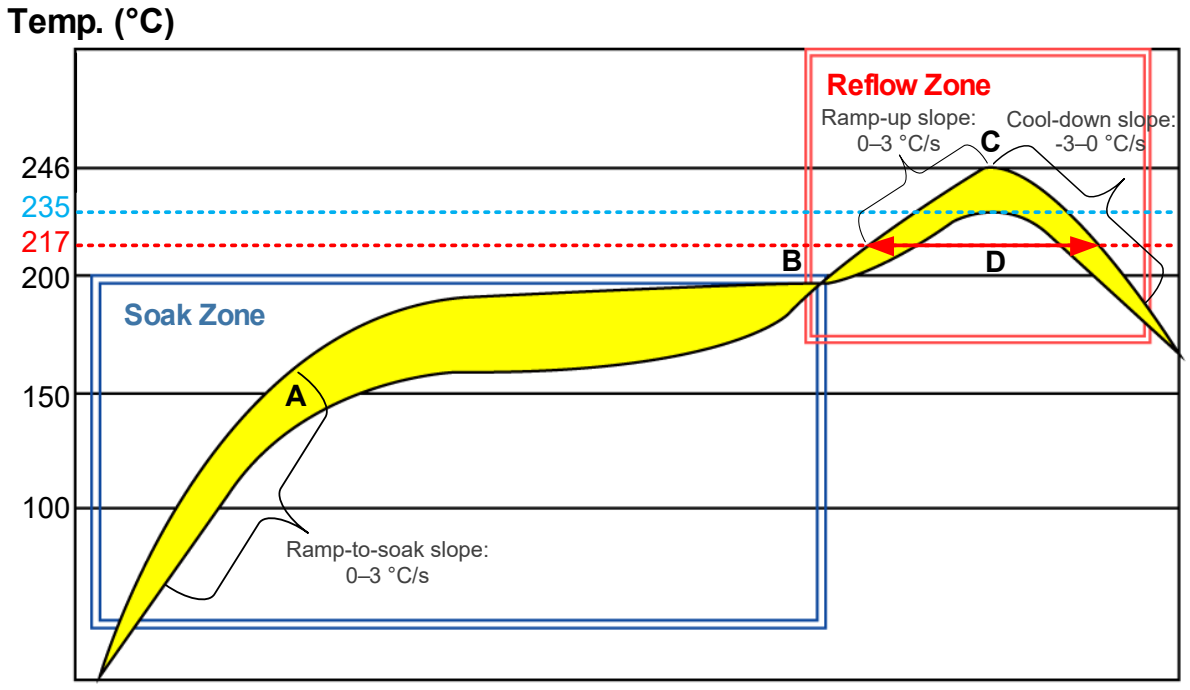


Figure 43: Recommended Reflow Soldering Thermal Profile

Table 40: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235–246 °C
Cooling down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [8]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

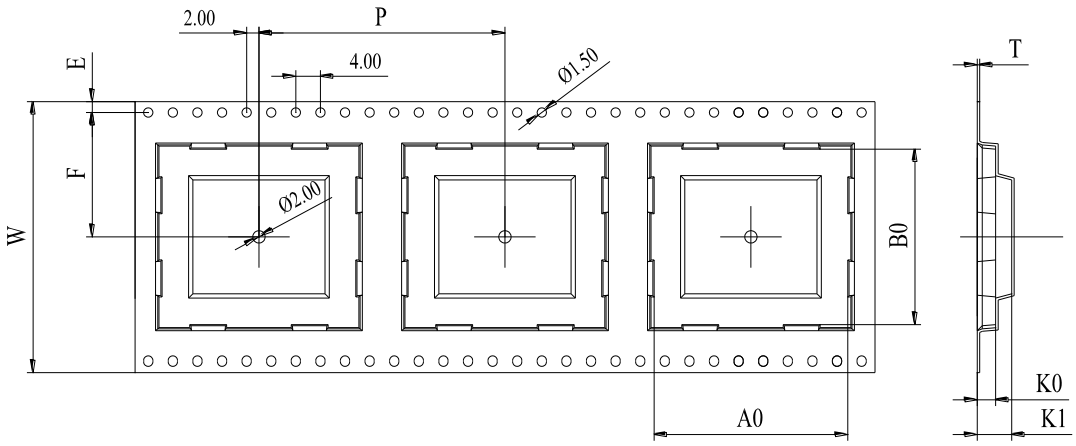


Figure 44: Carrier Tape Dimension Drawing

Table 41: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	25.5	29.5	3.2	5.8	20.2	1.75

8.3.2. Plastic Reel

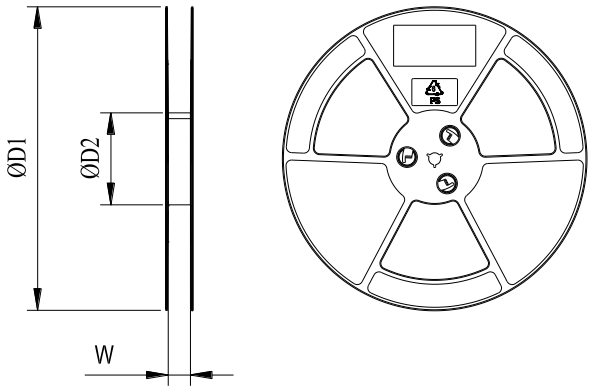


Figure 45: Plastic Reel Dimension Drawing

Table 42: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

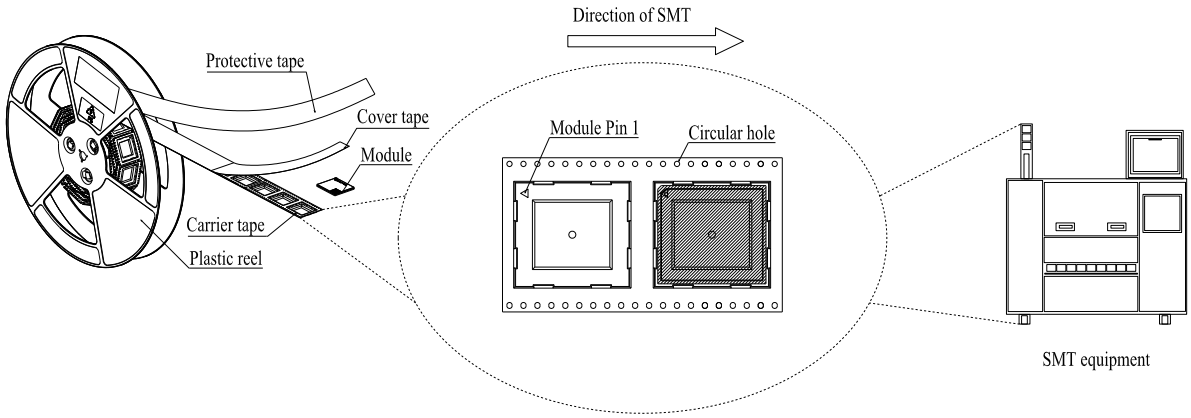
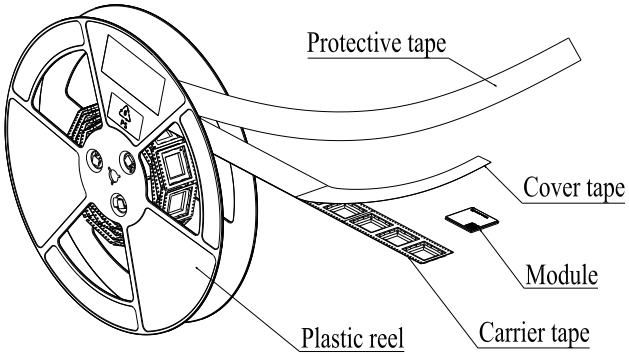


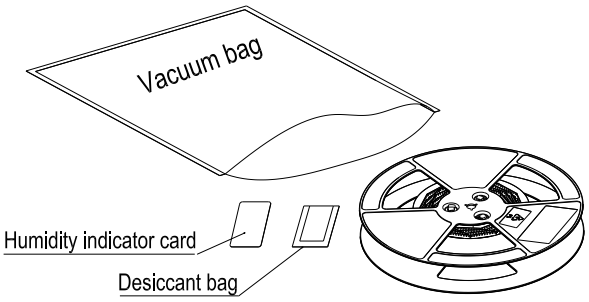
Figure 46: Mounting Direction

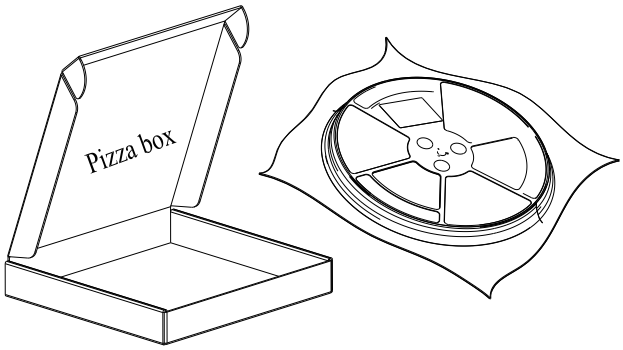
8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 1000 modules.

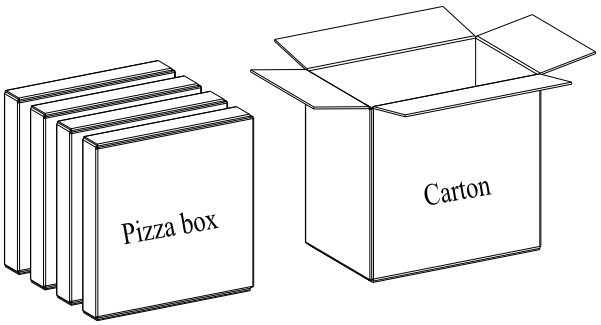


Figure 47: Packaging Process

9 Appendix References

Table 43: Related Documents

Document Name
[1] Quectel_LTE_OPEN_EVB_User_Guide
[2] Quectel_EG91xN_Series_QuecOpen_Device_Management_API_Reference_Manual
[3] Quectel_EG91xN_Series_QuecOpen_Low_Power_Consumption_API_Reference_Manual
[4] Quectel_EG91xN_Series_QuecOpen_Booting&Shutdown_User_Guide
[5] Quectel_EG912N_EN_QuecOpen_GPIO _Configuration
[6] Quectel_EC200S&EG91xN_Series_QuecOpen_ADC_Development_Guide
[7] Quectel_RF_Layout_Application_Note
[8] Quectel_Module_SMT_Application_Note

Table 44: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
AMR-WB	Adaptive Multi-Rate Wideband
AP	Application Processor
bps	Bits Per Second
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection MUX

CS	Coding Scheme
CTS	Clear To Send
DCE	Data Communications Equipment
DCS	Data Coding Scheme
DFOTA	Delta Firmware Upgrade Over the Air
DL	Downlink
DRX	Discontinuous Reception
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EGSM	Enhanced GSM
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
EVB	Evaluation Board
FDD	Frequency Division Duplex
FILE	File Protocol
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP-SSL: FTP over SSL / FTP Secure
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
HB	High Band
HR	Half Rate

HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I/O	Input/Output
LB	Low Band
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LSB	Least Significant Bit
LTE	Long Term Evolution
MB	Middle Band
MCU	Microcontroller Unit
MHB	Middle/High Band
MLCC	Multi-layer Ceramic Capacitor
MIMO	Multiple Input Multiple Output
MMS	Multimedia Messaging Service
MO	Mobile Originated
MQTT	Message Queuing Telemetry Transport
MS	Mobile Station
MSB	Most Significant Bit
MT	Mobile Terminated
NITZ	Network Identity and Time Zone / Network Informed Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NTP	Network Time Protocol

PA	Power Amplifier
PAP	Password Authentication Protocol
PAM	Power Amplifier Module
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PING	Packet Internet Groper
PMIC	Power Management Integrated Circuit
PPP	Point-to-Point Protocol
PRX	Primary Receive
RAM	Random Access Memory
RI	Ring Indicator
RF	Radio Frequency
Rx	Receive
SIMO	Single Input Multiple Output
SMD	Surface Mount Device
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
STB	Set Top Box
TCP	Transmission Control Protocol
TDD	Time Division Duplexing

THD	Total Harmonic Distortion
Tx	Transmit
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access