EG810M-EU QuecOpen&QuecPython Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2024-05-11	Mark YANG/ Stefan FAN/ Jerry LIN/ Pinky YANG	Creation of the document
1.0	2024-06-25	Mark YANG/ Stefan FAN/ Jerry LIN/ Pinky YANG	First official release

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1 Introduction

This document defines the EG810M-EU module in QuecOpen® or QuecPython® solution and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module.

1.1. QuecOpen® Solution Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle.
- Simplify circuit and hardware structure design to reduce engineering costs.
- Miniaturize products.
- Reduce product power consumption.
- Apply OTA technology.
- Enhance product competitiveness and price-performance ratio.

1.2. QuecPython® Solution Introduction

QuecPython® is a Python runtime environment transplanted from MicroPython® open-source library. It is a new IoT development solution based on Quectel's module that uses MircroPython® to invoke the module's software functions and external hardware interfaces to help users perform the secondary development of embedded applications. Its main advantages are as follows:

- Efficient and convenient Python development: provide abundant API to ensure the stability and functionality of the interfaces to the greatest extent.
- Compatible with MicroPython®, easy to update and iterate.
- High data security for its architecture.
- Strong portability for its design architecture can be quickly transplanted and adapted to other application platforms.

1.3. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.

2 Product Overview

The module is an SMD type module with compact packaging, which is engineered to meet the demands in M2M applications.

Table 2: Basic Information

Basic Information	EG810M-EU
Packaging type	LGA
Pin counts	109
Dimensions	(17.7 +0.3/-0.15) mm × (15.8 +0.3/-0.15) mm × (1.7 ±0.2) mm
Weight	Approx. 0.98 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Wireless Network Type	EG810M-EU
LTE-FDD	B1/B3/B5/B7/B8/B20/B28

2.2. Key Features

Table 4: Key Features

Categories	Descriptions
Supply Voltage	● Supply voltage range: 3.4–4.3 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: stored in USIM card and ME, ME by default ● SGS SMS (optional), IMS SMS (optional)
USB Interface	● Compliant with USB 2.0 (slave mode only), with data transmission rates up to 480 Mbps ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial drivers for Windows 8.1/10/11, Linux 2.6–6.7 and Android 4.x–13.x
Forced Download Interface	Supports one forced download interface
USIM Interfaces	● Supports 1.8 V and 3.0 V USIM card and DSSS function ● USIM2 is optional
UARTs	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for partial log output ● Baud rate: 115200 bps **Auxiliary UART:** ● Used for communication with peripherals ● Baud rate: 115200 bps
Audio Features	Supports echo cancellation and noise suppression
PCM Interface (optional)	● Used for audio data transmission with external Codec ● Supports 16-bit linear data format ● Supports short frame synchronization: the module only works as a master device
I2C Interfaces (optional)	● Supports two I2C interfaces ● Complies with I2C-bus specification
Analog Audio Interface (optional)	Supports one analog audio input and one analog audio output
SPI	● Supports slave mode* and master mode (default) with a maximum clock frequency of 26 MHz ● Multiplexed from PCM interface
LCM Interface	● Supports LCD display module with a maximum resolution of 240 × 320 ● Supports SPI four-wire single data trace transmission ● Supports RGB565 format output
Matrix Keypad Interface	Supports 3 × 3 matrix keypad

Camera Interface	● Supports up to 0.3 MP ● Supports the single data line or dual data line transmission of SPI
ADC Interfaces	Supports two ADC interfaces
Network Indication	NET_STATUS indicates network activity status
AT Commands	Compliant with *3GPP TS 27.007, 3GPP TS 27.005* and Quectel enhanced AT commands
Antenna Interfaces	● LTE/Wi-Fi Scan antenna interface (ANT_MAIN) ● 50 Ω characteristic impedance
Transmitting Power	LTE-FDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Supports 3GPP Rel-13 Cat 1 bis FDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports UL QPSK, 16QAM modulations ● Supports DL QPSK, 16QAM, 64QAM modulations ● LTE-FDD maximum data rates: – DL: 10 Mbps – UL: 5 Mbps
Position Fixing	Supports Wi-Fi Scan [1] function (share the main antenna)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX*/HTTPS/FTPS/SSL/FILE/MQTT/MMS*/SMTP*/SMTPS* protocols ● Compliant with PAP and CHAP for PPP connections
Temperature Ranges	● Normal operating temperature [2]: -35 °C to +75 °C ● Extended temperature [3]: -40 °C to +85 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	Use USB 2.0 interface or DFOTA to upgrade
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTE

1. Different tools must be used for firmware upgrade for QuecOpen and QuecPython solutions.
   - QuecOpen: The 6.0 and above version QFlash tool must be used for firmware upgrade.
   - QuecPython: The 3.3 and above version QPYcom tool must be used for firmware upgrade.

   For more details about QPYcom tool, please visit https://python.quectel.com/doc/Application_guide/zh/dev-tools/QPYcom/index.html.
2. PCM, I2C, USIM2 and analog audio functions of the module are optional. If the USIM2 function is required, contact Quectel Technical Support.

[1] Wi-Fi Scan function shares the same antenna interface with the main antenna. These two antennas should use TDM (Time Division Multiplexing) and cannot be used simultaneously. Wi-Fi Scan only supports receiving and does not support transmitting.
[2] Within this range, the module's indicators comply with 3GPP specification requirements.
[3] Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call*, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. Functional Diagram

The block diagram illustrates the following major functional parts:

- Power management
- Baseband part
- Flash
- Radio frequency part
- Peripheral interfaces

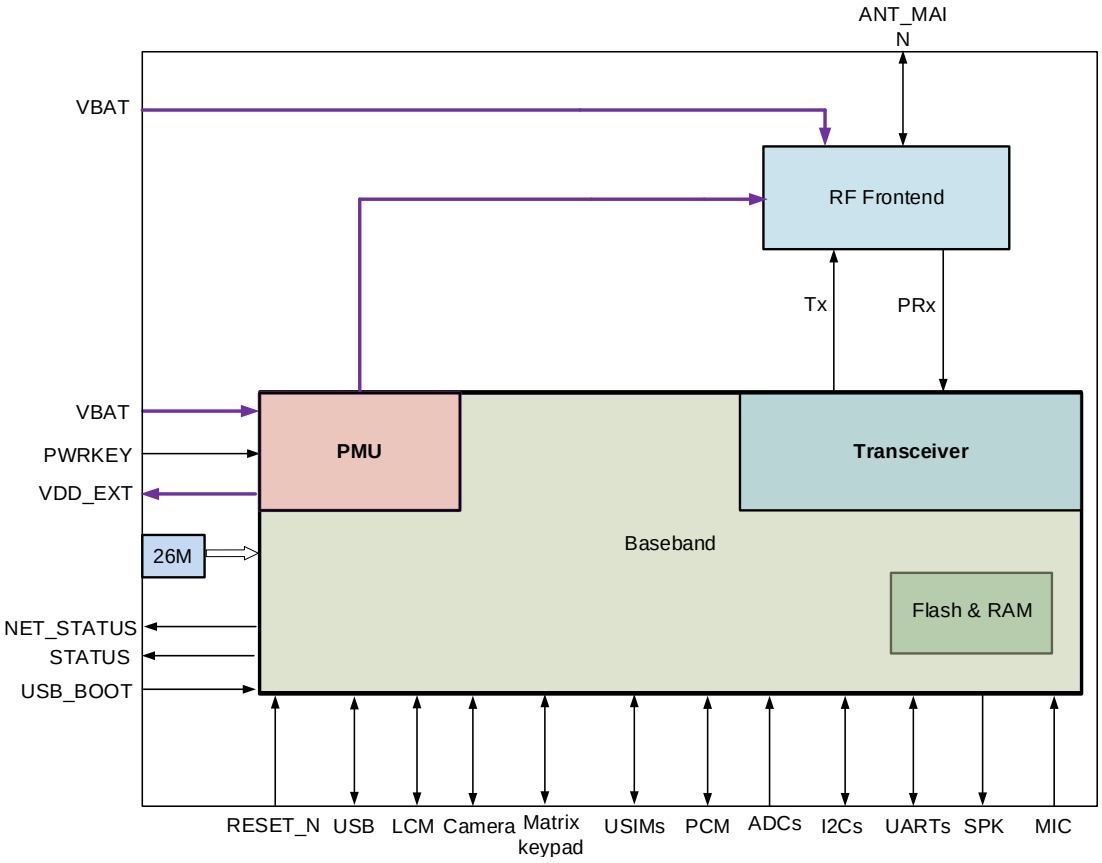


Figure 1: Functional Diagram

NOTE

PCM, I2C, USIM2 and analog audio functions of the module are optional. If the USIM2 function is required, contact Quectel Technical Support.

2.4. Pin Assignment

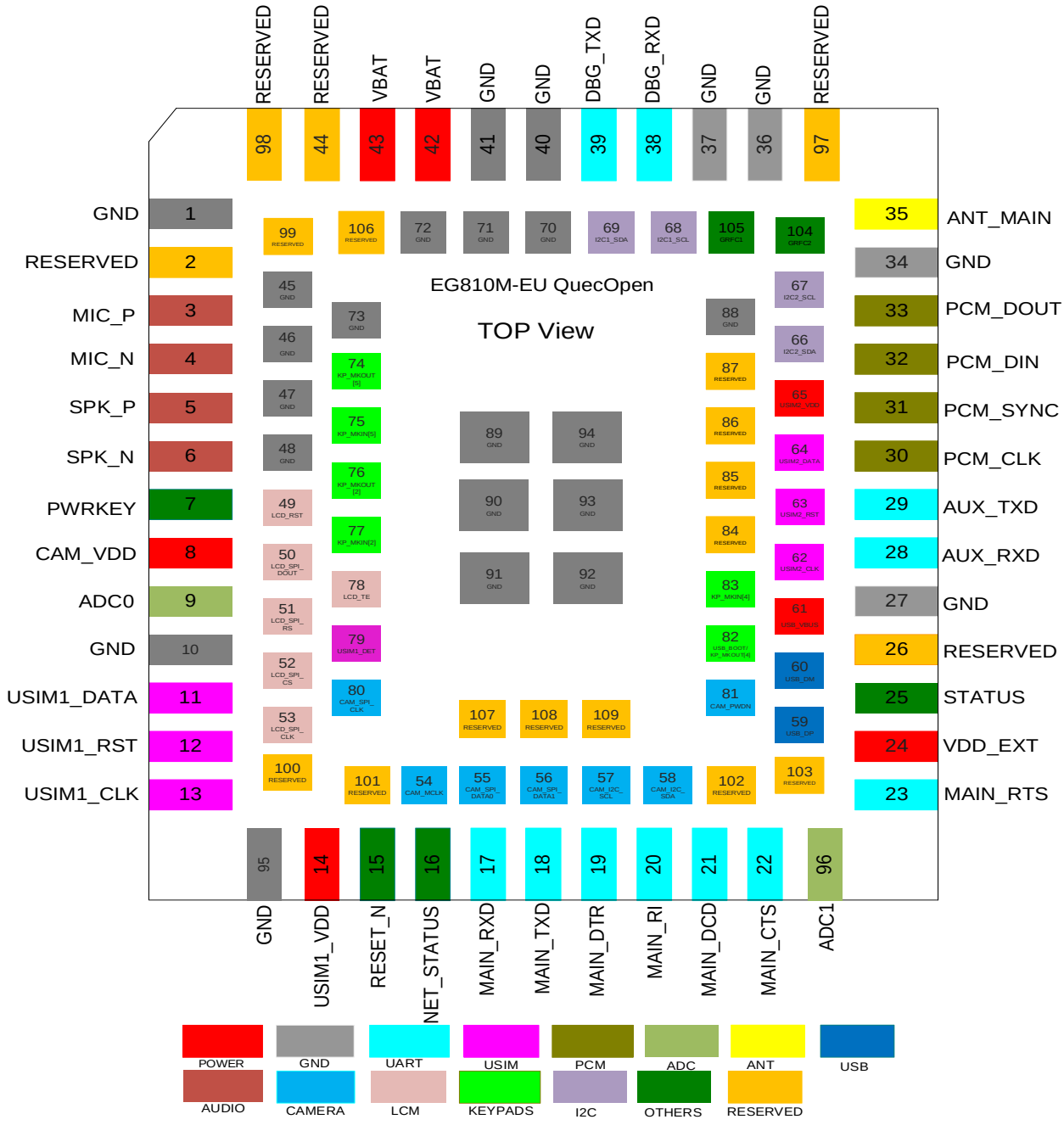


Figure 2: Pin Assignment (Top View)

NOTE

1. PCM, I2C, USIM2 and analog audio functions of the module are optional. If the USIM2 function is required, contact Quectel Technical Support.
2. Keep all RESERVED pins and unused pins open. Connect all GND pins to the ground.
3. Do not pull USB_BOOT/KP_MKOUT[4] down to low level before the module is successfully turned

on.
4. Ensure an uninterrupted reference ground plane below the module, with minimal distance between the ground plane and the module layer. Avoid routing other traces on the first layer adjacent to the module layer. At least four-layer board design is recommended.
5. Different tools must be used for firmware upgrade for QuecOpen and QuecPython solutions.
   - QuecOpen: The 6.0 and above version QFlash tool must be used for firmware upgrade.
   - QuecPython: The 3.3 and above version QPYcom tool must be used for firmware upgrade.

   For more details about QPYcom tool, please visit https://python.quectel.com/doc/Application_guide/zh/dev-tools/QPYcom/index.html.

2.5. Pin Definitions

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	42, 43	PI	Power supply for the module	Vmax = 4.3 V Vmin = 3.4 V Vnom = 3.8 V	External power supply must be provided with sufficient current of at least 2.0 A.

					It is recommended to add a TVS externally. A test point is recommended to be reserved.
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95				
Power Supply Output					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_EXT	24	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
Turn on/off/Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	7	DI	Turn on/off the module	V_{IL}max = 0.5 V Vnom = VBAT	A test point is recommended to be reserved.
RESET_N	15	DI	Reset the module	V_{IL}max = 0.5 V Vnom = 1.8 V	Active low. A test point is recommended to be reserved if unused.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_STATUS	16	DO	Indicate the module's network activity status	1.8 V	If unused, keep them open.
STATUS	25	DO	Indicate the module's operation status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_DP	59	AIO	USB 2.0 differential data (+)		Complies with USB 2.0. A differential impedance of 90 Ω is needed. Test points must be reserved.
USB_DM	60	AIO	USB 2.0 differential data (-)		
USB_VBUS	61	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	A test point must be reserved.
USIM Interfaces [4]					

[4] USIM2 is optional, and if the interface is required, contact Quectel Technical Support.

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM1_DATA	11	DIO	USIM1 card data	1.8/3.0 V	
USIM1_RST	12	DO	USIM1 card reset		
USIM1_CLK	13	DO	USIM1 card clock		
USIM1_VDD	14	PO	USIM1 card power supply		Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM1_DET	79	DI	USIM1 card hot-plug detect	1.8 V	If unused, keep it open.
USIM2_VDD	65	PO	USIM2 card power supply	1.8/3.0 V	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM2_DATA	64	DIO	USIM2 card data		
USIM2_CLK	62	DO	USIM2 card clock		
USIM2_RST	63	DO	USIM2 card reset		
Auxiliary UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_RXD	28	DI	Auxiliary UART receive	1.8 V	If unused, keep them open.
AUX_TXD	29	DO	Auxiliary UART transmit		
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RXD	17	DI	Main UART receive	1.8 V	If unused, keep them open.
MAIN_TXD	18	DO	Main UART transmit		
MAIN_DTR	19	DI	Main UART data terminal ready		
MAIN_RI	20	DO	Main UART ring indication		
MAIN_DCD	21	DO	Main UART data carrier detect		
MAIN_CTS	22	DO	Clear to send signal from the module		Connect to the MCU's CTS. If unused, keep it open.
MAIN_RTS	23	DI	Request to send signal to the module		Connect to the MCU's RTS. If unused, keep it open.

Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	38	DI	Debug UART receive	1.8 V	Test points must be reserved.
DBG_TXD	39	DO	Debug UART transmit		
I2C Interfaces (Optional)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C1_SDA	69	OD	I2C1 serial data		An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C1_SCL	68	OD	I2C1 serial clock		
I2C2_SCL	67	OD	I2C2 serial clock		
I2C2_SDA	66	OD	I2C2 serial data		
PCM Interface (Optional)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK	30	DO	PCM clock	1.8 V	If unused, keep them open.
PCM_SYNC	31	DO	PCM data frame sync		
PCM_DIN	32	DI	PCM data input		
PCM_DOUT	33	DO	PCM data output		
Analog Audio Interfaces (Optional)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_P	3	AI	Microphone analog input (+)		If unused, keep them open.
MIC_N	4	AI	Microphone analog input (-)		
SPK_P	5	AO	Analog audio differential output (+)		Used for earpiece. The interface can drive 32 Ω earpiece with power rate at 37 mW @ THD = 1 %. It can also be used to drive external power amplifier devices if the output power rate cannot meet the demand. If unused, keep them open.
SPK_N	6	AO	Analog audio differential output (-)		

Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	35	AIO	Main antenna/Wi-Fi Scan antenna interface		50 Ω characteristic impedance.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	9	AI	General-purpose ADC interface	0–1.2 V	If unused, keep them open.
ADC1	96	AI			
Antenna Tuner Control Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	105	DO	Generic RF controller	1.8 V	If unused, keep them open.
GRFC2	104	DO			
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_RST	49	DO	LCD reset	1.8 V	If unused, keep them open.
LCD_SPI_DOUT	50	DO	LCD SPI data output		
LCD_SPI_RS	51	DO	LCD SPI register select		
LCD_SPI_CS	52	DO	LCD SPI chip select		
LCD_SPI_CLK	53	DO	LCD SPI clock		
LCD_TE	78	DI	LCD tearing effect		
Camera Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CAM_MCLK	54	DO	Camera master clock	1.8 V	If unused, keep them open.
CAM_SPI_DATA0	55	DI	Camera SPI data bit 0		
CAM_SPI_DATA1	56	DI	Camera SPI data bit 1		
CAM_I2C_SCL	57	OD	Camera I2C clock		External 1.8 V pull-up is needed. If unused, keep them open.
CAM_I2C_SDA	58	OD	Camera I2C data		

CAM_SPI_CLK	80	DI	Camera SPI clock		If unused, keep them open.
CAM_PWDN	81	DO	Camera power down		
CAM_VDD	8	PO	Camera power supply	2.8 V/ 100 mA	
Matrix Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
KP_MKOUT[5]	74	DO	Matrix keypad output 5	1.8 V	If unused, keep them open.
KP_MKIN[5]	75	DI	Matrix keypad input 5		
KP_MKOUT[2]	76	DO	Matrix keypad output 2		
KP_MKIN[2]	77	DI	Matrix keypad input 2		
USB_BOOT/ KP_MKOUT[4]	82	DO	Matrix keypad output 4		
KP_MKIN[4]	83	DI	Matrix keypad input 4		
Forced Download Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT/ KP_MKOUT[4]	82	DI	Force the module into download mode	1.8 V	Active low. This pin cannot be pulled down to low level before the module starts up successfully. A test point is recommended to be reserved.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	2, 26, 44, 84–87, 97–103, 106–109				Keep them open.

NOTE

1. PCM, I2C, USIM2 and analog audio functions of the module are optional. If the USIM2 function is required, contact Quectel Technical Support.
2. Keep all RESERVED pins and unused pins open. Connect all GND pins to the ground.
3. Do not pull USB_BOOT/KP_MKOUT[4] down to low level before the module is successfully turned on.

2.6. EVB Kit

Quectel supplies an evaluation board (LTE OPEN EVB) with accessories to develop and test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Overview of Operating Modes

Modes	Functions	
Full Functionality Mode	Idle	Software is active. The module is registered on the network but there is no data interaction.
	Voice/Data	Network connection is ongoing. Power consumption is decided by the network setting and data transmission rate.
Minimum Functionality Mode	● Use API can set the module to the minimum functionality mode when the power is on. ● Both the RF function and USIM card are disabled.	
Airplane Mode	● Use API can set the module to airplane mode. ● The RF function is disabled.	
Sleep Mode	Power consumption of the module will be reduced to an ultra-low level. The module can still receive paging, SMS, voice call and TCP/UDP data from network.	
Power Down Mode	PMU shuts down the power supply. Software is not active. However, operating voltage connected to VBAT remains applied.	

The following table shows the related API used for operating modes.

Table 8: Related API of Operating Modes

		QuecOpen	QuecPython
	API	*ql_dev_set_modem_fun()*	*net.setModemFun()*
Minimum Functionality Mode (Both RF function and USIM card are disabled)	Values of *function/fun*	*QL_DEV_MODEM_MIN_FUN*	0
Full Functionality Mode (Default)		*QL_DEV_MODEM_FULL_FUN*	1
Airplane Mode (RF function is disabled)		*QL_DEV_MODEM_DISBLE_TRANSMIT_AND_RECEIVE_RF_CIRCUITS*	4

NOTE

For more details about API of operating modes:
- QuecOpen: See ***document [2]***;
- QuecPython: Please visit https://python.quectel.com/doc/API_reference/zh/iotlib/net.html.

3.2. Sleep Mode

In sleep mode, power consumption of the module can be reduced to an ultra-low level.

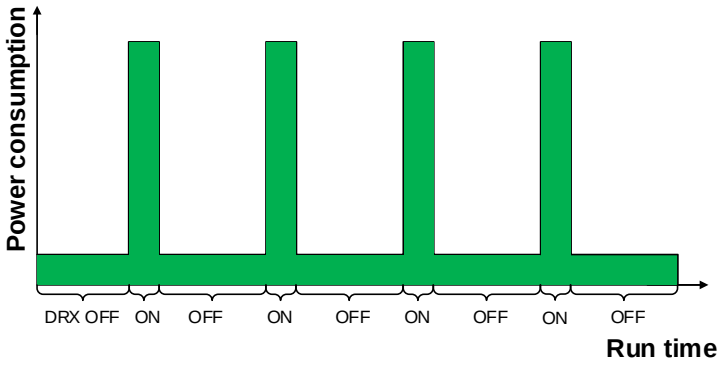


Figure 3: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

The following three conditions should be met to set the module into sleep mode.

- Enable sleep function through API.
- All GPIOs which can be configured as interrupt wake-up function are in non-wake-up state.
- Disconnect USB_VBUS.

Table 9: Related API of Enabling Sleep Mode

	QuecOpen	QuecPython
API	*ql_autosleep_enable()*	*pm.autosleep()*

The following figure shows the connection between the module and the host.

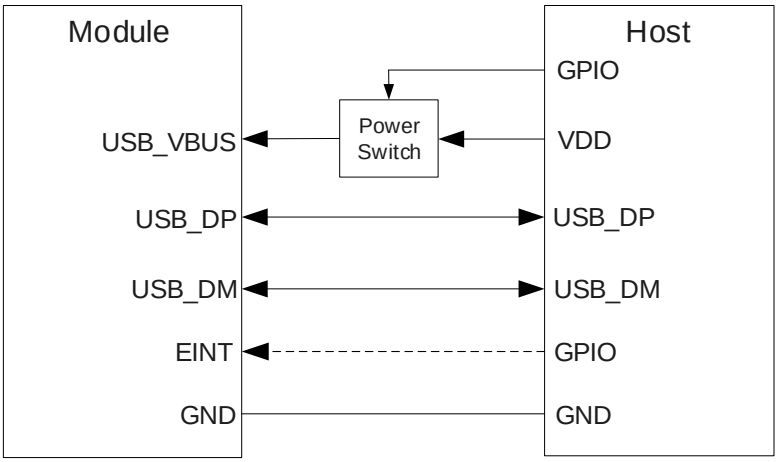


Figure 4: Sleep Mode Application without Suspend Function

You can wake up the module by turning on the power switch to power the USB_VBUS or by using GPIO interrupts.

NOTE

1. Pay attention to the level matching shown in the dotted line between the module and the host in the circuit diagrams.
2. For more details about API of enabling sleep mode:
   - QuecOpen: See ***document [3]***;
   - QuecPython: Please visit https://python.quectel.com/doc/API_reference/zh/syslib/pm.html.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all API related to it will be inaccessible. This mode can be set via following ways:

Software:

The airplane mode can be set through API. For more details, see ***Table 8***.

3.4. Power Supply

3.4.1. Power Supply Interface

The module provides two VBAT pins used to connect the external power supply.

Table 10: Pin Description of Power Supply Interface

Pin Name	Pin No.	I/O	Description	Comment
VBAT	42, 43	PI	Power supply for the module	External power supply must be provided with sufficient current of at least 2.0 A. It is recommended to add a TVS externally. A test point is recommended to be reserved.
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95			

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of at least 2 A. If the voltage difference between input voltage and the desired output VBAT is small, it is suggested to use an LDO; if the voltage difference is large, then a buck converter is suggested to use.

The following figure illustrates a reference design for 5 V input power supply.

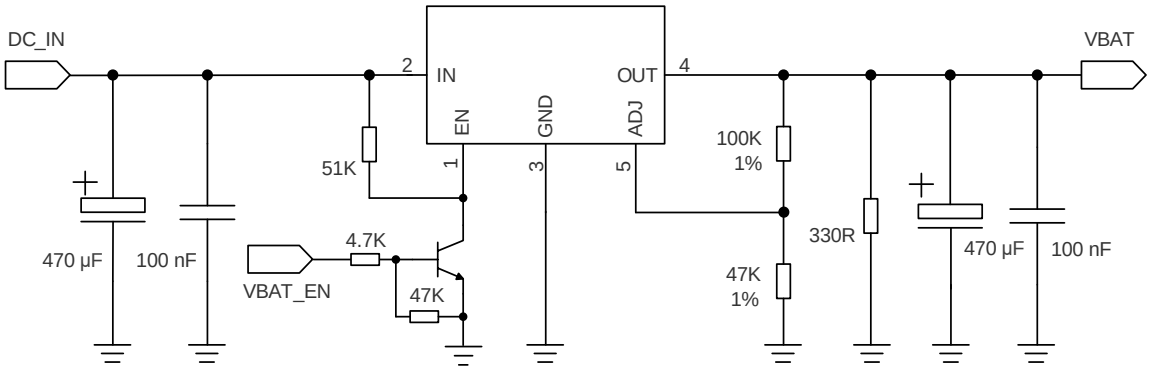


Figure 5: Reference Design of Power Input

NOTE

To avoid corrupting internal flash, do not cut off the power supply when the module works normally. Only after shutting down the module with PWRKEY or APIs, can you cut off the power supply.

3.4.3. Power Supply Voltage Monitoring

You can use the following APIs to monitor and query the VBAT voltage.

Table 11: Related API of Monitoring Power Supply Voltage

	QuecOpen	QuecPython
API	*ql_get_battery_vol()*	*Power.getVbatt()*

NOTE

For more details about API of monitoring power supply voltage:
- QuecOpen: See ***document [4]***;
- QuecPython: Please visit https://python.quectel.com/doc/API_reference/zh/peripherals/misc.Power.html.

3.4.4. Requirements for Voltage Stability

The power supply range of the module is from 3.4 V to 4.3 V. Ensure the input voltage never drops below 3.4 V.

To decrease the voltage drop, a bypass capacitor of about 100 μF with low ESR (ESR ≤ 0.7 Ω) should be used, and reserve a multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR. Use five ceramic capacitors (1.8 pF, 3.9 pF, 10 pF, 33 pF and 100 nF) for composing the MLCC array and a 0 Ω resistor for future debugging (resistance package is not less than 0603), and place these capacitors close to VBAT pins. When the external power supply is connected to the module, the width of VBAT trace should be not less than 2 mm respectively. As per design rules, the longer the VBAT trace is, the wider it should be.

In order to avoid the ripple and surge and ensure the stability of the power supply to the module, add a TVS with V_{RWM} = 4.7 V, low-clamp voltage and peak pulse current Ipp at the front end of the power supply.

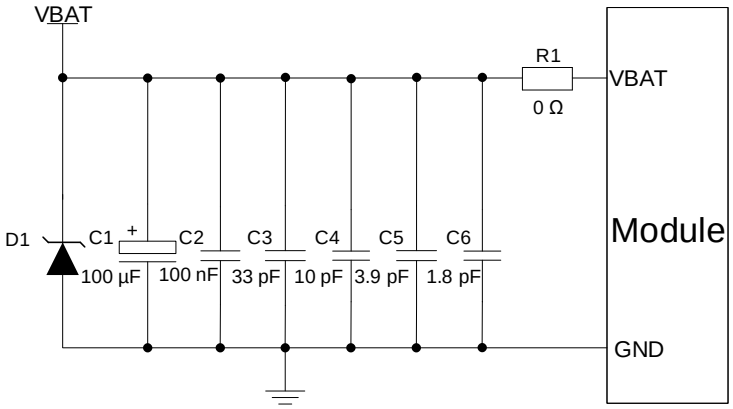


Figure 6: Reference Design of Power Supply

3.5. Turn-on

3.5.1. Turn-on with PWRKEY

Table 12: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turn on/off the module	A test point is recommended to be reserved.

When the module is in turn-off state, it can be turned on by driving PWRKEY low for at least 700 ms. It is recommended to use an open drain/collector driver to control PWRKEY.

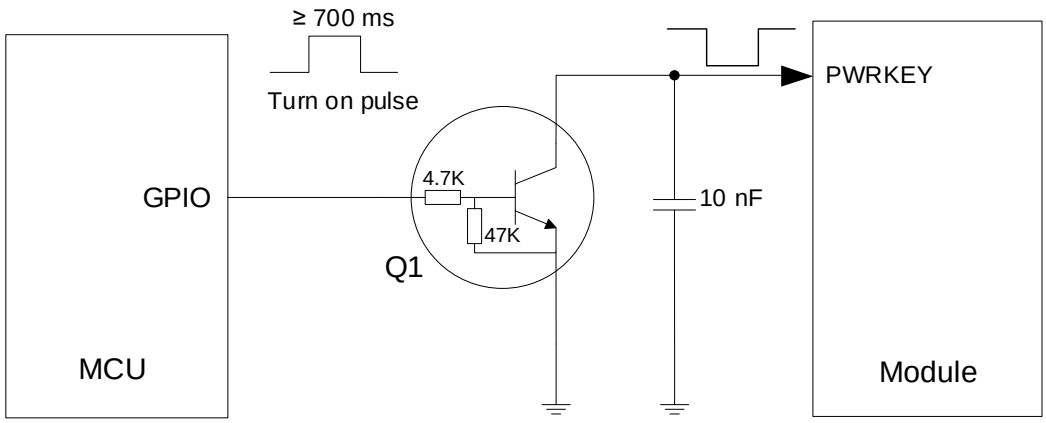


Figure 7: Reference Design of Turn-on with Driving Circuit

Another way to control PWRKEY is by using a push button directly. When pressing the button, an electrostatic strike may be generated from finger. Therefore, a TVS should be placed near the push button for ESD protection.

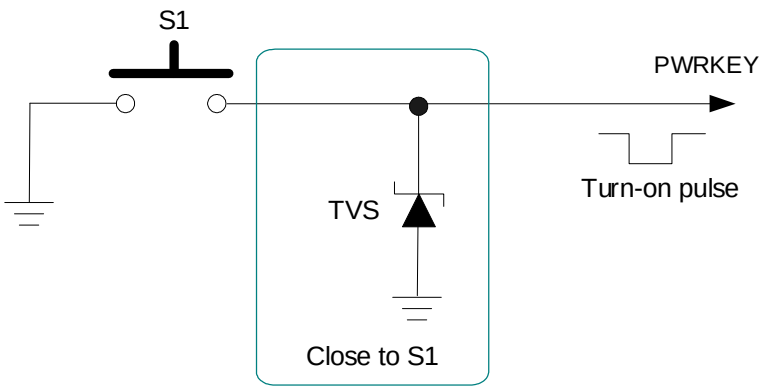


Figure 8: Reference Design of Turn-on with a Button

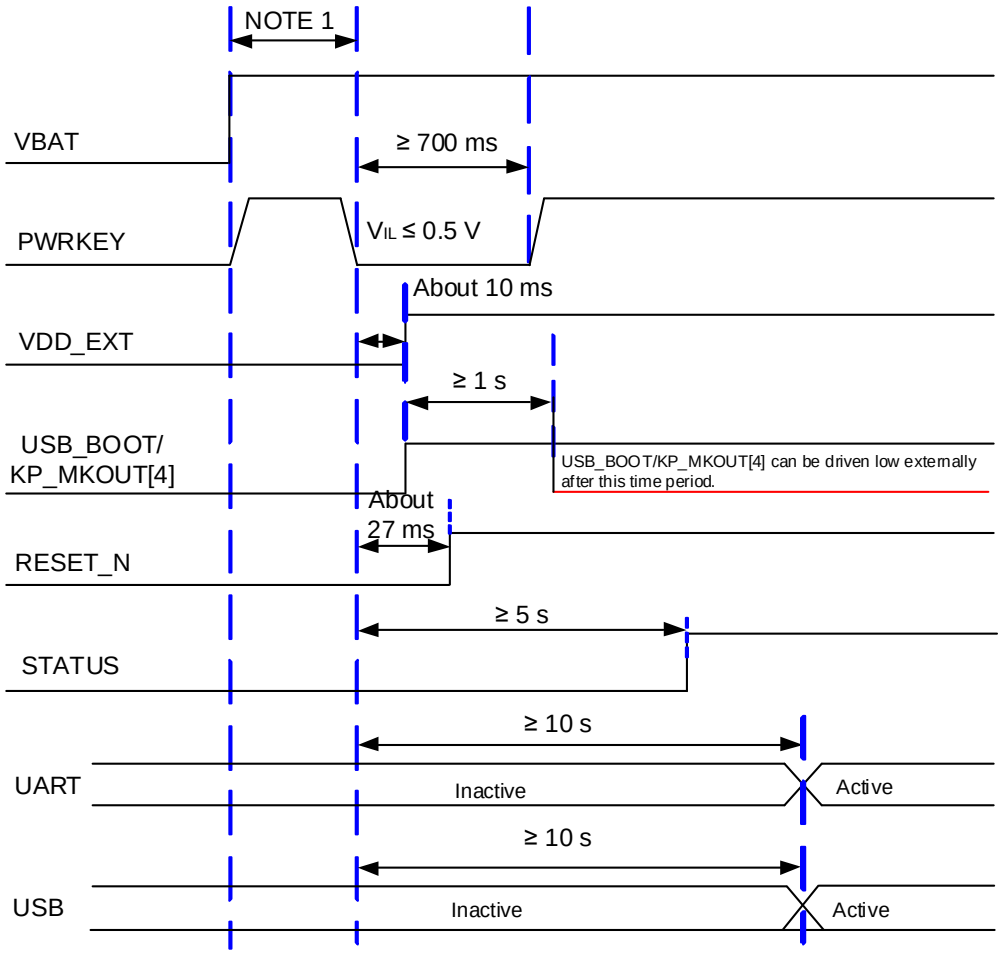


Figure 9: Timing of Turn-on with PWRKEY

NOTE

1. Ensure VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to be turned on automatically when powered up while turn-off function is not needed, PWRKEY can be driven low directly to ground with a recommended 4.7 kΩ resistor.

3.6. Turn-off

3.6.1. Turn-off with PWRKEY

Drive PWRKEY low for at least 650 ms and then release it to turn off the module.

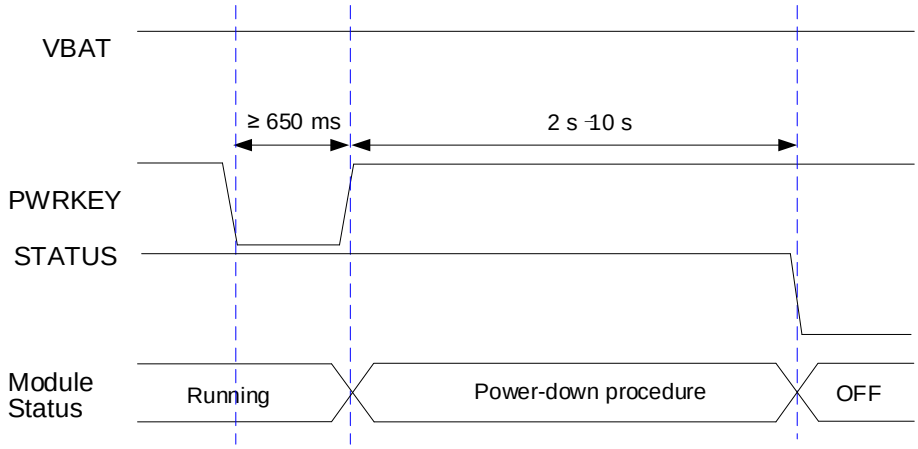


Figure 10: Timing of Turn-off with PWRKEY

3.6.2. Turn-off with API

To turn off the module, you can also execute APIs, which have the same timing and effect as turning off the module through driving PWRKEY low.

Table 13: Related API of Turning off the Module

	QuecOpen	QuecPython
API	*ql_power_down()*	*Power.powerDown()*

NOTE

1. To avoid corrupting the data in the internal flash, do not cut off the power supply when the module works normally. Only after shutting down the module with PWRKEY or APIs, can you cut off the power supply.
2. When turning off module with the APIs, keep the PWRKEY at high level, otherwise the module will be turned on again automatically after successful turn-off.
3. For more details about API of turning off the module:
   - QuecOpen: See ***document [5]***;
   - QuecPython: Please visit https://python.quectel.com/doc/API_reference/zh/peripherals/misc.Power.html.

3.7. Reset

Drive RESET_N low for at least 300 ms and then release it can reset the module. RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 14: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	15	DI	Reset the module	Active low. A test point is recommended to be reserved if unused.

The recommended circuit for reset function is similar to PWRKEY control circuit, you can use open drain/collector driver or button to control RESET_N.

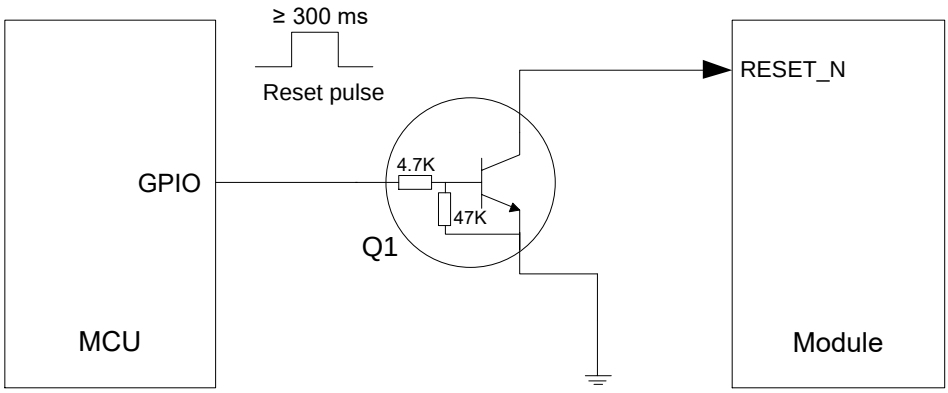


Figure 11: Reference Design of Reset with Driving Circuit

Another way to control RESET_N is by using a push button directly.

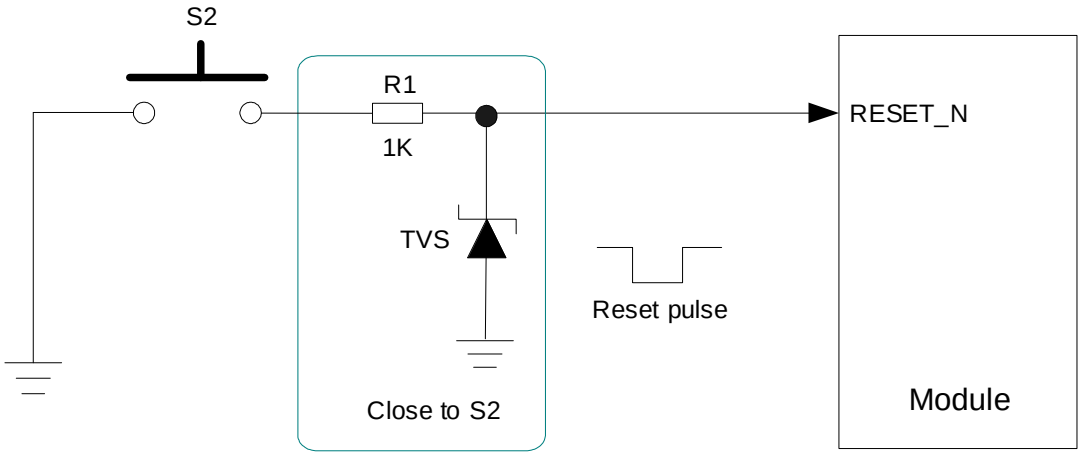


Figure 12: Reference Design of Reset with a Button

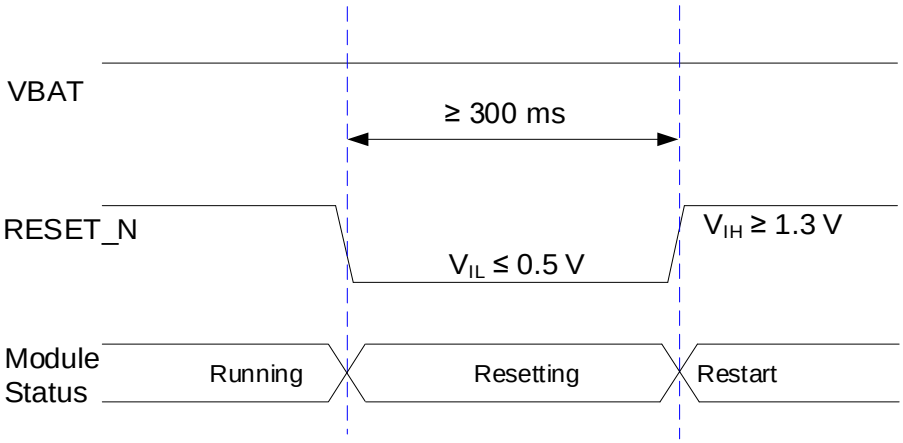


Figure 13: Timing of Reset

NOTE

1. Use RESET_N only when you fail to turn off the module with the APIs or PWRKEY.
2. Make sure the capacitance on PWRKEY and RESET_N never exceeds 10 nF.

4 Application Interfaces

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specifications and supports High-Speed (480 Mbps) and Full-Speed (12 Mbps) on USB 2.0. The USB interface can be used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 15: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	59	AIO	USB 2.0 differential data (+)	Complies with USB 2.0. A differential impedance of 90 Ω is needed. Test points must be reserved.
USB_DM	60	AIO	USB 2.0 differential data (-)	
USB_VBUS	61	AI	USB connection detect	Typical value is 5.0 V. A test point must be reserved.

It is recommended to use USB 2.0 interface for firmware upgrading and test points must be reserved for software debugging.

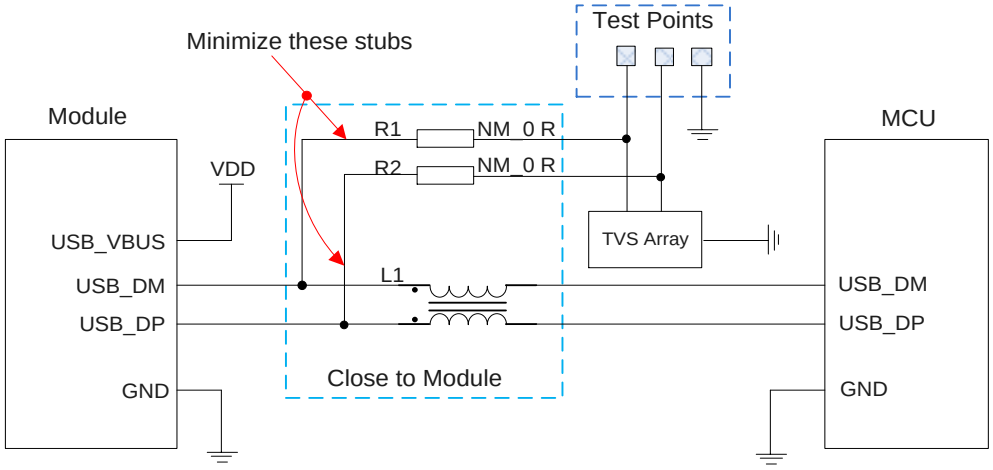


Figure 14: Reference Design of USB 2.0 Interface

It is recommended to add a common-mode choke L1 in series between MCU and the module to suppress EMI. Meanwhile, it is also suggested to add R1 and R2 in series between the module and test points for debugging. These resistors are not mounted by default. To ensure the signal integrity of USB 2.0 data transmission, L1, R1 and R2 should be placed close to the module, and resistors should be placed close to each other. Extra stubs of trace should be kept as short as possible.

To ensure performance, the following principles should be complied with when designing USB interface:

- The impedance of USB differential trace is 90 Ω. Route USB differential traces in the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Do not route signal traces under VBAT traces, crystal-oscillators, magnetic devices, sensitive circuits and provide clearance from RF signals, analog signals, and noise signals generated by clock and DC-DC.
- Pay attention to the impact caused by junction capacitance of the ESD protection component on USB data traces. Typically, junction capacitance should be less than 2 pF.

For more details about the USB specifications, visit http://www.usb.org/home.

4.2. Forced Download Interface

The module provides a USB_BOOT/KP_MKOUT[4] for forced download. You can make the module enter forced download mode by driving USB_BOOT/KP_MKOUT[4] low to GND before turning on the module. In this mode, the module supports firmware upgrade over USB 2.0 interface with shorter time period.

Table 16: Pin Description of USB_BOOT/KP_MKOUT[4]

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT/ KP_MKOUT[4]	82	DI	Force the module into download mode	1.8 V power domain. Active low. This pin cannot be pulled down to low level before the module starts up successfully. A test point is recommended to be reserved.

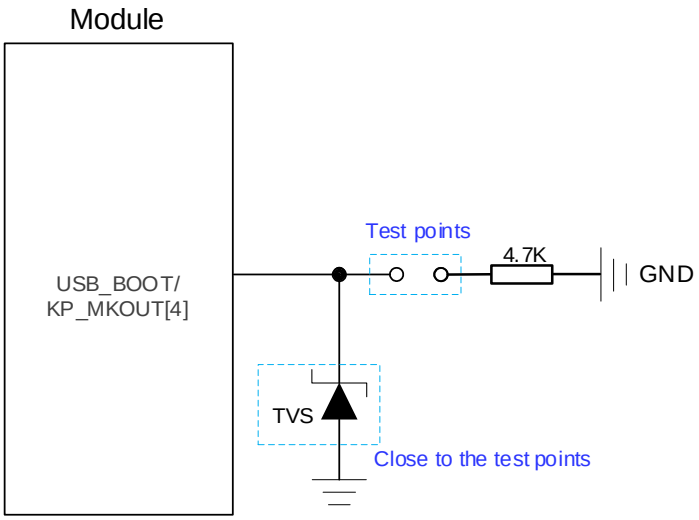


Figure 15: Reference Design of USB_BOOT

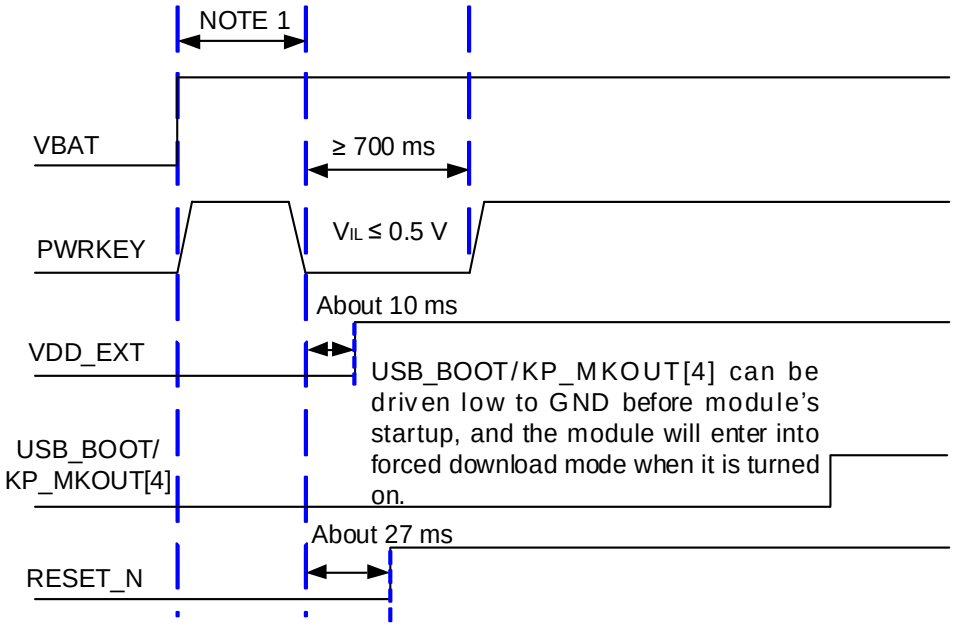


Figure 16: Timing of Entering Forced Download Mode

NOTE

1. Ensure VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low shall be at least 30 ms.
2. Follow the above timing when using MCU to control module to enter the forced download mode. Directly connect the test points as shown in ***Figure 15*** can manually force the module to enter download mode.
3. If pull USB_BOOT/KP_MKOUT[4] down to GND, the resistor is recommended to choose 4.7 kΩ.
4. Different tools must be used for firmware upgrade for QuecOpen and QuecPython solutions.

- QuecOpen: The 6.0 and above version QFlash tool must be used for firmware upgrade.
- QuecPython: The 3.3 and above version QPYcom tool must be used for firmware upgrade.

For more details about QPYcom tool, please visit https://python.quectel.com/doc/Application_guide/zh/dev-tools/QPYcom/index.html.

4.3. USIM Interfaces

The USIM interfaces meet ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V USIM card is supported, and Dual SIM Single Standby function is supported. USIM2 is optional, if it is required, contact Quectel Technical Support.

Table 17: Pin Description of USIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DATA	11	DIO	USIM1 card data	-
USIM1_RST	12	DO	USIM1 card reset	-
USIM1_CLK	13	DO	USIM1 card clock	-
USIM1_VDD	14	PO	USIM1 card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM1_DET	79	DI	USIM1 card hot-plug detect	If unused, keep it open.
USIM2_VDD	65	PO	USIM2 card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM2_DATA	64	DIO	USIM2 card data	-
USIM2_CLK	62	DO	USIM2 card clock	-
USIM2_RST	63	DO	USIM2 card reset	-

The module supports USIM card hot-plug via USIM_DET (level trigger pin), and both high-level and low-level detections are supported. The function can be configured through API.

The following table shows the related API of configuring USIM card hot-plug function.

Table 18: Related API of Configuring USIM Card Hot-plug Function

	QuecOpen	QuecPython
API	*ql_sim_config_hot_plug_detect*	*sim.setSimDet*

NOTE

For more details about API of configuring USIM card hot-plug function:

- QuecOpen: See ***document [6]***;
- QuecPython: Please visit https://python.quectel.com/doc/API_reference/zh/iotlib/sim.html.

The following figure shows a reference design for USIM card interface with an 8-pin USIM card connector.

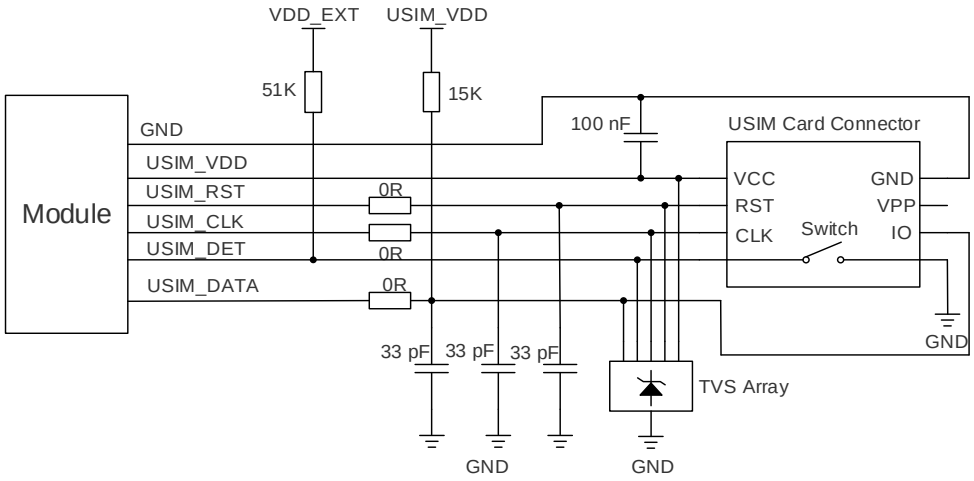


Figure 17: Reference Design of USIM Interface with an 8-pin USIM Card Connector

If the USIM card detection function is not needed, keep USIM_DET open. A reference circuit for USIM interface with a 6-pin USIM card connector is illustrated in the following figure.

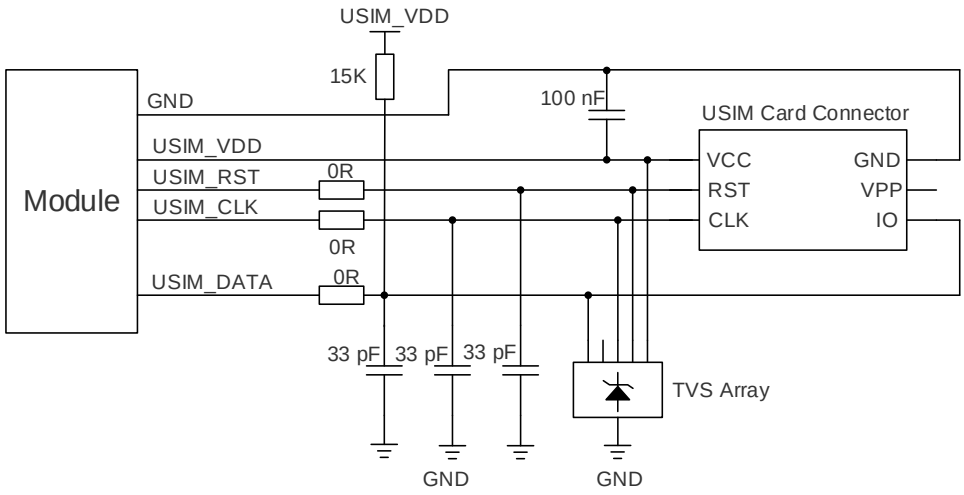


Figure 18: Reference Design of USIM Interface with a 6-pin USIM Card Connector

To enhance the reliability and availability of the USIM card in applications, follow the notes below for the USIM circuit design:

- Place USIM card connector close to the module. Keep the trace length as short possible, at most 200 mm.
- Keep USIM card signals away from RF and power supply traces.
- Ensure the bypass capacitor between USIM_VDD and GND does not exceed 1 μF, and the capacitor should be placed close to the USIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, add a TVS array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the USIM card to facilitate debugging. The 33 pF capacitors in parallel on USIM_DATA, USIM_CLK and USIM_RST traces are used for filtering RF interference. Additionally, keep the USIM peripheral circuit close to the USIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the USIM card. If the USIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the USIM card connector.

NOTE

Only USIM1 supports hot-plug function.

4.4. UART

The module provides three UARTs: main UART, debug UART and auxiliary UART.

Table 19: UART Information

UART Types	Supported Baud Rates (bps)	Default Baud Rates (bps)	Functions
Main UART	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	115200	Data transmission and AT command communication
Debug UART	115200	115200	Partial log output
Auxiliary UART	115200	115200	Communication with peripherals

Table 20: Pin Description of UARTs

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RXD	17	DI	Main UART receive	1.8 V power domain. If unused, keep them open.
MAIN_TXD	18	DO	Main UART transmit	
MAIN_DTR	19	DI	Main UART data terminal ready	
MAIN_RI	20	DO	Main UART ring indication	
MAIN_DCD	21	DO	Main UART data carrier detect	
MAIN_CTS	22	DO	Clear to send signal from the module	1.8 V power domain. Connect to the MCU's CTS. If unused, keep it open.
MAIN_RTS	23	DI	Request to send signal to the module	1.8 V power domain. Connect to the MCU's RTS. If unused, keep it open.
AUX_RXD	28	DI	Auxiliary UART receive	1.8 V power domain. If unused, keep them open.
AUX_TXD	29	DO	Auxiliary UART transmit	
DBG_RXD	38	DI	Debug UART receive	1.8 V power domain. Test points must be reserved.
DBG_TXD	39	DO	Debug UART transmit	

The module provides 1.8 V UART. You can use a voltage-level translator between the module and the MCU's UART if the application is equipped with a 3.3 V UART. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design:

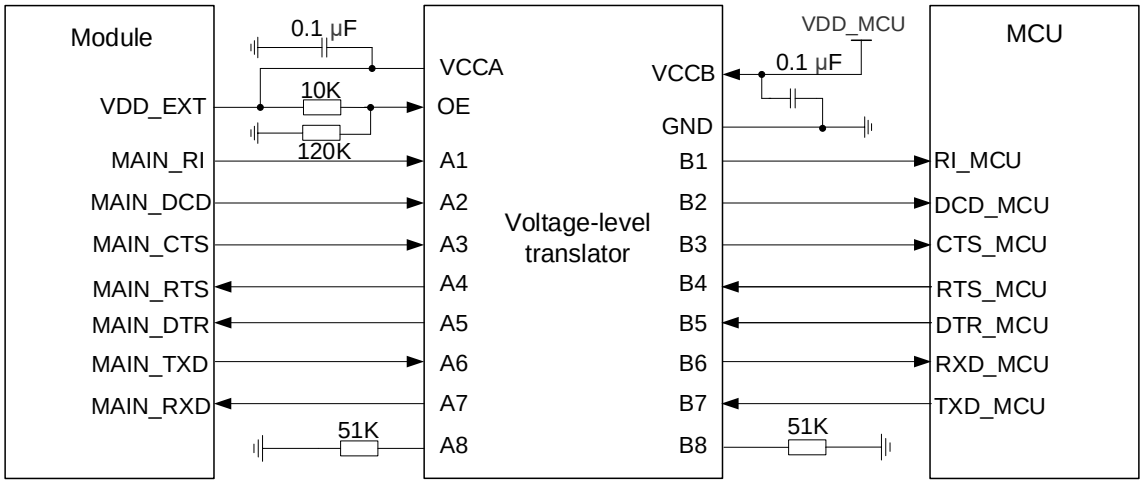


Figure 19: Reference Design of UART with a Voltage-level Translator

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

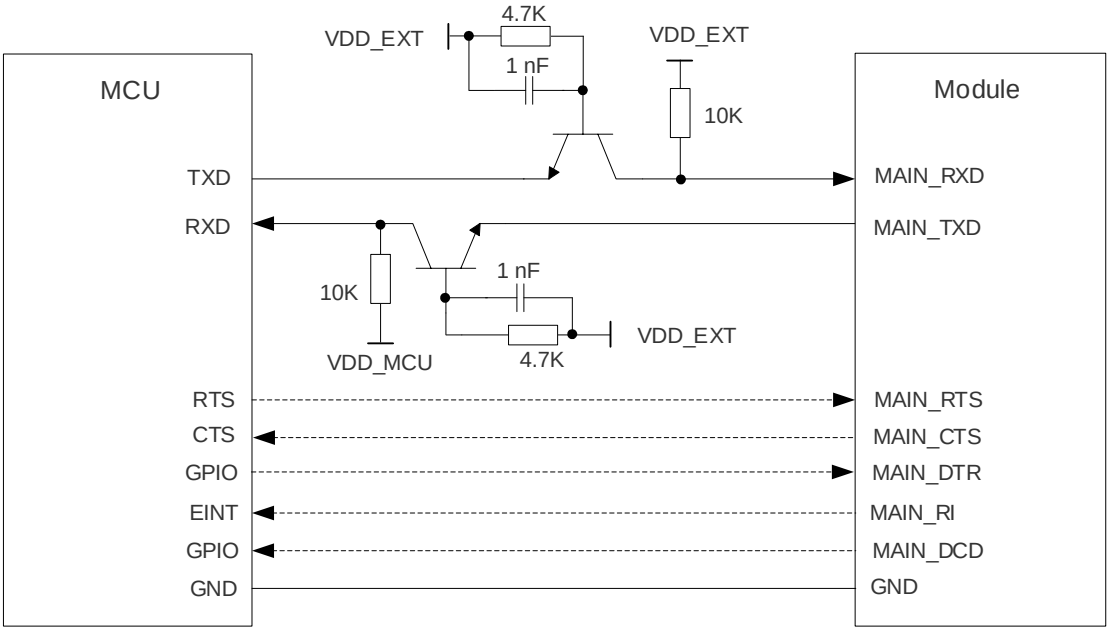


Figure 20: Reference Design of UART with Transistor Circuit

NOTE

1. Transistor circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
3. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

4.5. PCM and I2C Interfaces (Optional)

The module provides one PCM interface and two I2C interfaces.

Table 21: Pin Description of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_CLK	30	DO	PCM clock	1.8 V power domain. If unused, keep them open.
PCM_SYNC	31	DO	PCM data frame sync	
PCM_DIN	32	DI	PCM data input	
PCM_DOUT	33	DO	PCM data output	

Table 22: Pin Description of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C2_SDA	66	OD	I2C2 serial data	An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C2_SCL	67	OD	I2C2 serial clock	
I2C1_SDA	69	OD	I2C1 serial data	
I2C1_SCL	68	OD	I2C1 serial clock	

The PCM interface supports primary mode (short frame synchronization), and the module only works as a master device.

The module supports 16-bit linear data format. The following figures show the short frame mode's timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 2048 kHz).

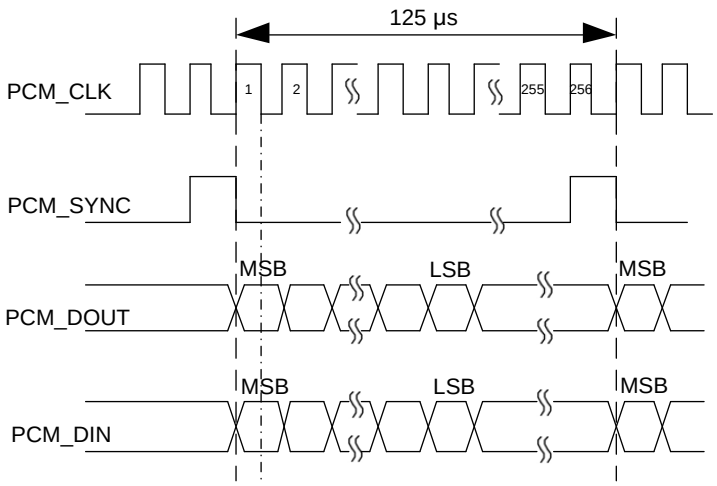


Figure 21: Timing of Short Frame Mode

In short frame mode, data is sampled on the falling edge of PCM_CLK, and transmitted on the rising edge. The falling edge of PCM_SYNC represents the MSB. In this mode, the PCM_CLK supports 256 kHz, 512 kHz, 1024 kHz, and 2048 kHz when PCM_SYNC operates at 8 kHz, and also supports 4096 kHz when PCM_SYNC operates at 16 kHz.

The default configuration is short frame mode, PCM_CLK = 2048 kHz, PCM_SYNC = 8 kHz.

The following figure shows a reference design of I2C and PCM interfaces with an external codec IC.

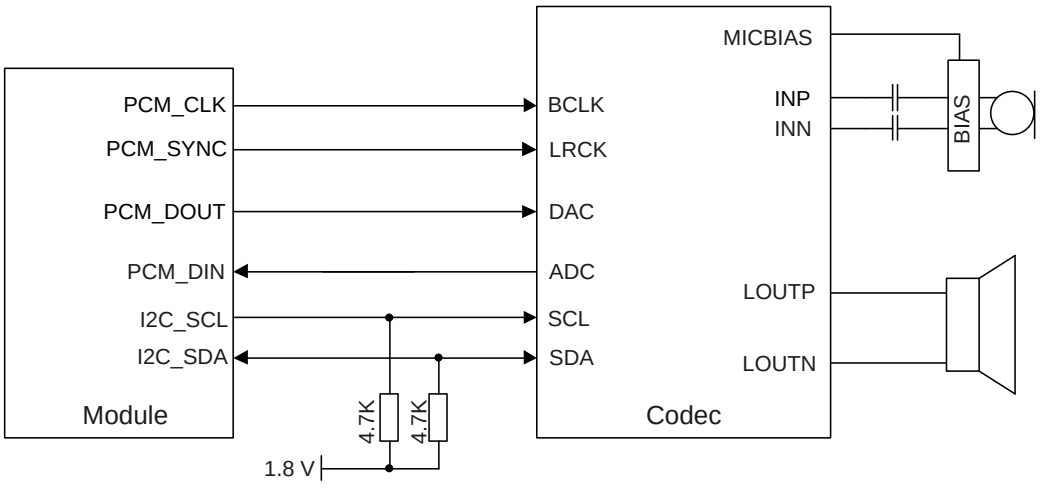


Figure 22: Reference Design of PCM and I2C Interfaces

NOTE

1. PCM and I2C function are optional. If these interfaces are not used, keep them open.
2. It is recommended to reserve an RC (R = 0 Ω, C = 33 pF) circuit on the PCM traces, especially for PCM_CLK.
3. The module can only be used as a master device in applications related to PCM and I2C interfaces.

4.6. SPI

The module's SPI supports slave mode* and master mode (default), the power domain of SPI is 1.8 V and a maximum clock frequency is 26 MHz. Pins 30–33 are used for PCM function by default, and SPI function can be realized by multiplexing from PCM interface.

Table 23: Pin Description of SPI Interface

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
PCM_CLK	30	SPI0_CLK	DIO	SPI clock	1.8 V power domain. If unused, keep them open. When the module is used as master device, SPI0_CLK and SPI0_CS pins are output signals; when the module is used as slave device*, SPI0_CLK and SPI0_CS pins are input signals.
PCM_SYNC	31	SPI0_CS	DIO	SPI chip select	
PCM_DIN	32	SPI0_DOUT	DO	SPI data output	
PCM_DOUT	33	SPI0_DIN	DI	SPI data input	

The following figure shows a reference design of SPI connected peripherals' circuit:

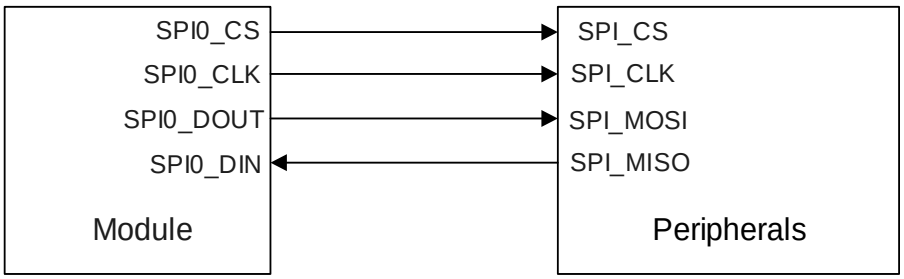


Figure 23: Reference Design of SPI Circuit (Module as Master Device)

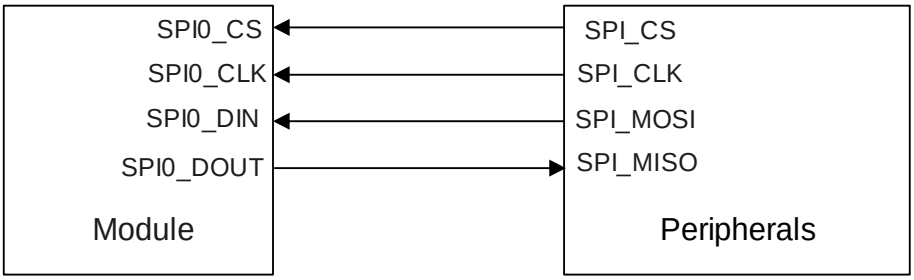


Figure 24: Reference Design of SPI Circuit (Module as Slave Device*)

NOTE

1. The module provides 1.8 V SPI interface. Use a voltage-level translator if the application is equipped with a 3.3 V system.
2. For more information about multiplexing, see ***document [7]***.

4.7. LCM Interface

The module's LCM interface supports display module with a maximum resolution of 240 × 320. The module supports four-wire single data line transmission of SPI, and supports RGB565 format output.

Table 24: Pin Description of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_RST	49	DO	LCD reset	1.8 V power domain. If unused, keep them open.
LCD_SPI_DOUT	50	DO	LCD SPI data output	
LCD_SPI_RS	51	DO	LCD SPI register select	
LCD_SPI_CS	52	DO	LCD SPI chip select	
LCD_SPI_CLK	53	DO	LCD SPI clock	
LCD_TE	78	DI	LCD tearing effect	

The reference design of LCM interface, see ***document [8]***.

4.8. Matrix Keypad Interfaces

The module supports 3 × 3 matrix keypad interfaces.

Table 25: Pin Description of Matrix Keypad Interfaces

Pin Name	Pin No.	I/O	Description	Comment
KP_MKOUT[5]	74	DO	matrix keypad output 5	1.8 V power domain. If unused, keep them open.
KP_MKIN[5]	75	DI	matrix keypad input 5	
KP_MKOUT[2]	76	DO	matrix keypad output 2	
KP_MKIN[2]	77	DI	matrix keypad input 2	
USB_BOOT/KP_MKOUT[4]	82	DO	matrix keypad output 4	
KP_MKIN[4]	83	DI	matrix keypad input 4	

The reference design of matrix keypad interface, see ***document [8]***.

4.9. Camera Interface

The module's camera interface supports up to 0.3 MP and supports the single data line or dual data line transmission of SPI.

Table 26: Pin Description of Camera Interface

Pin Name	Pin No.	I/O	Description	Comment
CAM_MCLK	54	DO	Camera master clock	1.8 V power domain. If unused, keep them open.
CAM_SPI_DATA0	55	DI	Camera SPI data bit 0	
CAM_SPI_DATA1	56	DI	Camera SPI data bit 1	
CAM_I2C_SCL	57	OD	Camera I2C clock	Pull each of them up to 1.8 V power domain with an external resistor. If unused, keep them open.
CAM_I2C_SDA	58	OD	Camera I2C data	
CAM_SPI_CLK	80	DI	Camera SPI clock	1.8 V power domain. If unused, keep them open.

CAM_PWDN	81	DO	Camera power down	
CAM_VDD	8	PO	Camera power supply	2.8 V/ 100 mA. If unused, keep them open.

The reference design of camera interface, see ***document [8]***.

NOTE

An LDO or the module's VDD_EXT can be used as the camera's CAM_VDDIO.

4.10. Analog Audio Interfaces (Optional)

The module provides one analog input channel and one analog output channel.

Table 27: Pin Description of Analog Audio Interface

Pin Name	Pin No.	I/O	Description	Comment
MIC_P	3	AI	Microphone analog input (+)	If unused, keep them open.
MIC_N	4	AI	Microphone analog input (-)	
SPK_P	5	AO	Analog audio differential output (+)	Used for earpiece. The interface can drive 32 Ω earpiece with power rate at 37 mW @ THD = 1 %. It can also be used to drive external power amplifier devices if the output power rate cannot meet the demand. If unused, keep them open.
SPK_N	6	AO	Analog audio differential output (-)	

- AIN channel is a differential input channel, which can be applied to the input from a microphone (usually an electret microphone is used).
- AOUT channel is a differential output channel, which can be applied to the output through a loudspeaker or an earpiece.
- The module's internal audio amplifier is configured as Class AB by default.

NOTE

The analog audio function is optional. If these interfaces are not used, keep them open.

4.10.1. Audio Interface Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) to filter out RF interference, thus reducing noise. Without these capacitors, noise could be heard during the call. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor to filter out high-frequency noises.

The filter capacitors on the PCB should be placed as close as possible to the audio device or audio interface, and the trace should be as short as possible. The filter capacitors should be passed before reaching other connection points.

To decrease radio or other signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.10.2. Microphone Interface Reference Design

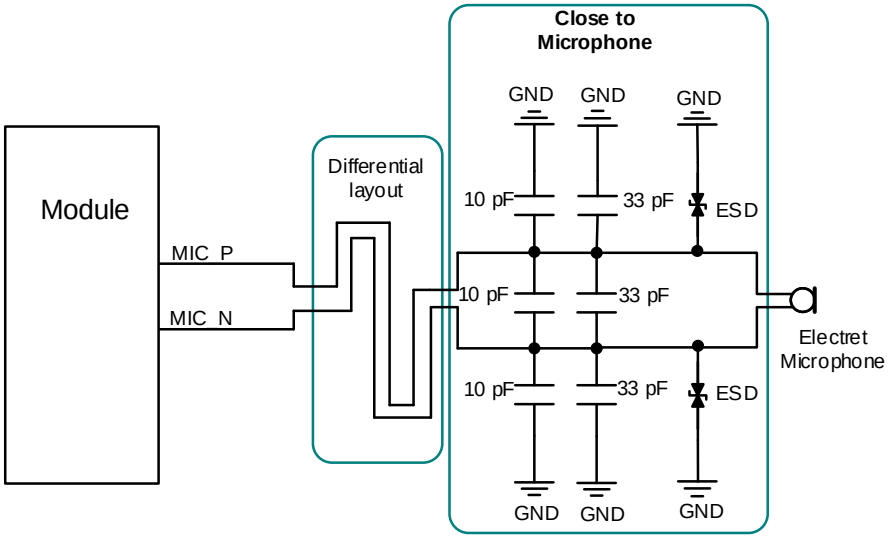


Figure 25: Reference Design of Microphone Interface

NOTE

MIC channel is sensitive to ESD, so do not remove the ESD protection components used to protect the MIC.

4.10.3. Earpiece Interface Reference Design

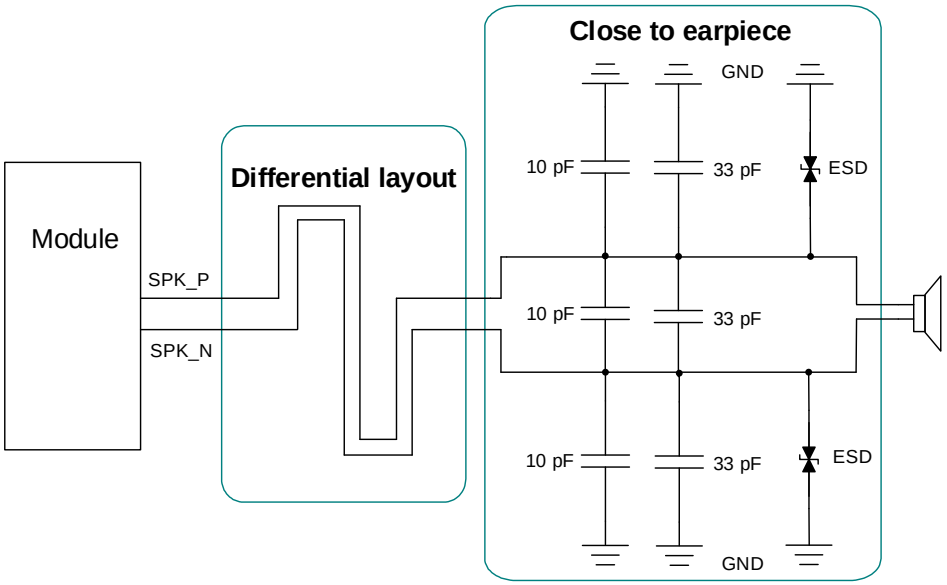


Figure 26: Reference Design of Earpiece Interface

4.10.4. Loudspeaker Interface Reference Design

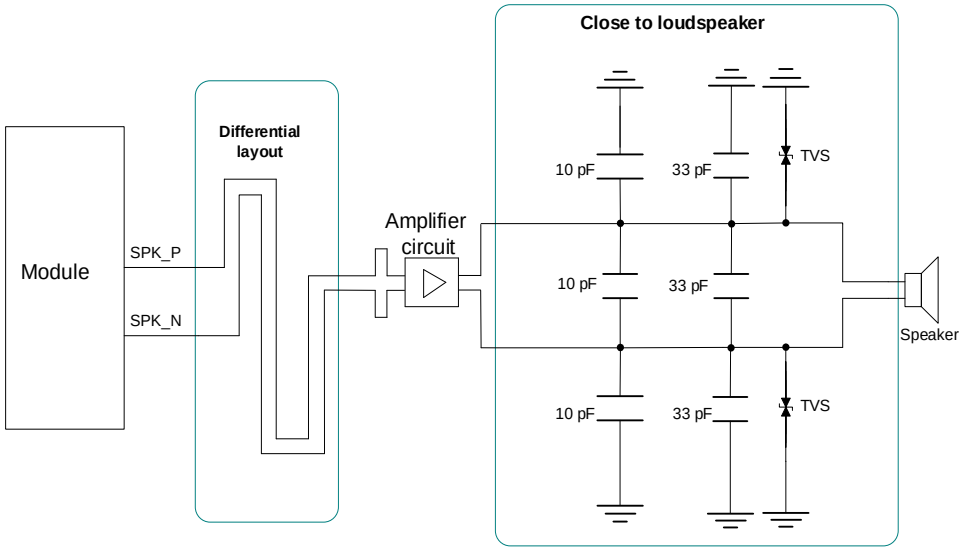


Figure 27: Reference Design of Loudspeaker Interface

For differential input and output audio power amplifiers, please visit http://www.ti.com/ to obtain the required devices. There are also many audio power amplifiers with the same performance to choose from the market.

4.11. ADC Interfaces

The module provides two ADC interfaces. To improve the accuracy of ADC, the trace of ADC interfaces should be surrounded by ground.

Table 28: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	9	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	96	AI		

You can use the following API to read the voltage value of ADC0 and ADC1.

Table 29: Related API of ADC Interfaces

	QuecOpen	QuecPython
API	*ql_adc_read()*	*ADC.read()*

Table 30: Characteristics of ADC Interfaces

Parameters	Min.	Typ.	Max.	Units
ADC0 input voltage range	0	-	1.2	V
ADC1 input voltage range	0	-	1.2	V
ADC resolution	-	-	12	bits

NOTE

1. A voltage divider circuit with two resistors must be used for ADC0 and ADC1 respectively, and the required resistance of the two resistors that connected to power supply is between 100 kΩ and 1 MΩ.
2. The accuracy of the two resistors in each voltage divider affects the sampling error of the ADC. It is recommended to use resistors with an accuracy of 1 %, if the accuracy of the ADC needs to be higher, resistors with an accuracy of 0.5 % are recommended. See ***document [8]*** for details.
3. For more details about API of ADC Interfaces:
   - QuecOpen: See ***document [4]***;
   - QuecPython: Please visit https://python.quectel.com/doc/API_reference/zh/peripherals/misc.ADC.html.

4.12. Indication Signal

Table 31: Pin Description of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	16	DO	Indicate the module's network activity status	1.8 V power domain. If unused, keep them open.
STATUS	25	DO	Indicate the module's operation status	

4.12.1. Network Status Indication

The module provides one network status indication pin: NET_STATUS for module's network activity status indication. This pin can be used to drive corresponding LED.

Table 32: Network Status Indication Pin Level Status and Module Network Status

Pin Name	Level Status	Module Network Status
NET_STATUS	Blink slowly (200 ms high level/1800 ms low level)	Network searching
	Blink slowly (1800 ms high level/200 ms low level)	Idle
	Blink quickly (125 ms high level/125 ms low level)	Data transmitting
	High level	Voice calling

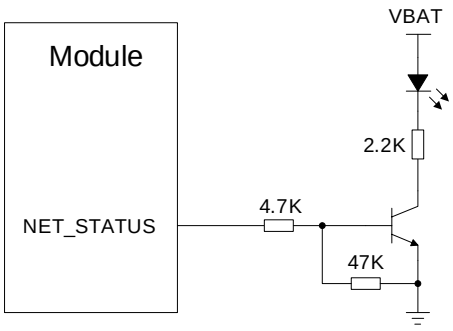


Figure 28: Reference Design of Network Status Indication

4.12.2. STATUS

STATUS indicates the module's operation status. It will output high level when module is turned on successfully.

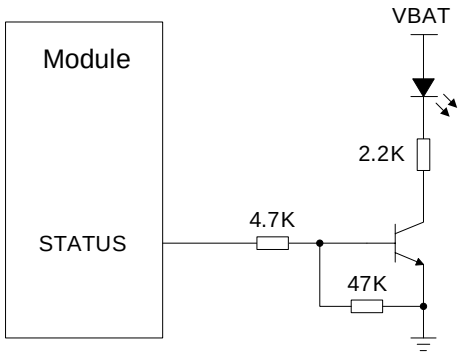


Figure 29: Reference Design of STATUS

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. LTE/Wi-Fi Scan Antenna Interface

5.1.1. Antenna Interface & Frequency Bands

Table 33: Pin Description of LTE/Wi-Fi Scan Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	35	AIO	Main antenna/Wi-Fi Scan antenna interface	50 Ω characteristic impedance.

NOTE

The module supports Wi-Fi Scan function. Wi-Fi Scan function shares the same antenna interface with the main antenna. These two antennas should use TDM (Time Division Multiplexing) and cannot be used simultaneously. Wi-Fi Scan only supports receiving and does not support transmitting.

Table 34: Operating Frequency (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960

LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803

5.1.2. Antenna Tuner Control Interfaces

The module can use GRFC interfaces to control external antenna tuner.

Table 35: Pin Description of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	105	DO	Generic RF controller	1.8 V power domain. If unused, keep them open.
GRFC2	104	DO		

Table 36: Truth Table of GRFC Interfaces (Unit: MHz)

GRFC1 Level	GRFC2 Level	Frequency Range	Bands
Low	Low	703–748	LTE B28
Low	High	824–849 832–862	LTE B5/B20
High	Low	880–915	LTE B8
High	High	1920–1980 1710–1785 2500–2570	LTE B1/B3/B7

5.1.3. Transmitting Power

Table 37: RF Transmitting Power

Frequency	Max.	Min.
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm

5.1.4. Receiver Sensitivity

Table 38: Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO	
LTE-FDD B1 (10 MHz)	-98.5	-	-	-96.3
LTE-FDD B3 (10 MHz)	-98.5	-	-	-93.3
LTE-FDD B5 (10 MHz)	-99	-	-	-94.3
LTE-FDD B7 (10 MHz)	-97	-	-	-94.3
LTE-FDD B8 (10 MHz)	-99	-	-	-93.3
LTE-FDD B20 (10 MHz)	-99.5	-	-	-93.3
LTE-FDD B28 (10 MHz)	-99.5	-	-	-94.8

5.1.5. Reference Design

Use a dual L-type matching circuit for all the antenna interfaces for better cellular performance. C1/C2 are not mounted by default.

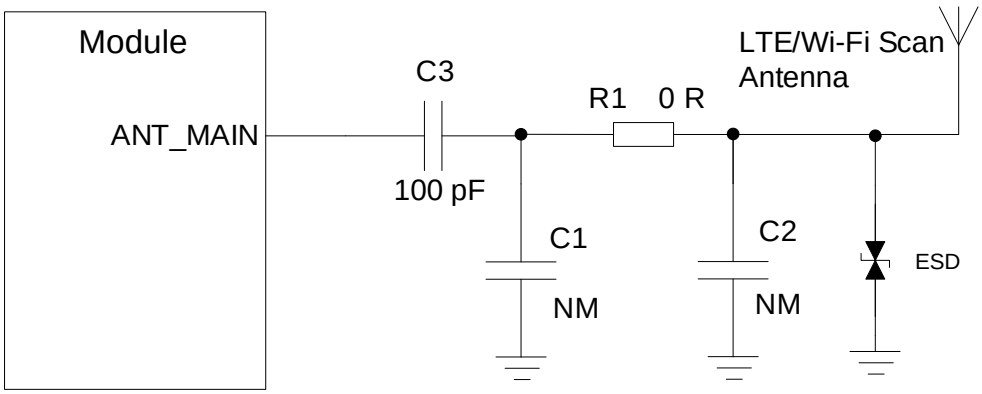


Figure 30: Reference Design of LTE/Wi-Fi Scan Antenna

NOTE

1. To reduce the coexistence problems and avoid the interference of receiving sensitivity, make sure that the isolation between antennas is not less than 20 dB.
2. Place the dual L-type matching components (R1, C1, C2, C3) as close to antennas as possible.
3. The junction capacitance of the ESD protection component on the antenna interface is recommended to be less than 0.05 pF.
4. If there is DC power at the antenna ports, C3 must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C3 should not be reserved.

5.2. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

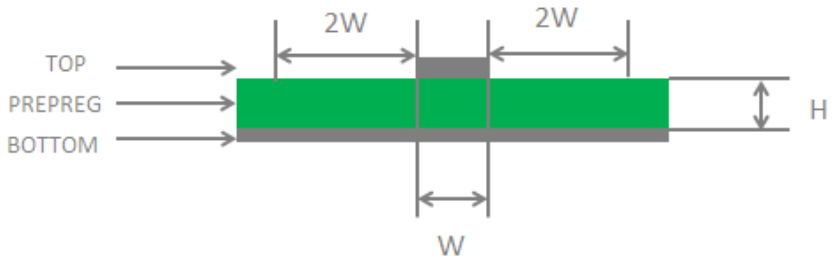


Figure 31: Microstrip Design on a 2-layer PCB

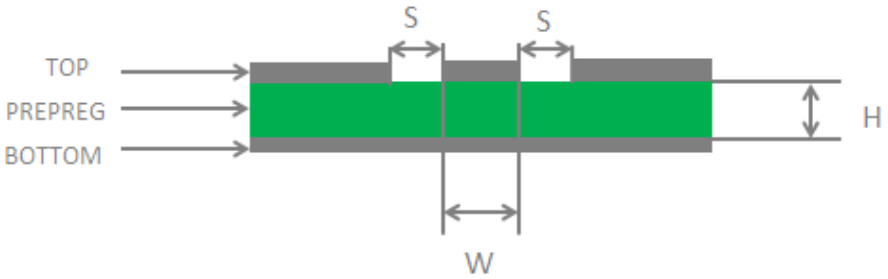


Figure 32: Coplanar Waveguide Design on a 2-layer PCB

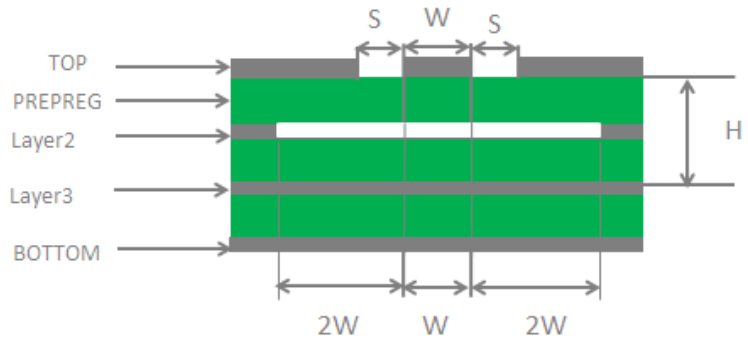


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

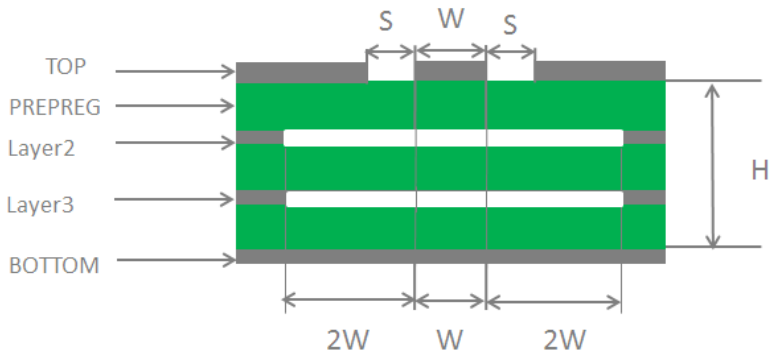


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [9]***.

5.3. Requirements for Antenna Design

Table 39: Requirements for Antenna Design

Antenna Types	Requirements
Cellular/Wi-Fi Scan	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Max input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

5.4. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

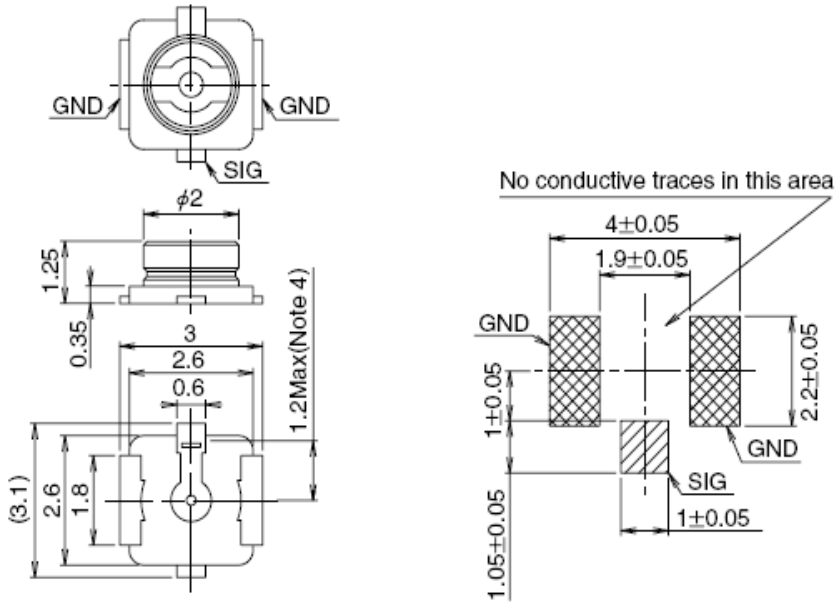


Figure 35: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

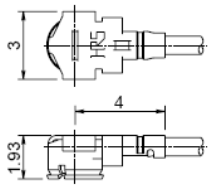
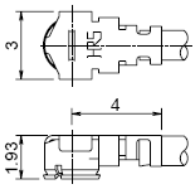
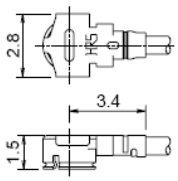
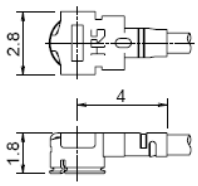
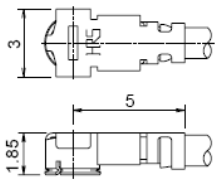
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 36: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connectors.

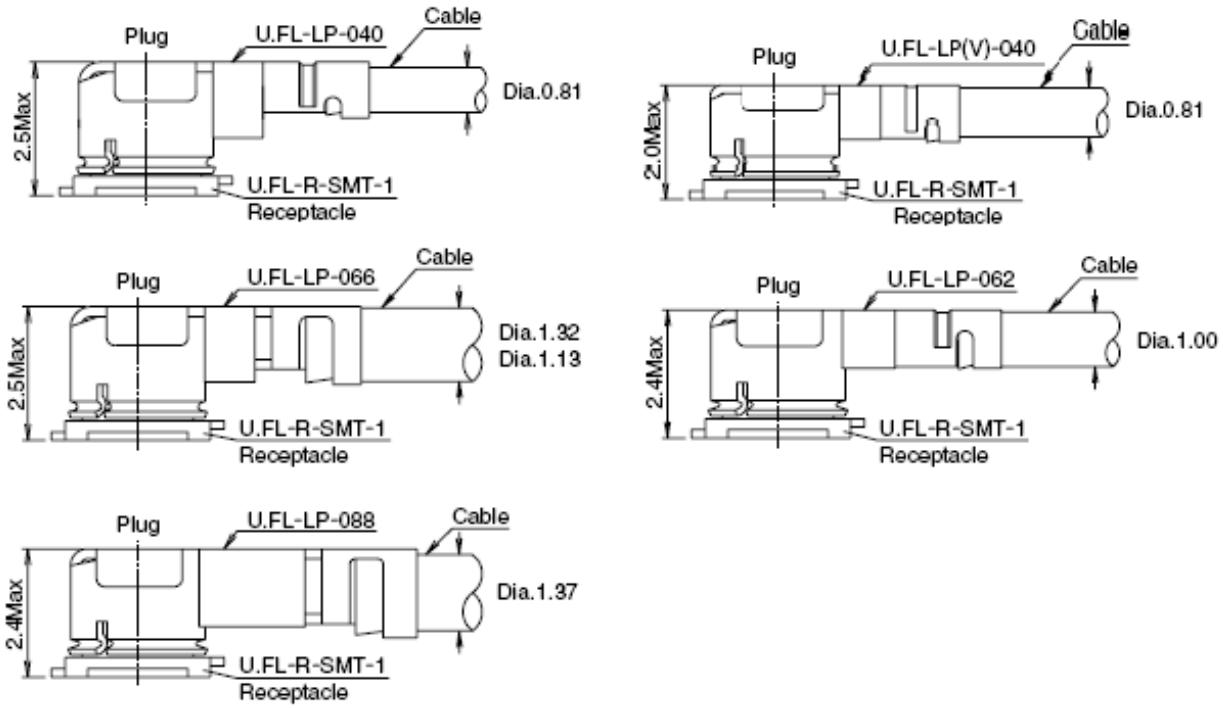


Figure 37: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Table 40: Absolute Maximum Ratings

Parameters	Min.	Max.	Unit
Voltage at VBAT	-0.3	6	V
Voltage at USB_VBUS	-0.3	5.5	V
Voltage at digital pins	-0.3	2.2	V
Voltage at ADC0	0	1.2	V
Voltage at ADC1	0	1.2	V
Current at VBAT	-	2	A

6.2. Power Supply Ratings

Table 41: Module Power Supply Ratings

Parameters	Descriptions	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltage must be within this range	3.4	3.8	4.3	V
I_{VBAT}	Peak supply consumption	At maximum power control level	-	1.5	2	A
USB_VBUS	USB connection detect	-	3.0	5.0	5.25	V

6.3. Power Consumption

Table 42: Power Consumption

State	Conditions	Typ.	Units
OFF state	Power down	17.62	μA
Sleep state	Minimum Functionality Mode (USB disconnected)	0.73	mA
	Airplane Mode (USB disconnected)	0.83	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.71	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.27	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.05	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.96	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	19.24	mA
	LTE-FDD @ PF = 64 (USB connected)	29.34	mA
LTE data transmission	LTE-FDD B1	564	mA
	LTE-FDD B3	532	mA
	LTE-FDD B5	530	mA
	LTE-FDD B7	633	mA
	LTE-FDD B8	547	mA
	LTE-FDD B20	526	mA
	LTE-FDD B28	576	mA

6.4. Digital I/O Characteristics

Table 43: 1.8 V I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	0.7 × VDDIO	VDDIO + 0.2
V_{IL}	Low-level input voltage	-0.3	0.3 × VDDIO
V_{OH}	High-level output voltage	VDDIO - 0.2	-
V_{OL}	Low-level output voltage	-	0.2

Table 44: USIM Low-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
USIM_VDD	Power supply	1.62	1.98
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD
V_{IL}	Low-level input voltage	0	0.2 × USIM_VDD
V_{OH}	High-level output voltage	0.7 × USIM_VDD	USIM_VDD
V_{OL}	Low-level output voltage	0	0.15 × USIM_VDD

Table 45: USIM High-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
USIM_VDD	Power supply	2.7	3.3
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD
V_{IL}	Low-level input voltage	0	0.15 × USIM_VDD
V_{OH}	High-level output voltage	0.7 × USIM_VDD	USIM_VDD
V_{OL}	Low-level output voltage	0	0.15 × USIM_VDD

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 46: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Test Points	Contact Discharge	Air Discharge	Unit
VBAT & GND	±5	±10	kV
All antenna interfaces	±4	±8	kV
Other interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 47: Operating and Storage Temperatures (Unit: °C)

Parameters	Min.	Typ.	Max.
Normal Operating Temperature [5]	-35	+25	+75
Extended Operating Temperature [6]	-40	-	+85
Storage Temperature	-40	-	+90

[5] Within this range, the module's indicators comply with 3GPP specification requirements.

[6] Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call*, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

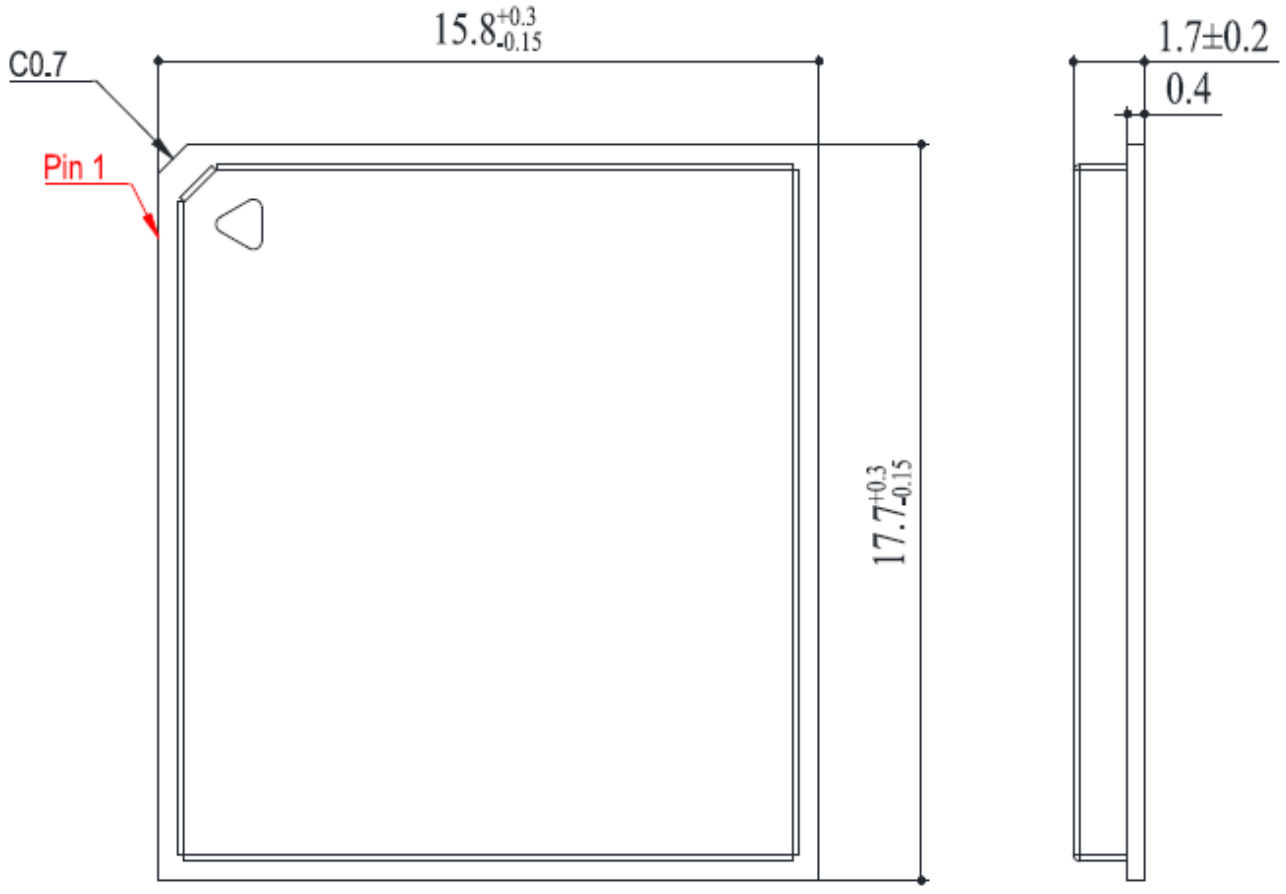


Figure 38: Module Top and Side Dimensions (unit: mm)

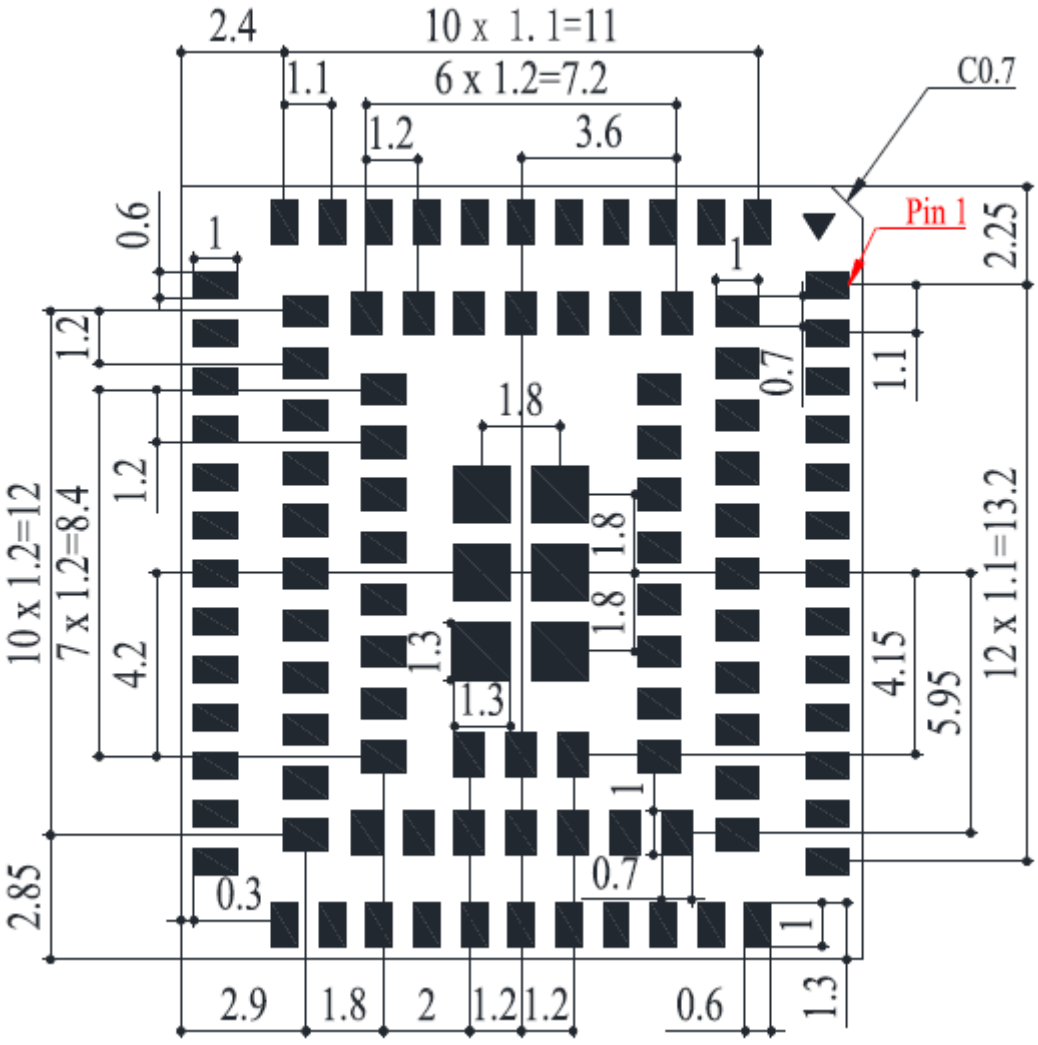


Figure 39: Module Bottom Dimensions (unit: mm)

NOTE

The package warpage level of the module refers to *JEITA ED-7306* standard.

7.2. Recommended Footprint

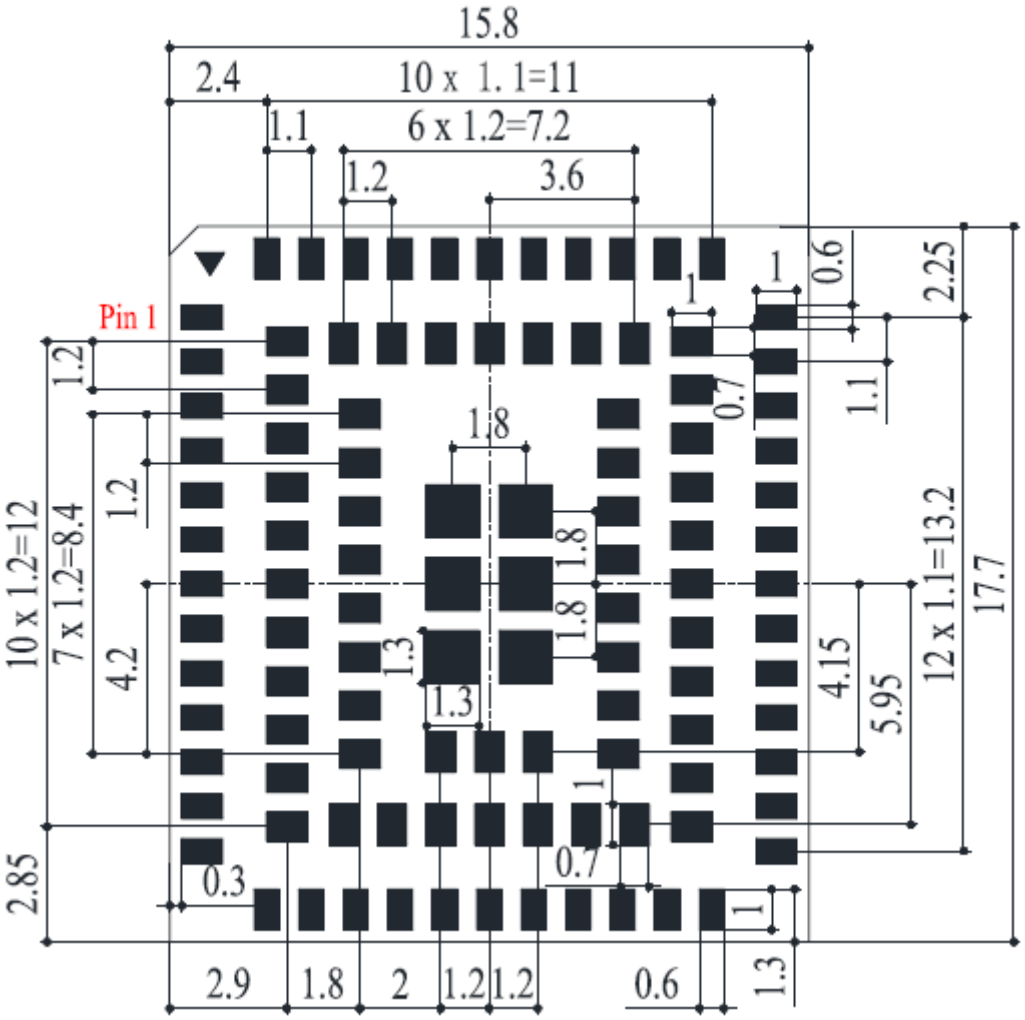


Figure 40: Recommended Footprint (unit: mm)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

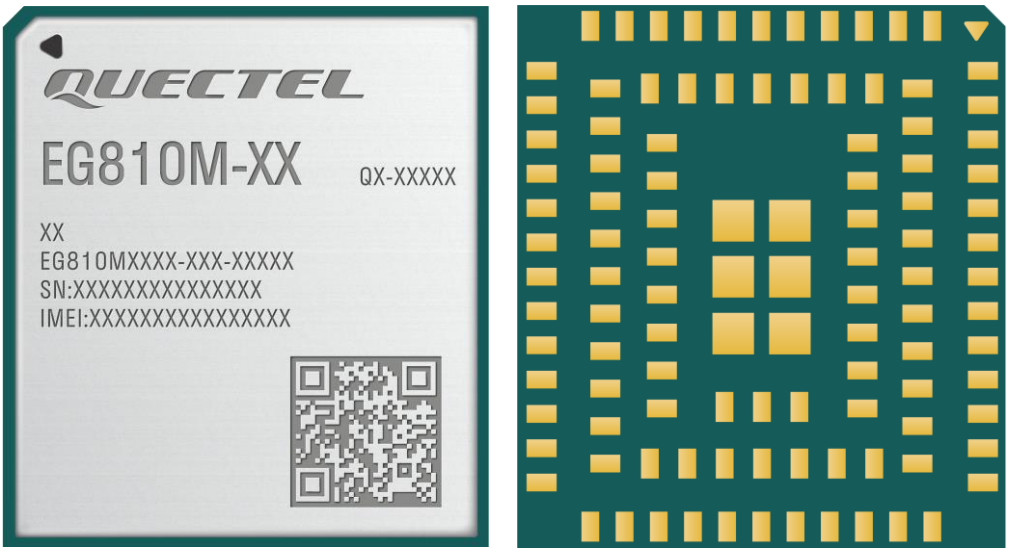


Figure 41: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [7] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[7] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [10]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

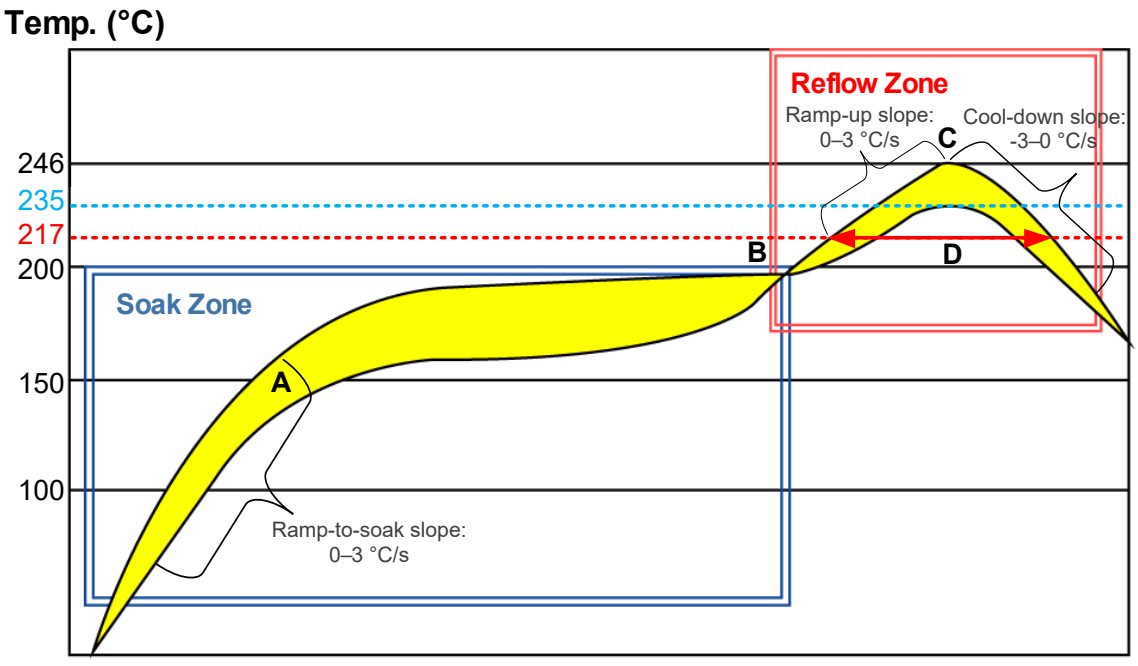


Figure 42: Recommended Reflow Soldering Thermal Profile

Table 48: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217°C)	40–70 s
Max Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [11]***.

8.3. Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

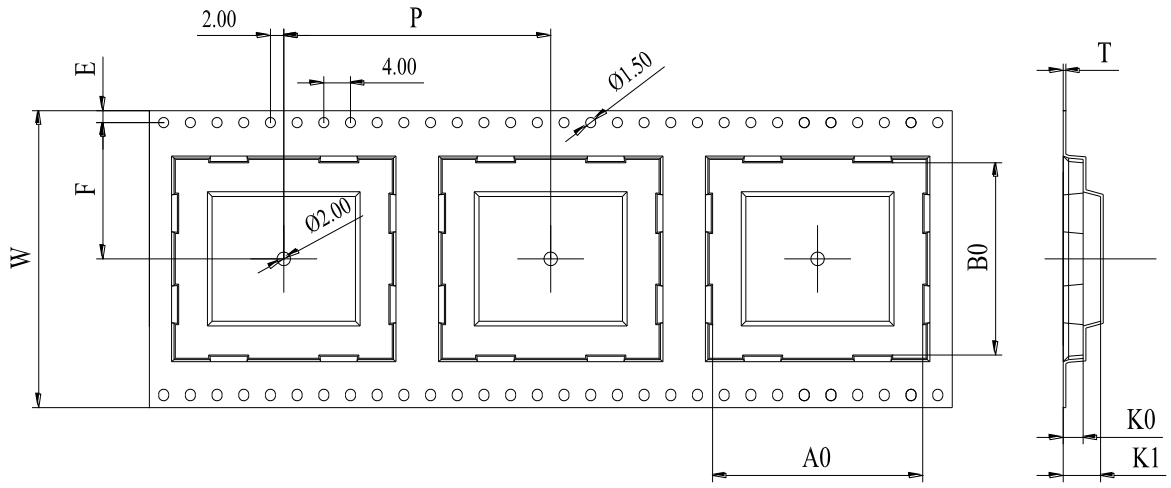


Figure 43: Carrier Tape Dimension Drawing (Unit: mm)

Table 49: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	24	0.4	16.2	18.1	2.2	7.6	14.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

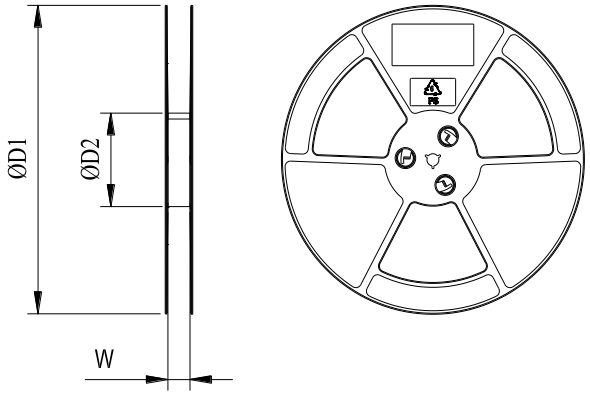


Figure 44: Plastic Reel Dimension Drawing

Table 50: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	32.5

8.3.3. Mounting Direction

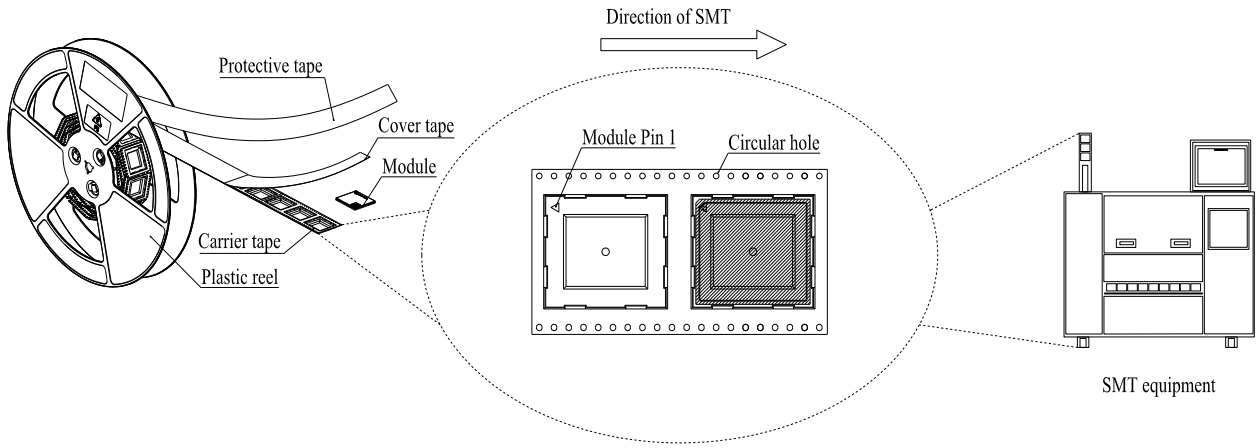
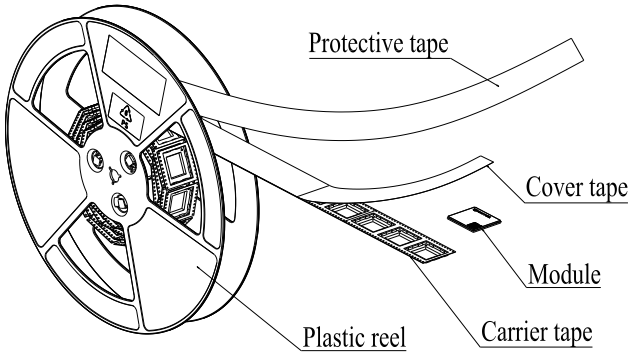


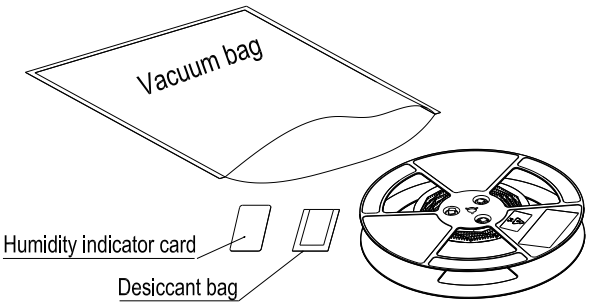
Figure 45: Mounting Direction

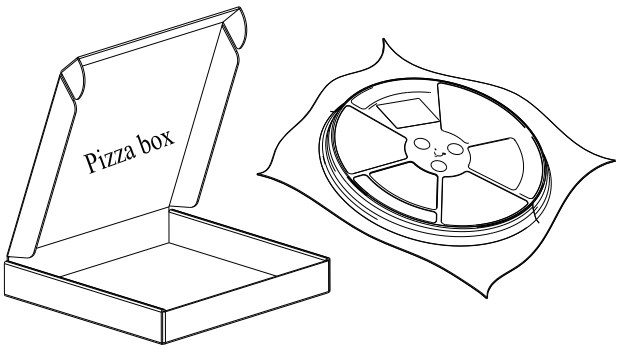
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

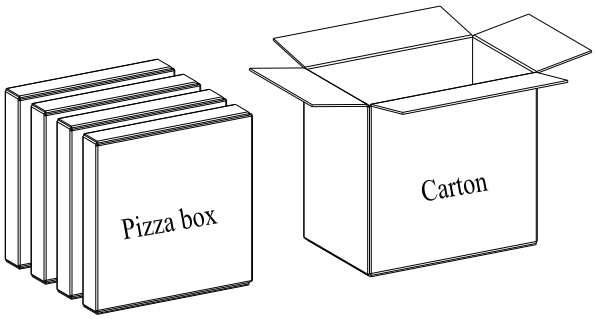


Figure 46: Packaging Process

9 Appendix References

Table 51: Related Documents

Document Name	
[1]	Quectel_LTE_OPEN_EVB_User_Guide
[2]	Quectel_EC200S&EC600M&EG800K&EG810M&EG91xN_Series_QuecOpen(SDK)_Device_Management_Guide
[3]	Quectel_EC200S&EC600M&EG800K&EG810M&EG91xN_Series_QuecOpen(SDK)_Low_Power_Mode_Development_Guide
[4]	Quectel_EC200S&EC600M&EG800K&EG810M&EG91xN_Series_QuecOpen(SDK)_ADC_Development_Guide
[5]	Quectel_EC200S&EC600M&EG800K&EG810M&EG91xN_Series_QuecOpen(SDK)_Booting&Shutdown_Development_Guide
[6]	Quectel_EC200S&EC600M&EG800K&EG810M&EG91xN_Series_QuecOpen(SDK)_SIM_Development_Guide
[7]	Quectel_EC800M&EG810M_Series_QuecOpen_GPIO_Configuration
[8]	Quectel_EG810M-EU_QuecOpen_Reference_Design
[9]	Quectel_RF_Layout_Application_Note
[10]	Quectel_Module_Stencil_Design_Requirements
[11]	Quectel_Module_SMT_Application_Note

Table 52: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
API	Application Programming Interface
bps	Bits per second
CHAP	Challenge Handshake Authentication Protocol

CMUX	Connection MUX
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over-The-Air
DRX	Discontinuous Reception
DSSS	Dual Sim Single Standby
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FDD	Frequency Division Duplexing
FILE	File Protocol
FTP	File Transfer Protocol
FTPS	FTP over SSL
GND	Ground
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IMS	IP Multimedia Subsystem
IMT-2000	International Mobile Telecommunications 2000
$I_O$max	Maximum Output Load Current
LCD	Liquid Crystal Display
LCM	LCD Module
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution

M2M	Machine to Machine
MCU	Microcontroller Unit
ME	Mobile Equipment
MLCC	Multi-layer Ceramic Capacitor
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PF	Paging Frame
PING	Packet Internet Groper
PMU	Power Management Unit
PPP	Point-to-Point Protocol
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SMD	Surface Mount Device
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SPI	Serial Peripheral Interface
SSL	Secure Sockets Layer

TCP	Transmission Control Protocol
THD	Total Harmonic Distortion
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
USIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
V_{RWM}	Working Peak Reverse Voltage
VSWR	Voltage Standing Wave Ratio