EC800M-CN QuecOpen Reference Design

LTE Standard Module Series

Version: 1.1

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Status: Released

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About the Document

Revision History

Version	Date	Author	Description
	2022-06-01	Mark YANG	Creation of the document
1.0	2022-09-26	Mark YANG	First official release
1.1	2023-01-05	Howell KANG/ Cuby LI	1. Added Bluetooth Interface Design (Sheets 1, 3 and 18). 2. Reserved test points for RESET_N and VDD_EXT (Sheets 1 and 17). 3. Added USB insertion enables automatic boot circuit (Sheet 4). 4. Added 1.8 pF and 3.9 pF ceramic capacitors, a 0 Ω resistor and related notes in VBAT design (Sheet 5). 5. Added resistors R0707 and R0708 (Sheet 7). 6. Added the note about reserving 33 pF capacitor of Audio Codec Design (Sheet 14).

Contents

1 Reference Design

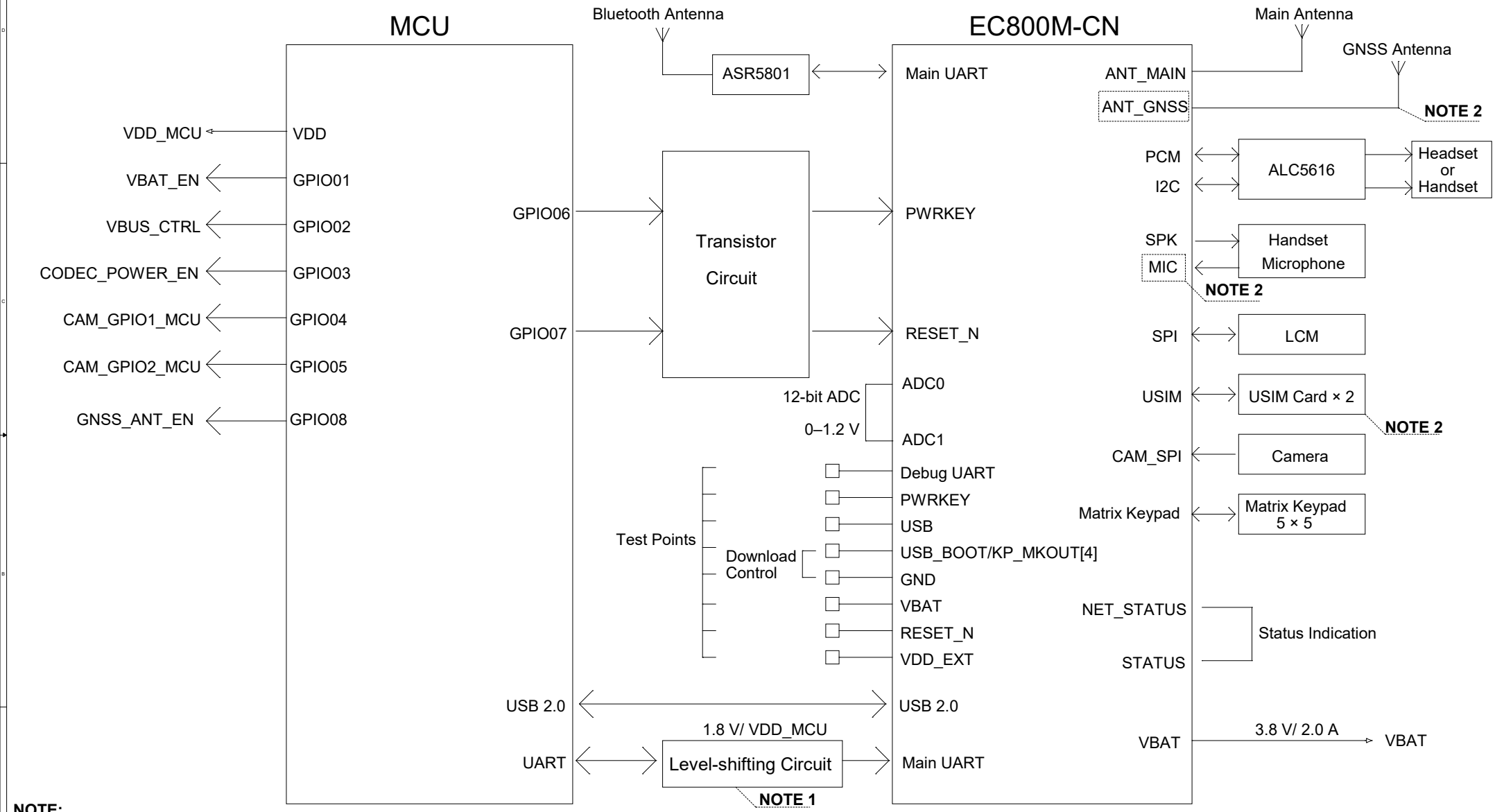
1.1. Introduction

This document provides the reference design for Quectel EC800M-CN QuecOpen® module.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



NOTE:

1. A level-shifting circuit or a voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.

2. GNSS function of the module is optional.

   a) If the module with GNSS function is selected, the analog audio input channel requires an external microphone bias circuit. And MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO. Only USIM1 interface is supported on this condition.

   b) If the module without GNSS function is selected, the analog audio input channel requires no external microphone bias circuit; and dual USIM cards are supported in this situation.

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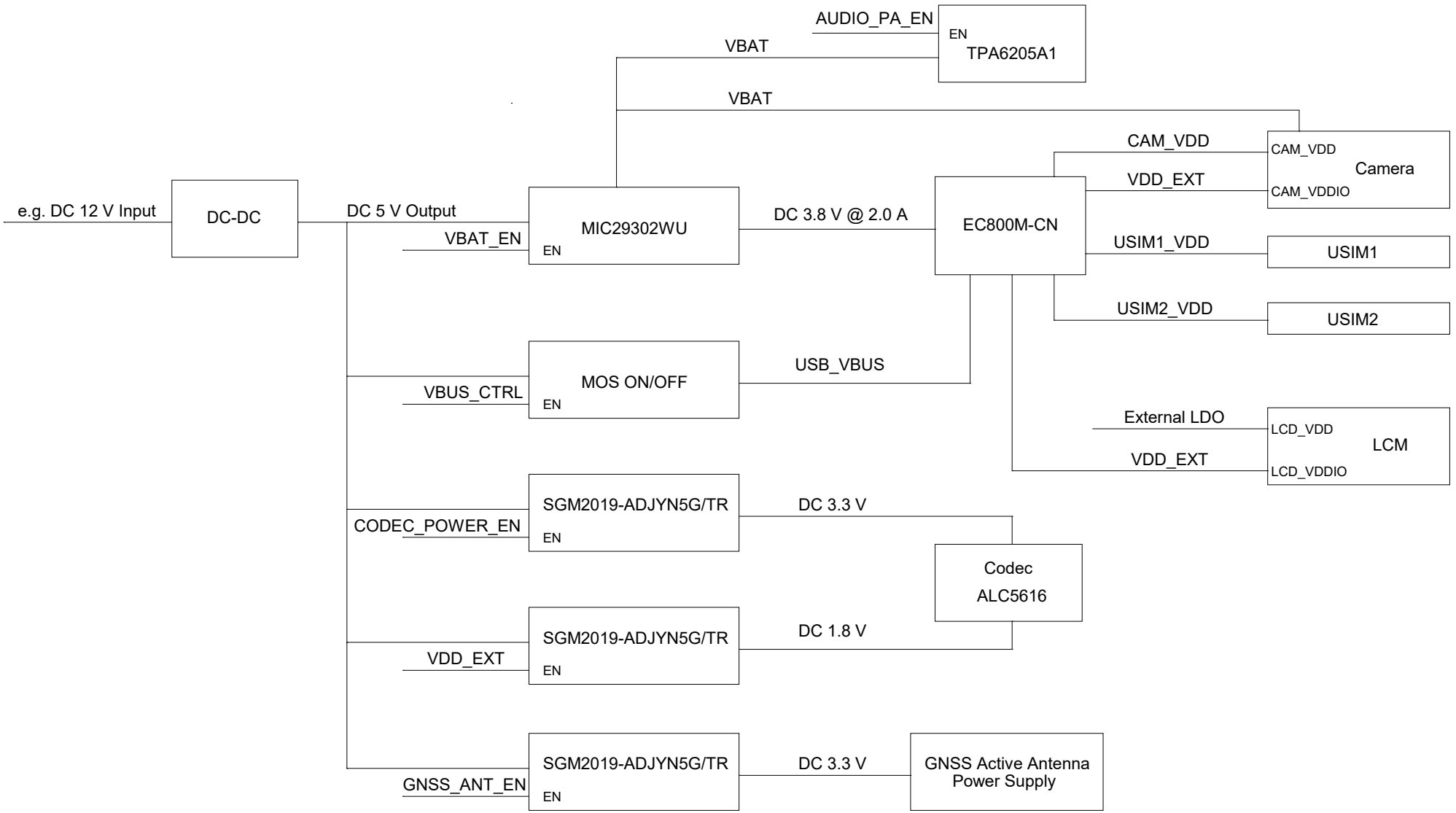
Power System Block Diagram



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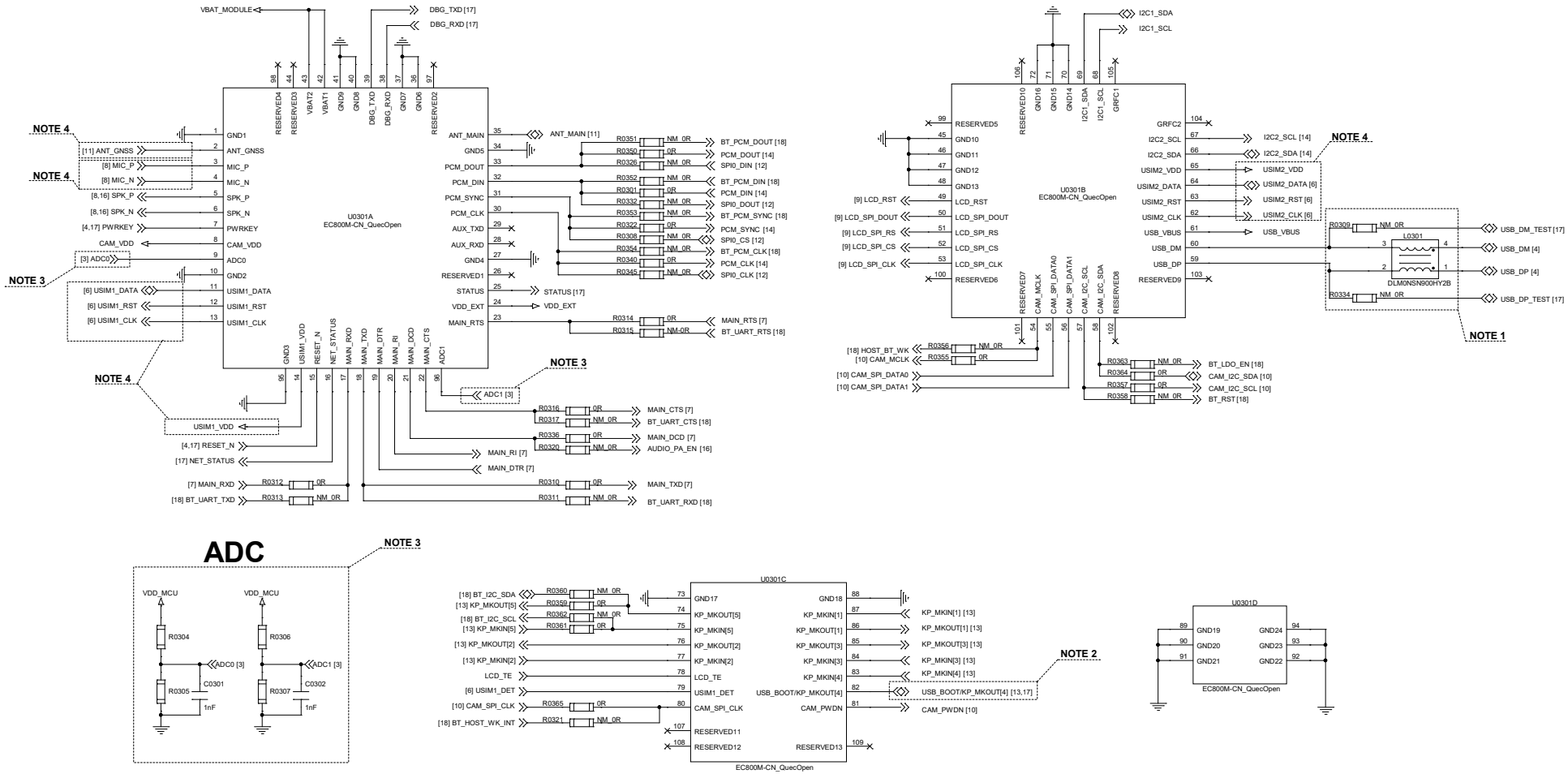
Module Interfaces



NOTE:

1. A common mode choke L0301 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, it is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the extra stubs of the trace. L0301 and two resistors R0309 and R0334 should be placed close to the module to ensure the integrity of USB signal.
2. USB_BOOT/KP_MKOUT[4] cannot be pulled down to low level before the module starts up successfully.
3. The voltage input range of ADC0 and ADC1 is 0–1.2 V. A voltage divider with resistance of more than 100 kΩ must be used for ADC interface application. The accuracy of the two resistors in each voltage divider affects the sampling error of the ADC. It is recommended to use resistors with an accuracy of 1%; if the accuracy of the ADC needs to be higher, resistors with an accuracy of 0.5% are recommended.
4. GNSS function of the module is optional:
   a) If the module with GNSS function is selected, the analog audio input channel requires an external microphone bias circuit. And MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO. Only USIM1 interface is supported on this condition.
   b) If the module without GNSS function is selected, the analog audio input channel requires no external microphone bias circuit; and dual USIM cards are supported in this situation.
5. All GND pins should be connected to the ground, and unused and RESERVED pins are kept floated.
6. Ensure there is a complete reference ground plane below the module, and the ground plane should be placed close to the module layer as possible.
   Other traces cannot be routed on the first layer below the module, at least four-layer board design is recommended.

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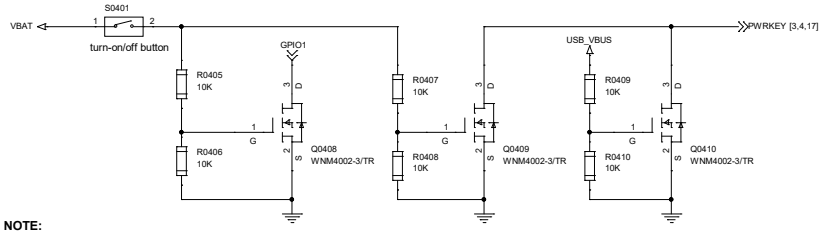
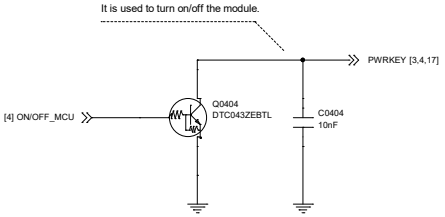
MCU Interfaces

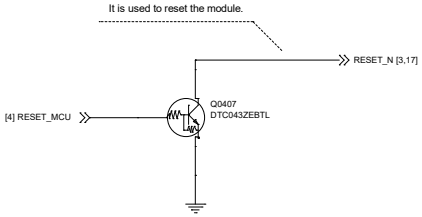
USB Insertion Enables Automatic Boot

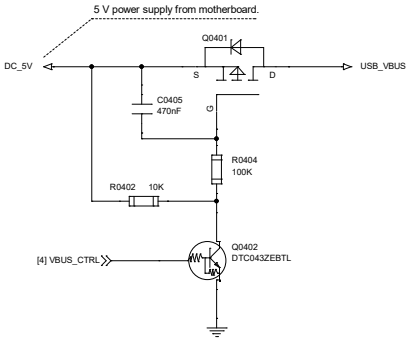


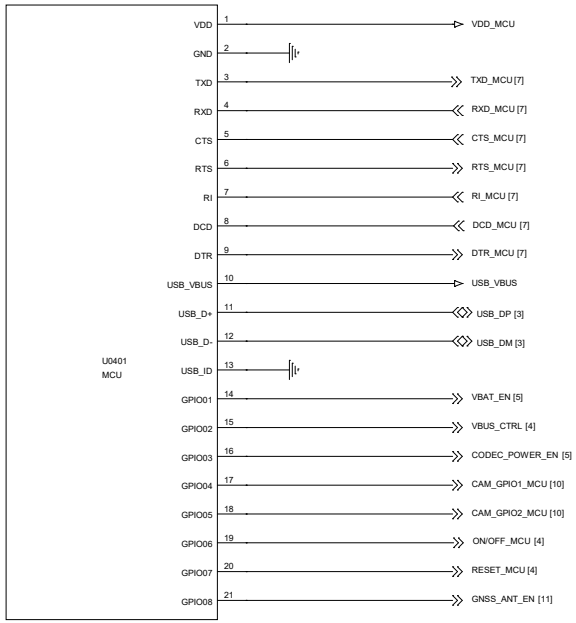
NOTE:

1. When USB is inserted, the module will boot automatically after the shutdown, and can not be shut down normally.
2. When USB is inserted, the level states of GPIO1 and PWRKEY pins are judged by the module to inform the system whether the module is booted by turn-on/off button or USB insertion. GPIO1 uses the GPIO resource with the default state of PU (pull-up).









NOTE:

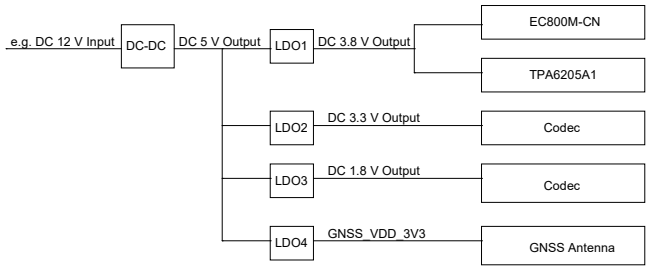
1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V. If the power domain of GPIO interfaces of U0401 is also 1.8 V, then the related level-shifting circuit is not needed.
2. The USB interface of the module can only serves as a slave device and supports full-speed and high-speed modes of USB 2.0. To communicate with the USB interface, MCU needs to support USB host mode or OTG function.
   The USB_VBUS pin of the module should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the GPIO pins which are at low level by default of MCU as the control pins for PWRKEY and RESET_N of the module. Please ensure that the load capacitance does not exceed 10 nF on PWRKEY and RESET_N pins.

Power Supply Design

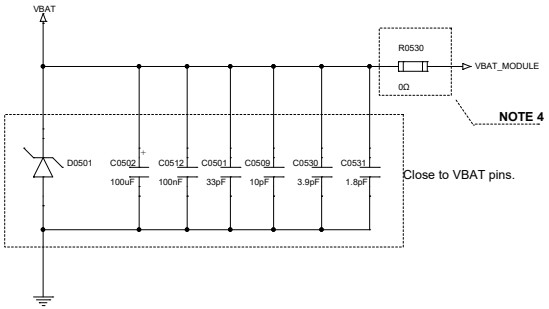
DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to a 5.0 V output, and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V to power the module, aduio PA, and Codec.

The supply current of the module must meet 2.0 A.



VBAT Design

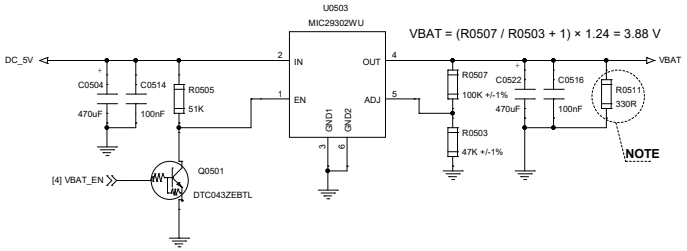


NOTE:

1. The power supply should be able to provide sufficient current up to 2.0 A for the module.
2. The width of VBAT trace should be not less than 2 mm.
3. The recommended operating voltage of VBAT ranges from 3.4 V to 4.3 V. The typical operating voltage of VBAT is 3.8 V.
4. It is recommended to reserve a 0 Ω resistor (the package should be 0603 at least) for future debugging. This resistor needs to be placed close to VBAT pins.

LDO Application

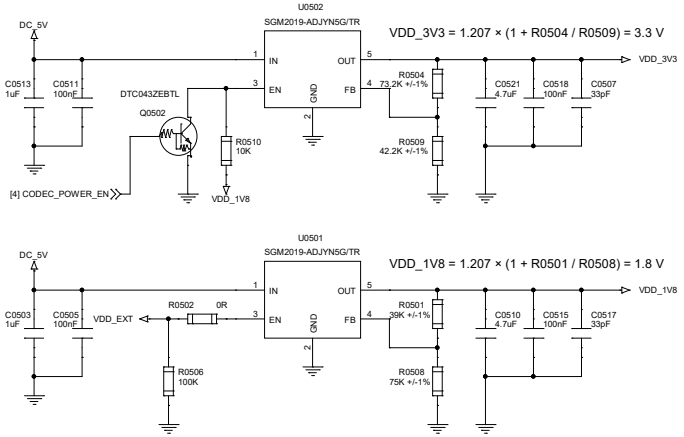
When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



NOTE:

The recommended load current should be larger than 10 mA.

Power Supply for Codec



NOTE:

1. VDD_EXT and CODEC_POWER_EN are used to turn on/off VDD_1V8 and VDD_3V3 respectively.
2. The following power-up/down sequences should be followed to ensure the audio codec works normally.

   Power-up sequence: power up VDD_1V8 first, and then VDD_3V3.

   Power-down sequence: power down VDD_3V3 first, and then VDD_1V8.

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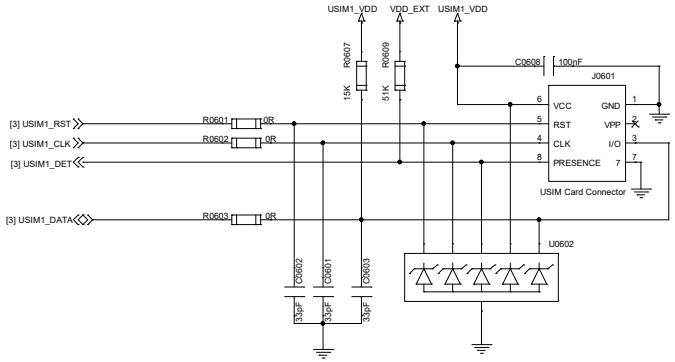
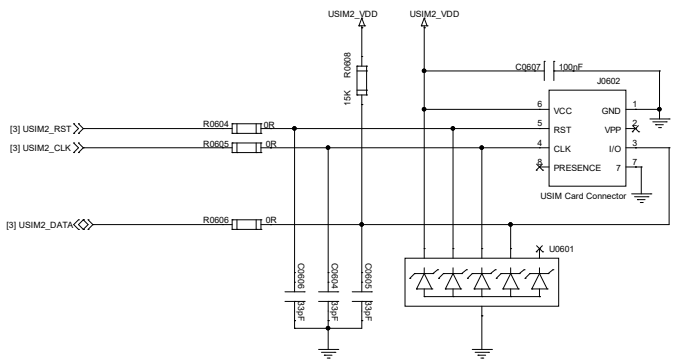
USIM Interface Design

USIM1



USIM2



NOTE:

1. U0601 and U0602 are recommended to be used to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.
2. The pull-up resistors R0607 and R0608 can improve anti-jamming capability, and should be placed close to the USIM card connector.
3. R0601–R0606 are used for debugging, and C0601–C0606 are used for filtering out RF interference.
4. The capacitance of C0607 and C0608 should be less than 1 μF and they should be placed close to the USIM card connector.
5. If the module with GNSS function is selected, only USIM1 interface is supported. If the module without GNSS function is selected, dual USIM cards are supported.

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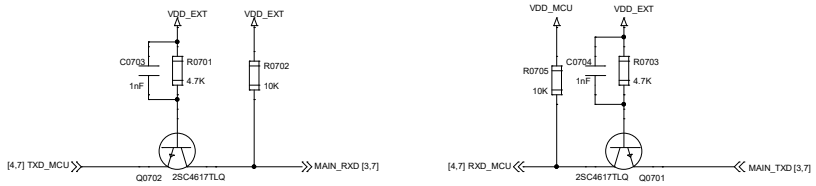
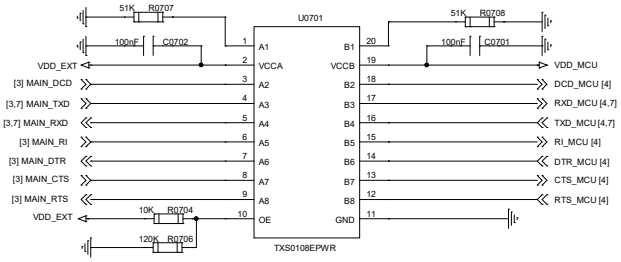
UART Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter one.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, please refer to the datasheet of TXS0108EPWR.
3. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C0703 and C0704 of 1 nF can improve the signal quality.
4. MAIN_RTS and MAIN_DTR level-shifting circuits are similar to that of the MAIN_RXD interface.
   MAIN_CTS, MAIN_RI and MAIN_DCD level-shifting circuits are similar to that of the MAIN_TXD interface.

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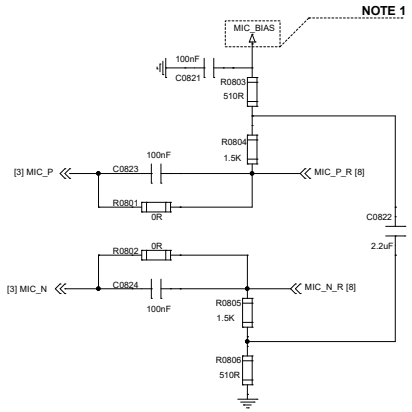
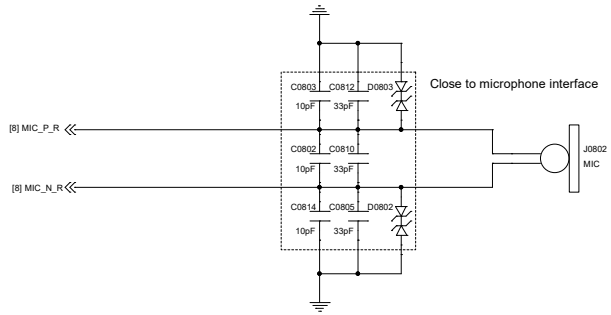
Analog Audio Design

Microphone Bias Circuit

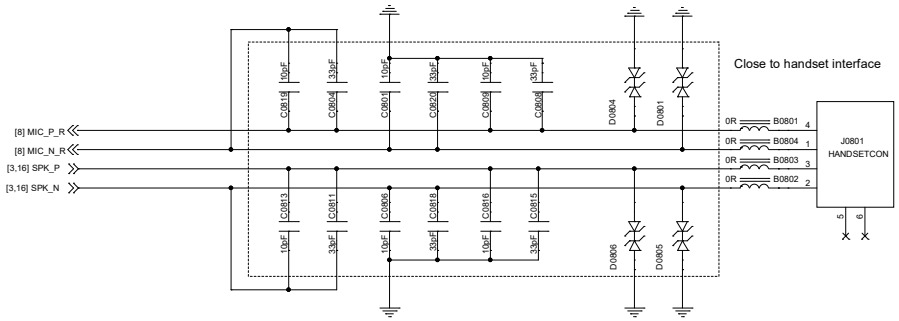


Case	C0821/C0822/C0823/C0824 R0803/R0804/R0805/R0806	R0801/R0802
External microphone bias circuit	M	NM
Without external microphone bias circuit	NM	M

Microphone Application



Handset Application



NOTE:

1. If the module with GNSS function is selected, the analog audio input channel requires an external microphone bias circuit, and MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO. If the module without GNSS function is selected, the analog audio input channel requires no external microphone bias circuit.
2. Both the MIC and SPK signal traces need to be routed as differential pairs.
3. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noises.
4. In the audio design, you can choose either the analog audio or the codec. It is not necessary to select both.
5. It is recommended to use 10 pF and 33 pF capacitors to filter RF interference.

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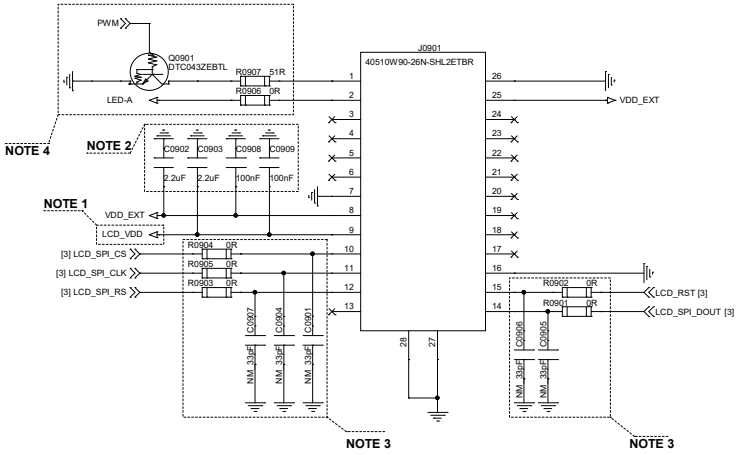
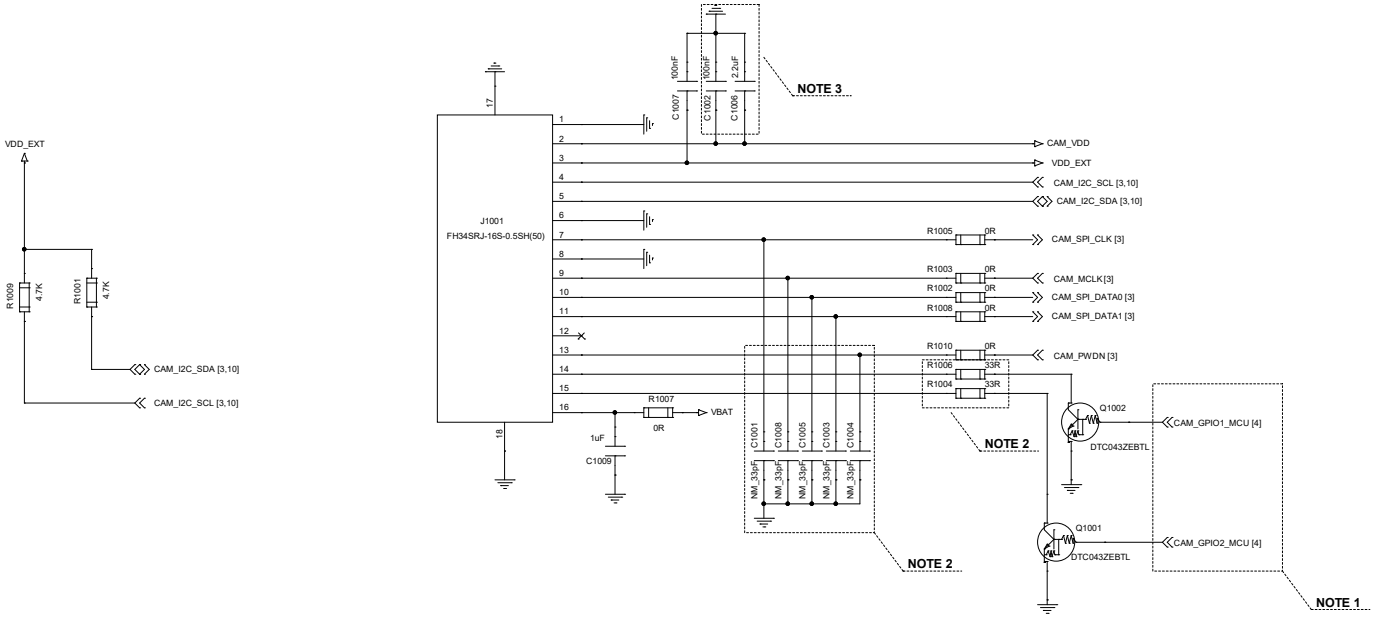
LCM Interface Design



NOTE:

1. It is recommended to design LCM power supply by yourself.
2. To avoid abnormal LCD display caused by power fluctuation, it is recommended to mount filter capacitors.
3. The 33 pF capacitors of the signal pins should be reserved, and be used according to the actual debugging situation.
4. The LED-A backlight power supply is designed by youself, and you can select the appropriate resistor (R0907) according to the digital transistor rated current and LED-A voltage value.

Camera Interface Design



NOTE:

1. By controlling the triode switching circuit, CAM_GPIO1_MCU controls the cathode of the positioning light of the camera, and CAM_GPIO2_MCU controls the cathode of the supplement light of the camera.

   It is recommended to select GPIO pins which are in pull-down status by default as the two control pins.

2. The 33 pF capacitors of the signal pins should be reserved, and be used according to the actual debugging situation.

   The values of current limiting resistors of positioning light and supplement light (R1004 and R1006) should be varied according to the required brightness.

3. The capacitors (C1002 and C1006) of the CAM_VDD power supply should be connected to the GND layer directly, otherwise, power supply noise may lead to abnormalities such as white dots on the preview screen.

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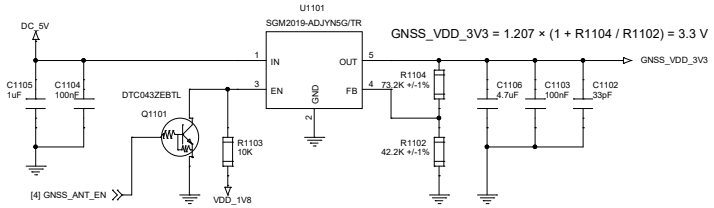
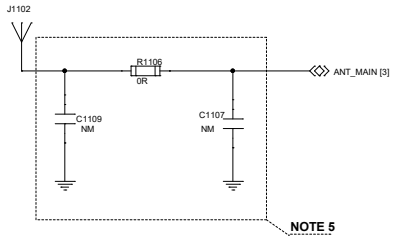
Antenna Interface Design

GNSS Active Antenna Power Supply



Main Antenna Design

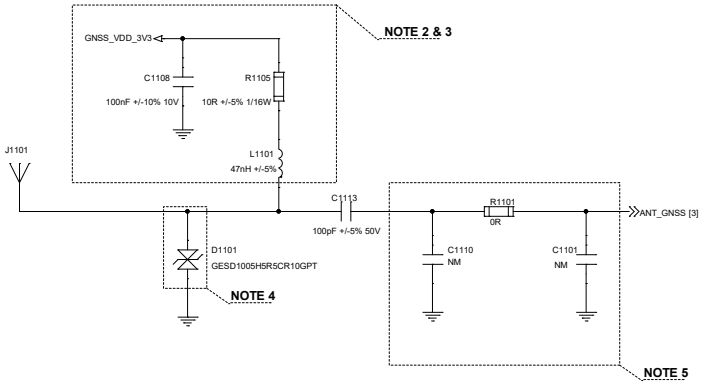


NOTE:

1. GNSS function is optional. Thus, the GNSS antenna design of this page is only applicable to the module with GNSS function.
2. The active antenna uses an LDO for power supply, and VDD circuit is not needed when using passive antenna.
3. L1101, R1105 and C1108 are recommended to be placed close to the RF traces during layout.
4. The junction capacitance of the ESD protection component on the antenna interface is recommended to be less than 0.05 pF.
5. Reserve a Π-type matching circuit at antenna interface.
6. The single-ended impedance of the RF antenna is 50 Ω, and the length should be as short as possible.
7. The voltage range of the external active antenna power supply is from 2.8 V to 4.3 V, and the typical value is 3.3 V.

   The power supply voltage can be designed according to the power supply requirements of the selected active antenna.

GNSS Antenna Design



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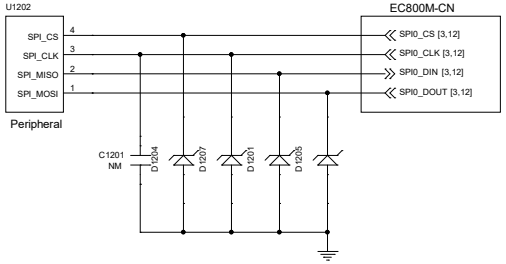
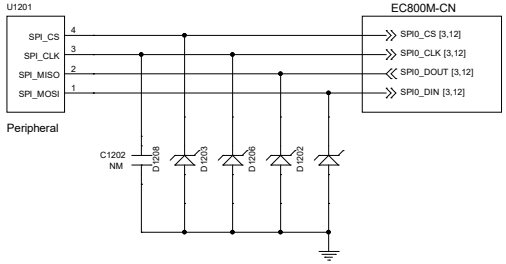
SPI Interface Design

Module As Master



Module As Slave



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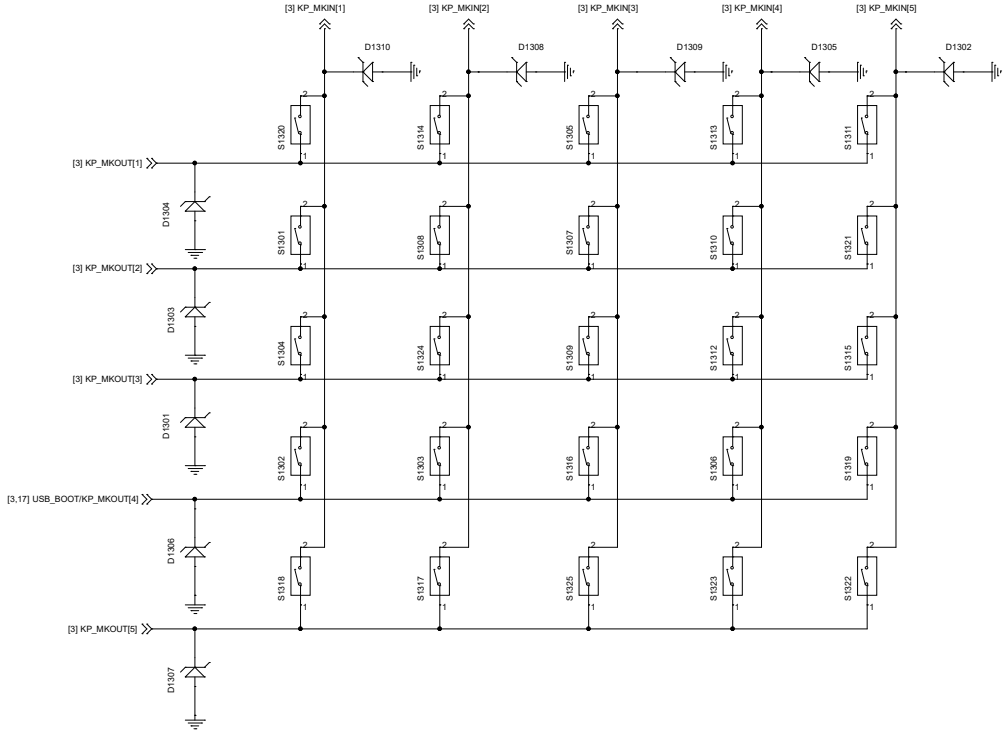
Matrix Keypad Design



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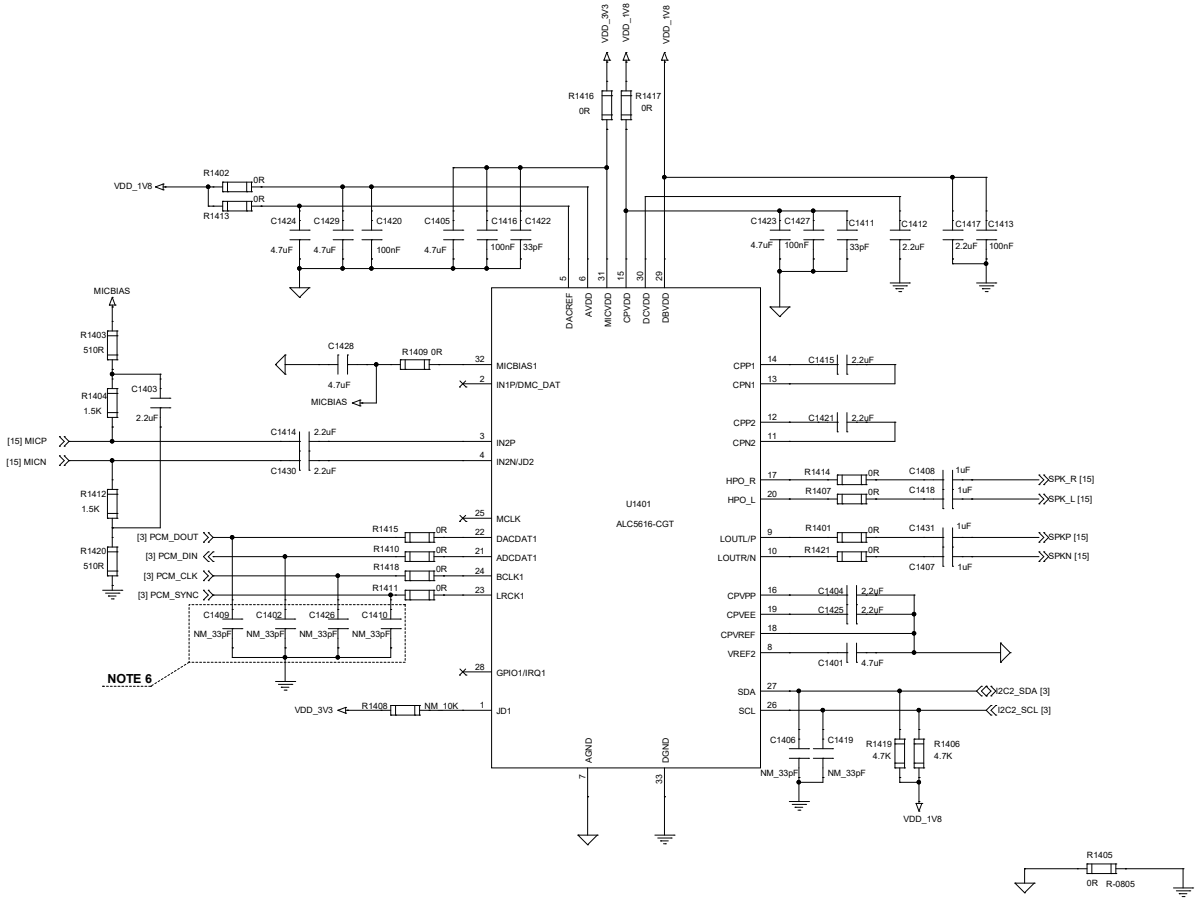
Audio Codec Design (ALC5616)



NOTE:

1. ALC5616 power-up sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD → MICVDD → software initialization.
2. ALC5616 power-down sequence: disable Codec function by software → MICVDD → DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.
3. The module will automatically initialize the Codec via I2C interface after it is turned on successfully, so all power supplies for the Codec need to be powered up before that.
4. Please pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805. For more details, please refer to sheet "Audio Codec Interface Design".
5. For more details, please refer to the datasheet of ALC5616.
6. The 33 pF capacitors of the signal pins should be reserved, and be used according to the actual debugging situation.

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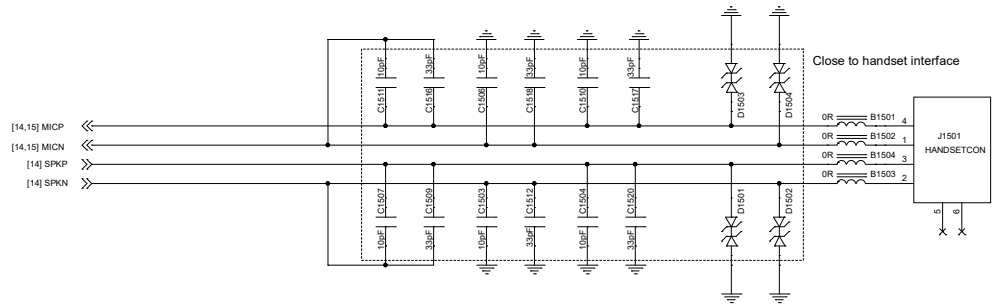
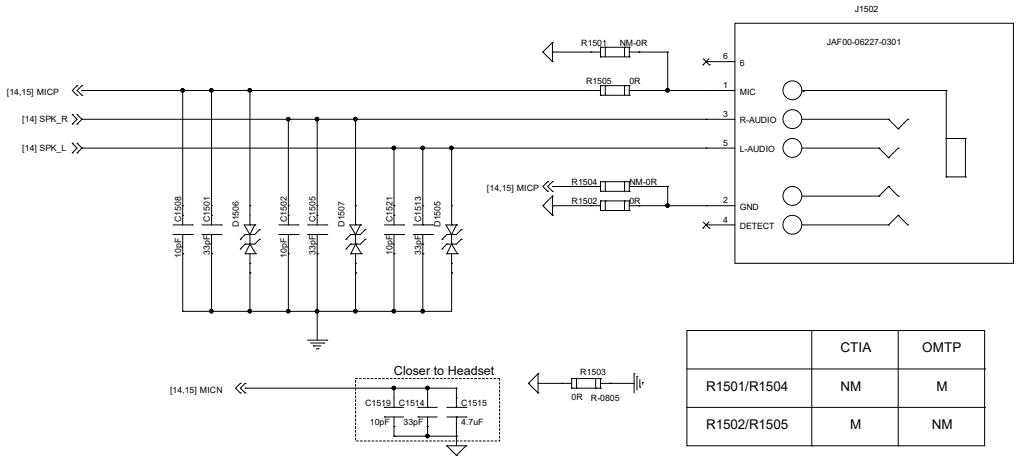
Audio Codec Interface Design

Handset Application



Headset Application



	CTIA	OMTP
R1501/R1504	NM	M
R1502/R1505	M	NM

NOTE:

1. The Codec analog output can drive handset and headset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.
2. In handset application, route the MIC and SPK signal traces as differential pairs respectively.
3. In headset application, route the MIC signal traces as a differential pair.
4. All MIC and SPK signal traces shall be surrounded with ground on the layer and ground planes above and below, and far away from noises such as clock and DC-DC signals.
5. Please pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805 (short-circuit through single point grounding).

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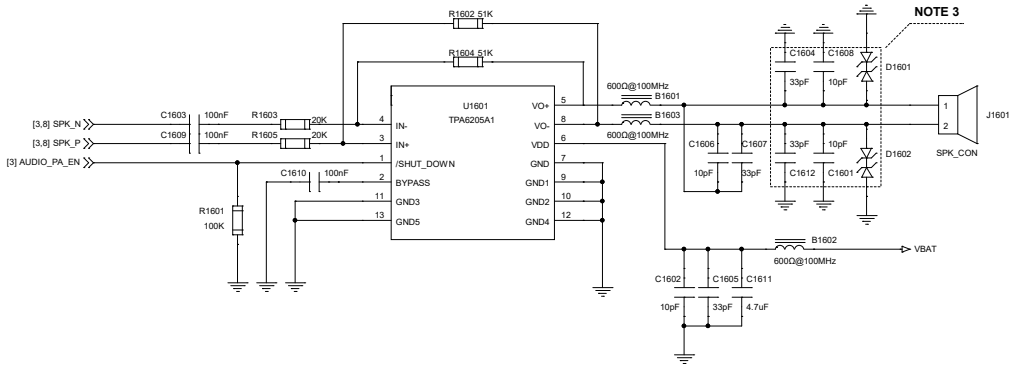
Analog Audio Design (Audio Power Amplifier)



NOTE:

1. SPK_P and SPK_N are differential output channels that can be used for an external audio power amplifier.
   It is recommended to use MAIN_DCD of the module to control the enable pin of the audio power amplifier to eliminate POP. For more information about AUDIO_PA_EN, please contact Quectel technical support.
2. The power amplifier in this design is for reference only. Select the appropriate audio power amplifier according to actual needs.
3. Filter capacitors and ESD protection components should be placed close to the loudspeaker.
4. The selection of ESD protection components is related to the selection of audio power amplifier. Please ensure that the output voltage of audio power amplifier is within the maximum reverse working voltage range of ESD protection components under normal working condition, so as to avoid damage to ESD protection components .

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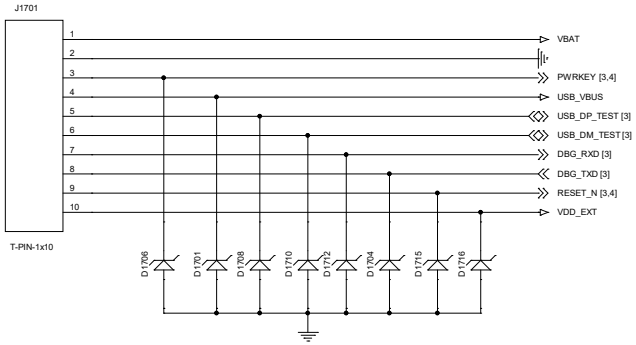
Other Designs

Indicators

NOTE:

1. For more details about STATUS and NET_STATUS, please refer to the hardware design document of the module.
2. If the low current consumption is required when your device is in sleep mode, replace the power supply VBAT of the STATUS and NET_STATUS indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

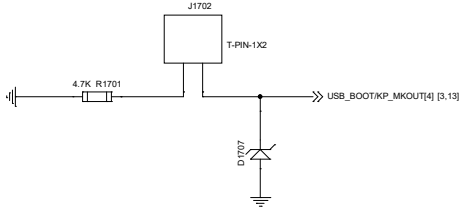
Reserved Test Points



NOTE:

1. Test points for both USB and debug UART interfaces are reserved for catching logs.
2. Test points for USB interface can also be reserved for firmware upgrade.
3. The junction capacitance of the ESD protection componets on USB data lines should be less than 2 pF.
4. The debug UART interface supports 1.8 V power domain, and a voltage-level translator should be used if the power domain of your application is 3.3 V.

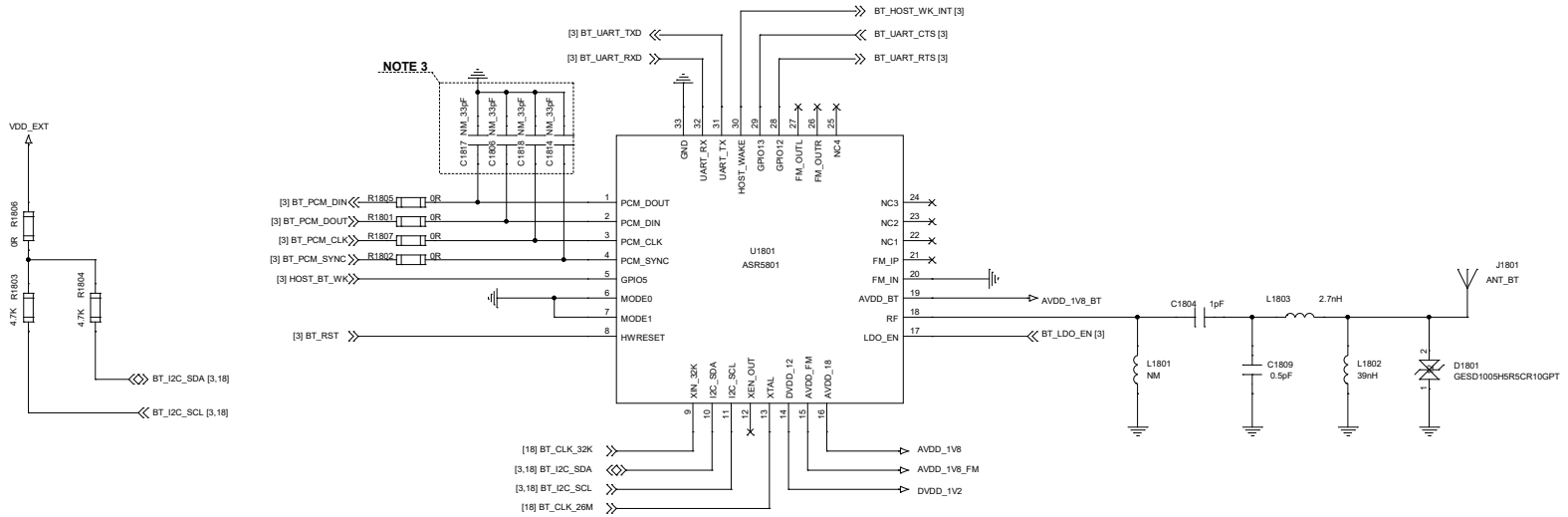
USB_BOOT Interface

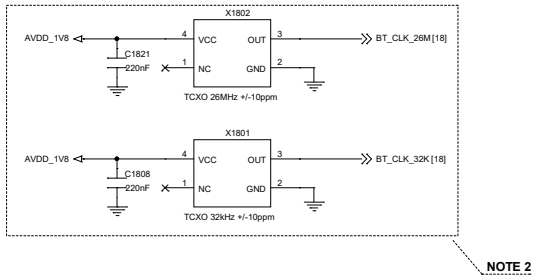


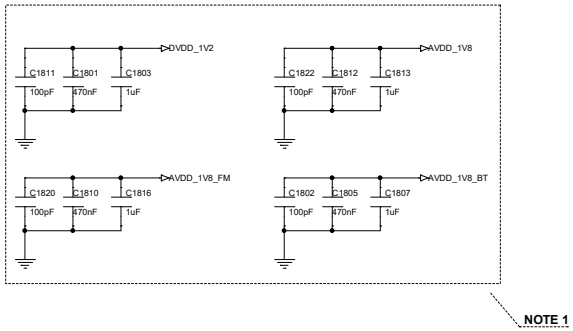
NOTE:

1. Ensure to reserve the USB_BOOT interface design and test points.
2. Before module is turned on, pull USB_BOOT/KP_MKOUT[4] down to GND, and the module will enter emergency download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.
3. The 6.0.1 and above version of Qflash tool must be used for firmware upgrading.

Bluetooth Interface Design







NOTE:

1. 1.8 V power supply of the bluetooth chip (AVDD_1V8) shall be designed by yourself, which is used to provide 1.8 V power supply for the chip.
   And the other three (DVDD_1V2, AVDD_1V8_FM and AVDD_1V8_BT) are the internal power supply pins of the chip,
   which are used to connect external filter capacitors.
2. It is recommended to choose 26 MHz and 32 KHz oscillators and to design power supply circuits on your own.
3. The 33 pF capacitors of the signal pins should be reserved, and be used according to the actual debugging situation.

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