EC600M Series QuecOpen Reference Design

LTE Standard Module Series

Version: 1.3

Date: 2024-06-03

Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2022-04-27	Andy ZHAO	Creation of the document
1.0	2022-08-31	Andy ZHAO	First official release
1.1	2022-09-14	Andy ZHAO	Updated related information of ADC interface: Added ADC voltage divider and related notes (Sheet 3); Updated ADC voltage domain from 1.8 V to 1.2 V (Sheet 1 and 3).
1.2	2023-02-24	Howell KANG	1. Updated the UART Level-shifting Circuit in IC Solution (Sheet 7). 2. Added a note about the capacitors of the signal pins (Sheet 13).
1.3	2024-06-03	Howell KANG/ Stefan FAN	1. Added the applicable module EC600M-EU and related information. 2. Added Wi-Fi & Bluetooth interface design (Sheets 1, 2, 3, 4, 5, 12 and 19). 3. Updated the resistance of resistors that connected to power supply on ADC interfaces' voltage divider circuit from 100 kΩ to 100 kΩ–1 MΩ; Added a note on pins 130–135 (Sheet 3). 4. Added USB insertion enabling automatic boot circuit (Sheet 4). 5. Added a note on UART hardware flow control design (Sheet 7). 6. Added ESD protection component and related note in antenna interface design (Sheet 11).

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EC600M series (EC600M-CN and EC600M-EU) module in QuecOpen® solution, including block diagram, power system block diagram, module interfaces, power supply design, USIM interface, UART, analog audio interface and other designs.

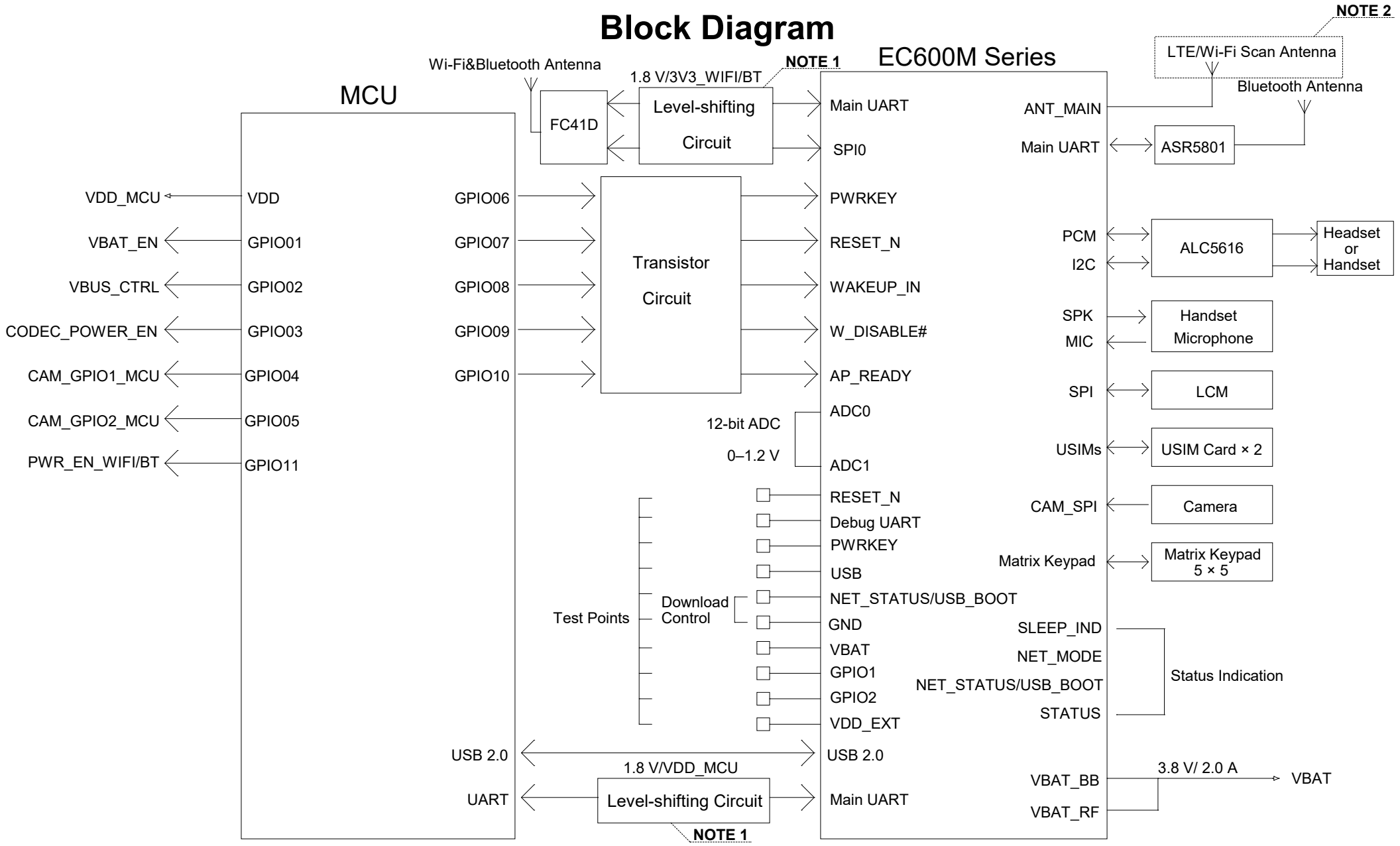
1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

NOTE

It is required to confirm the applicability and price from the supplier about the IC involved in the reference design.

Block Diagram



NOTE:

1. A transistor solution or an IC solution TXS0108EPWR provided by Texas Instruments is recommended.
2. The module supports Wi-Fi Scan function. Wi-Fi Scan that only supports receiving shares the same antenna interface with main antenna, thus the two functions cannot be used at the same time.

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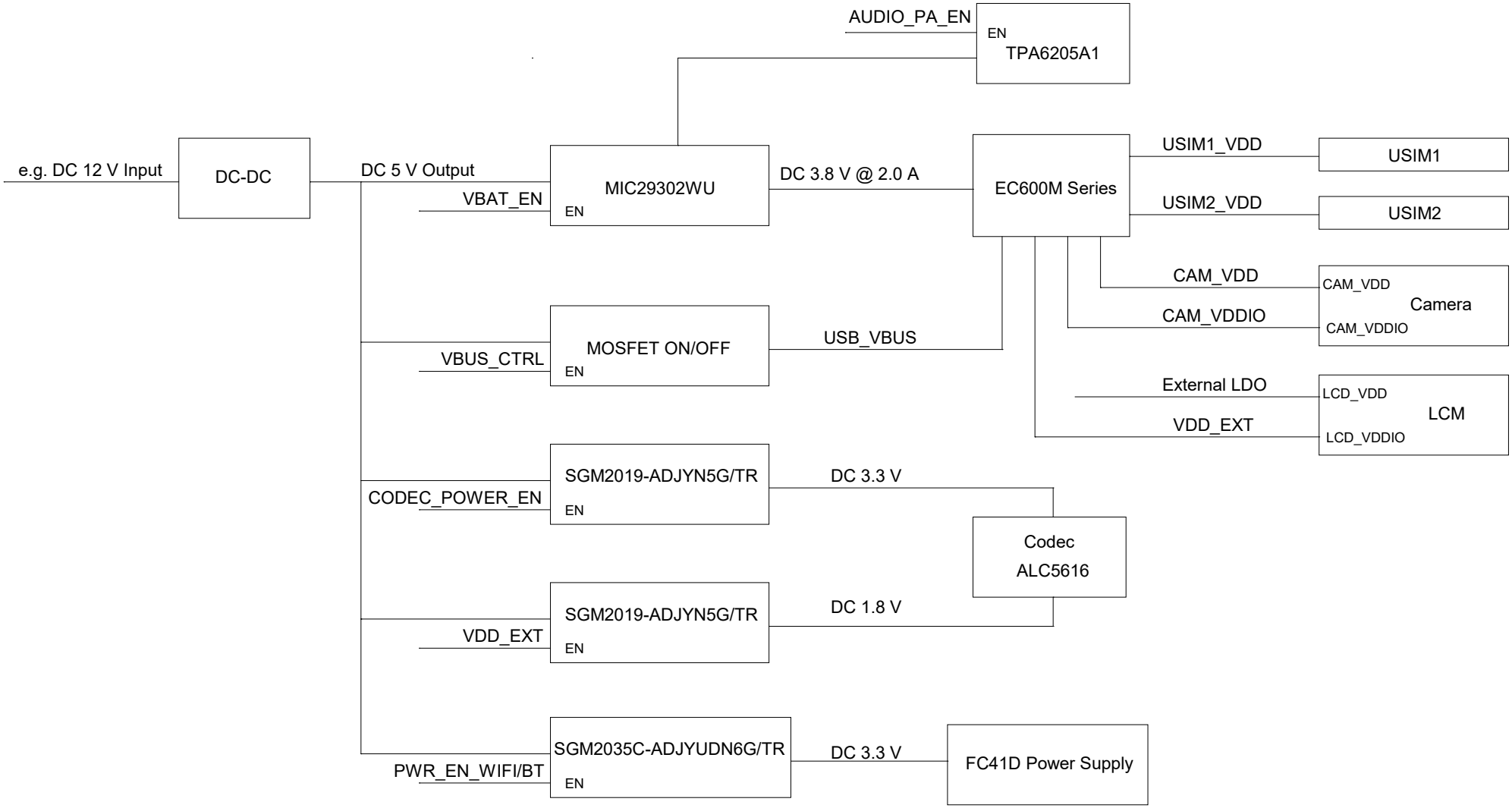
Power System Block Diagram



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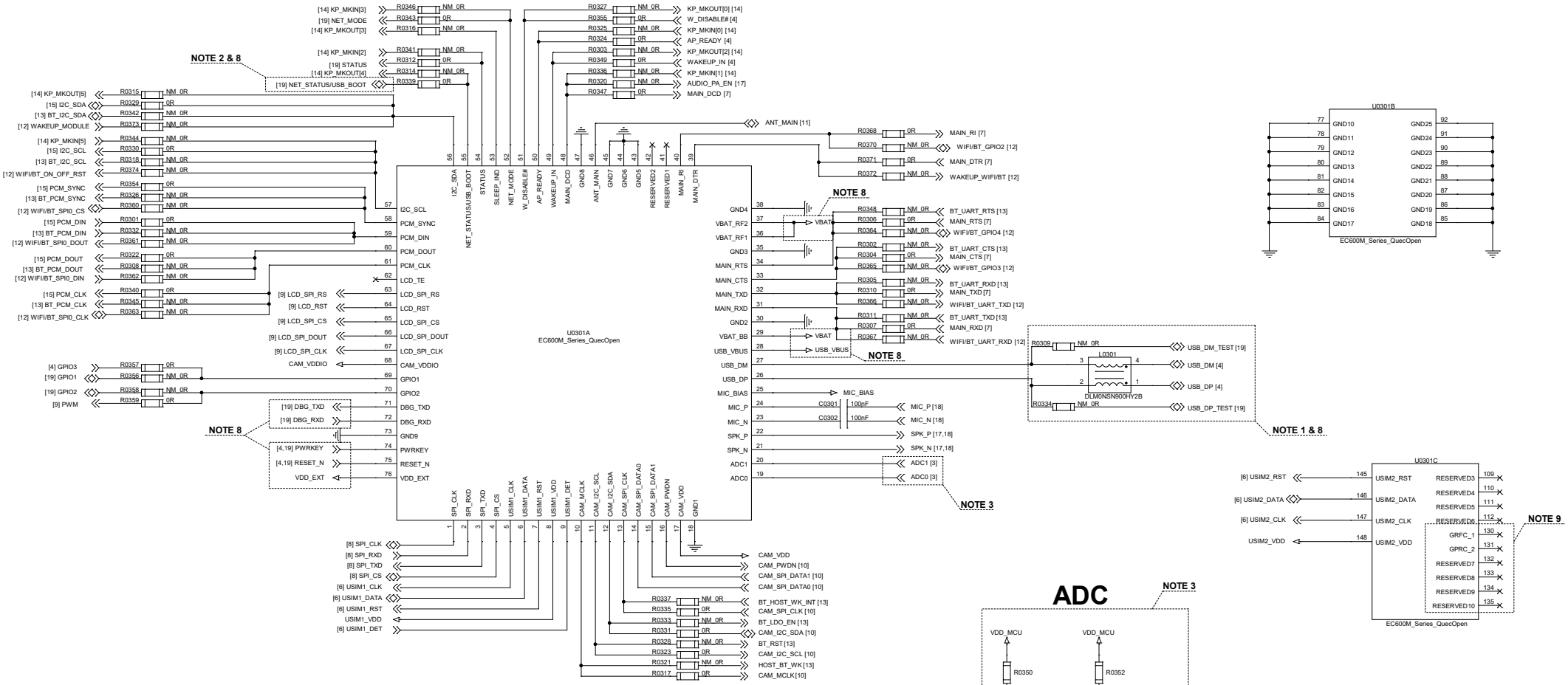
Module Interfaces



NOTE:

1. It is recommended to add a common mode choke L0301 in series between the module and your MCU to suppress EMI.
   Additionally, test points must be reserved over USB_DP and USB_DM for firmware upgrades, and it is recommended to minimize extra trace stubs.
   Place L0301 and two resistors, R0301 and R0302, close to the module to ensure USB signal integrity.
2. NET_STATUS/USB_BOOT cannot be pulled down to low level before the module starts up successfully.
3. The input voltage range of ADC0 and ADC1 is 0–1.2 V. A voltage divider circuit with two resistors must be used for ADC0 and ADC1 voltage inputs respectively, and the required resistance of the two resistors (R0350 and R0352) that connected to VDD_MCU is between 100 kΩ and 1 MΩ. The accuracy of the two resistors in each voltage divider affects the sampling error of the ADC. It is recommended to use resistors with an accuracy of 1 %. For higher ADC accuracy, resistors with accuracy of 0.5 % are recommended.
4. Connect all GND pins to ground, and keep unused and RESERVED pins open.
5. For more details about GPIO multiplexing function, see the GPIO configuration document of the module.
6. Ensure an uninterrupted reference ground plane below the module, with minimal distance between the ground plane and the module layer. At least four-layer board design is recommended.
7. The 6.0 and above version of QFlash tool must be used for firmware upgrading.
8. Test points must be reserved for DBG_TXD/RXD, USB_DP/DM and USB_VBUS. It is recommended to reserve test points for VDD_EXT, NET_STATUS/USB_BOOT, PWRKEY and VBAT.
   If RESET_N is unused, it is recommended to reserve a test point.
9. EC600M-CN does not have pins 130–135.

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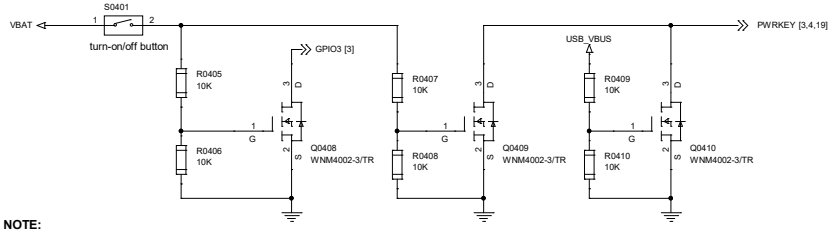
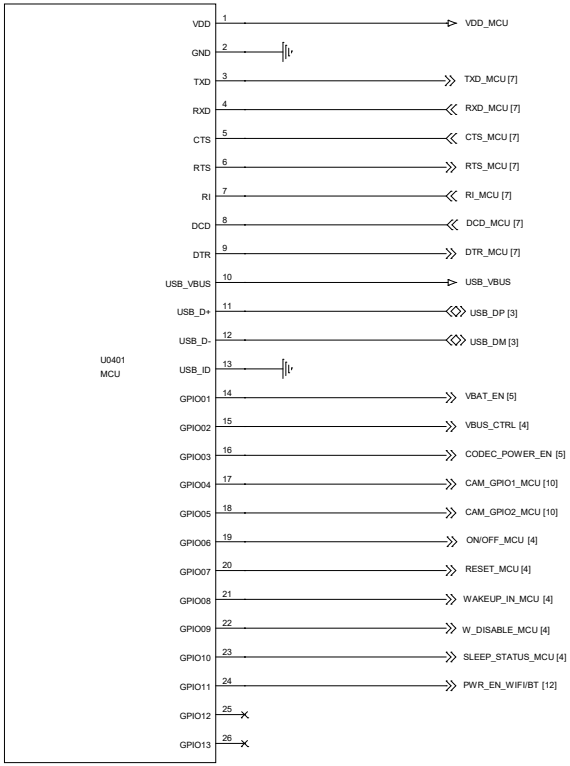
MCU Interfaces

USB Insertion Enables Automatic Boot

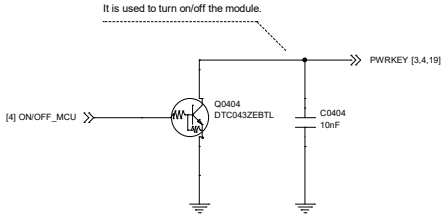


NOTE:

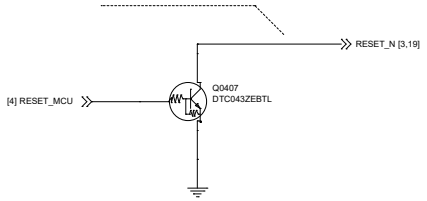
1. When USB is inserted, the module cannot be shut down normally, and will boot automatically after the shut down.
2. When USB is inserted, the level states of GPIO3 and PWRKEY pins are used to determine whether the module is turned on by the turn-on/off button or USB insertion. GPIO3 utilizes the GPIO resource with a default pull-up (PU) state.



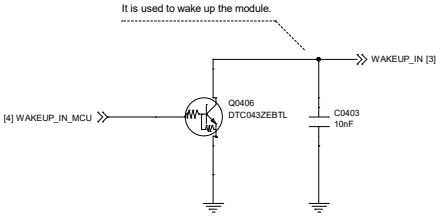
It is used to turn on/off the module.



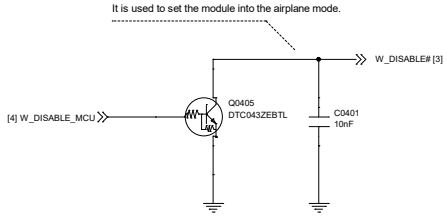
It is used to reset the module.

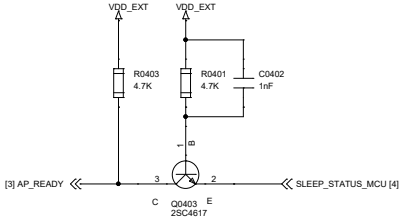


It is used to wake up the module.

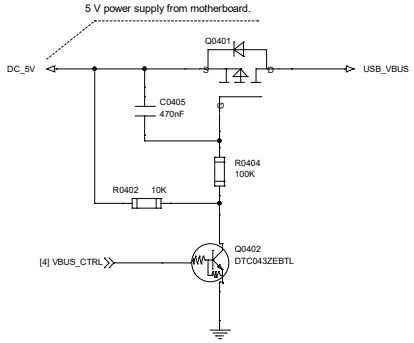


It is used to set the module into the airplane mode.





5 V power supply from motherboard.



NOTE:

1. If the power domain of your MCU (U0401) is also 1.8 V, the level-shifting circuit is not necessary as it matches the 1.8 V power domain of the module's GPIO interfaces.
2. The USB interface of the module can only serve as a slave device and supports full-speed and high-speed modes of USB 2.0. To communicate with the USB interface, MCU needs to support USB host mode or OTG function.
   For USB detection, the USB_VBUS pin of the module should be powered by an external power system. Use VBUS_CTRL to control the on/off state of the USB_VBUS power supply.
3. It is recommended to choose MCU GPIO pins with a default low level to control the module's PWRKEY and RESET_N pins. Ensure that the load capacitance on these pins does not exceed 10 nF.

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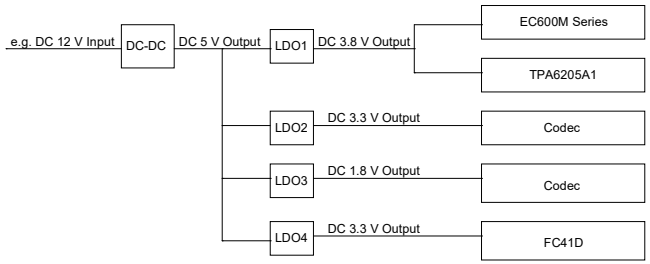
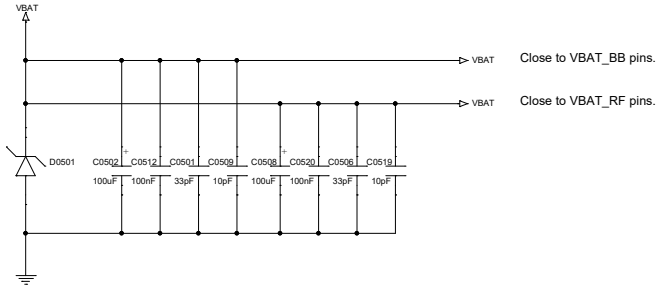
Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to 5.0 V, and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V to power the module, audio PA Codec and FC41D.



VBAT Design

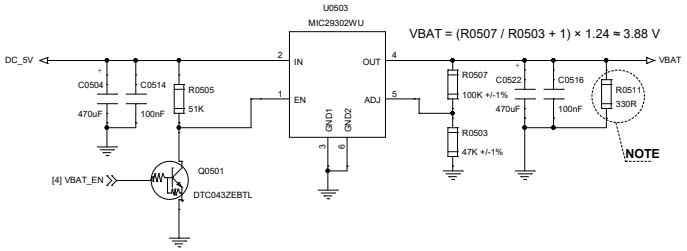


NOTE:

1. The power supply for the module should be capable of supplying a minimum current of 2.0 A.
2. The VBAT trace should be connected to VBAT_BB and VBAT_RF pins in a star configuration.
3. The width of VBAT_BB trace should be at least 1 mm; and the width of VBAT_RF trace should be at least 2 mm.
4. The recommended operating voltage range for VBAT is 3.4 V to 4.3 V, with a typical value of 3.8 V.

LDO Application

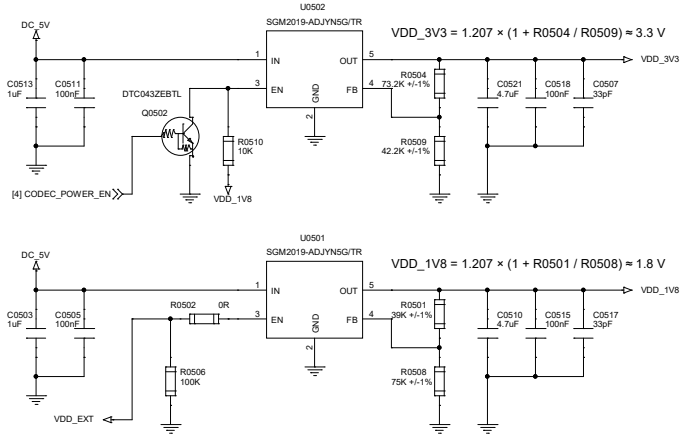
When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.



NOTE:

The recommended load current should exceed 10 mA.

Power Supply for Codec



NOTE:

1. VDD_EXT and CODEC_POWER_EN are used to turn on/off VDD_1V8 and VDD_3V3 respectively.
2. To ensure proper functioning of the audio codec, adhere to the following power-up/down sequences:

   Power-up sequence: power on VDD_1V8 first, followed by VDD_3V3.

   Power-down sequence: power off VDD_3V3 first, followed by VDD_1V8.

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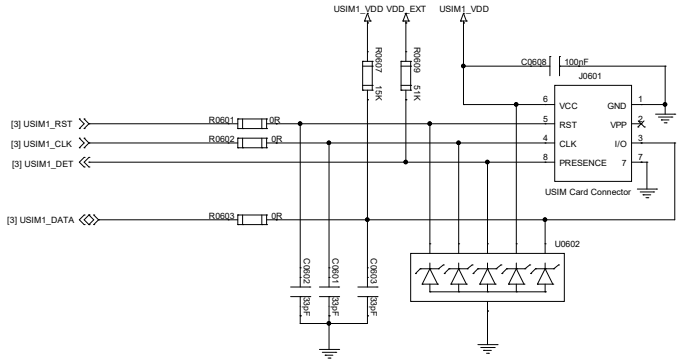
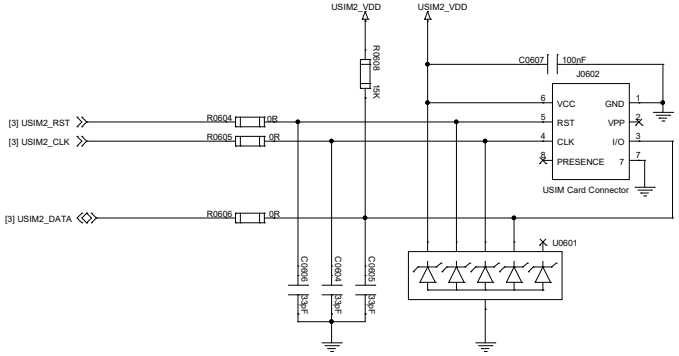
USIM Interface Design

USIM1



USIM2



NOTE:

1. U0601 and U0602 are recommended to be used to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.
2. The pull-up resistors R0607 and R0608 can improve anti-jamming capability, and should be placed close to the USIM card connector.
3. R0601–R0606 are used for debugging, and C0601–C0606 are used for filtering out RF interference.
4. The capacitance of C0607 and C0608 should be less than 1 μF and they should be placed close to the USIM card connector.

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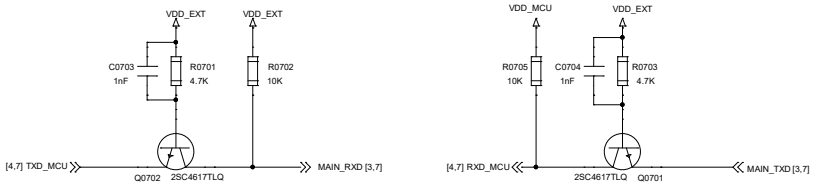
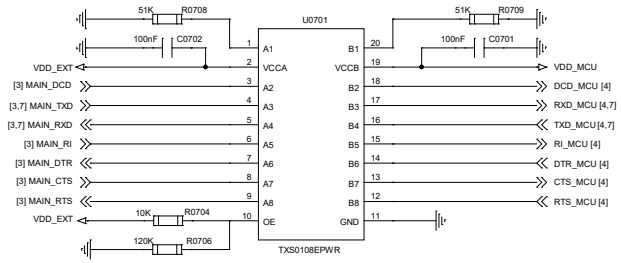
UART Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution

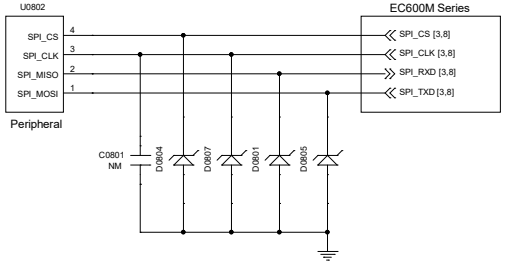


NOTE:

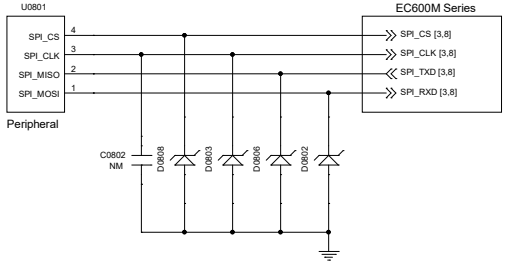
1. There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter one.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, see the datasheet of TXS0108EPWR.
3. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C0703 and C0704 of 1 nF can improve the signal quality.
4. MAIN_RTS and MAIN_DTR level-shifting circuits are similar to that of the MAIN_RXD.
   MAIN_CTS, MAIN_RI and MAIN_DCD level-shifting circuits are similar to that of the MAIN_TXD.
5. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

SPI Design

Module As Master



Module As Slave



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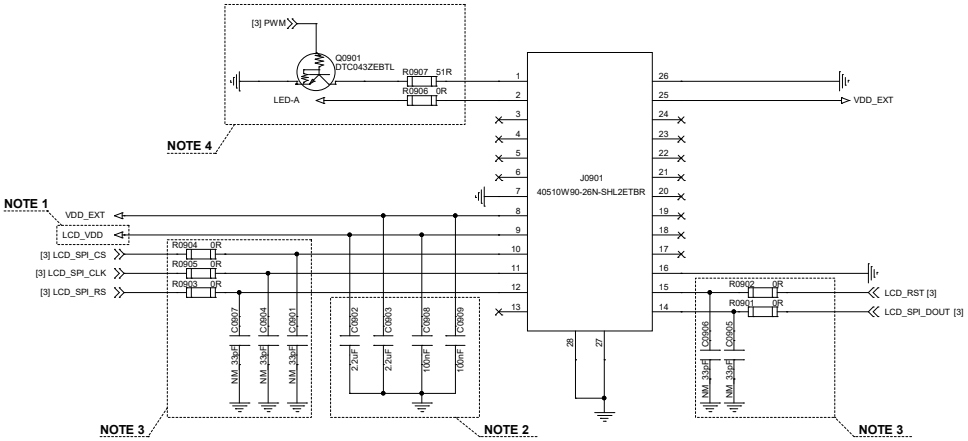
LCM Interface Design



NOTE:

1. It is recommended to design LCM power supply by yourself.
2. To avoid abnormal LCM display caused by power fluctuation, it is recommended to mount filter capacitors.
3. The 33 pF capacitors of the signal pins should be reserved, and be used according to the actual debugging situation.
4. The LED-A backlight power supply is designed by youself, and you can select the approriate resistor (R0907) according to the digital transistor rated current and LED-A voltage value.

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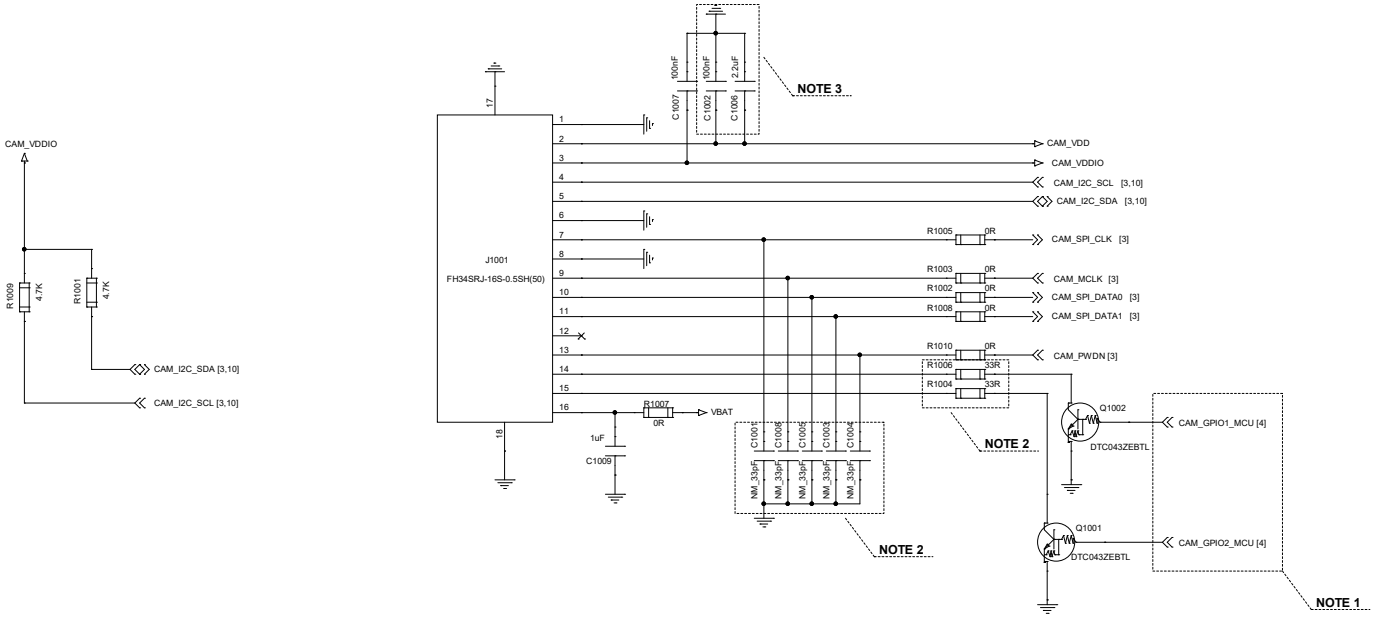
Camera Interface Design



NOTE:

1. By controlling the triode switching circuit, CAM_GPIO1_MCU controls the cathode of the positioning light of the camera, and CAM_GPIO2_MCU controls the cathode of the supplement light of the camera.

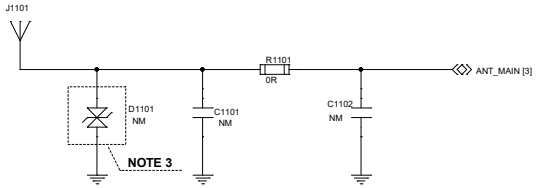
   It is recommended to select GPIO pins which are in pull-down status by default as the two control pins.

2. The 33 pF capacitors of the signal pins should be reserved, and be used according to the actual debugging situation.

   The values of current limiting resistors (R1004 and R1006) of positioning light and supplement light should be varied according to the required brightness.

3. The capacitors (C1002 and C1006) of the CAM_VDD power supply should be connected to the GND layer directly. Otherwise, power supply noise may lead to abnormalities such as white dots on the preview screen.

Antenna Interface Design



NOTE:

1. It is highly recommended to reserve a Π-type matching circuit at antenna interface for future debugging.
2. The single-ended impedance of the RF antenna is 50 Ω.
3. It is recommended to reserve an ESD protection component for the antenna interface and the junction capacitance should not exceed 0.05 pF.

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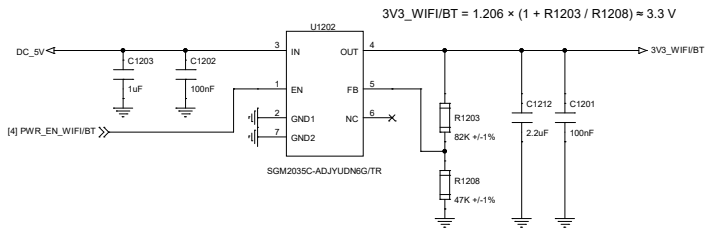
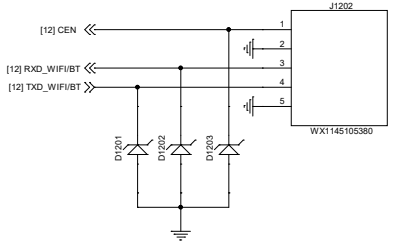
Wi-Fi&Bluetooth Interface Design

Power Supply for FC41D



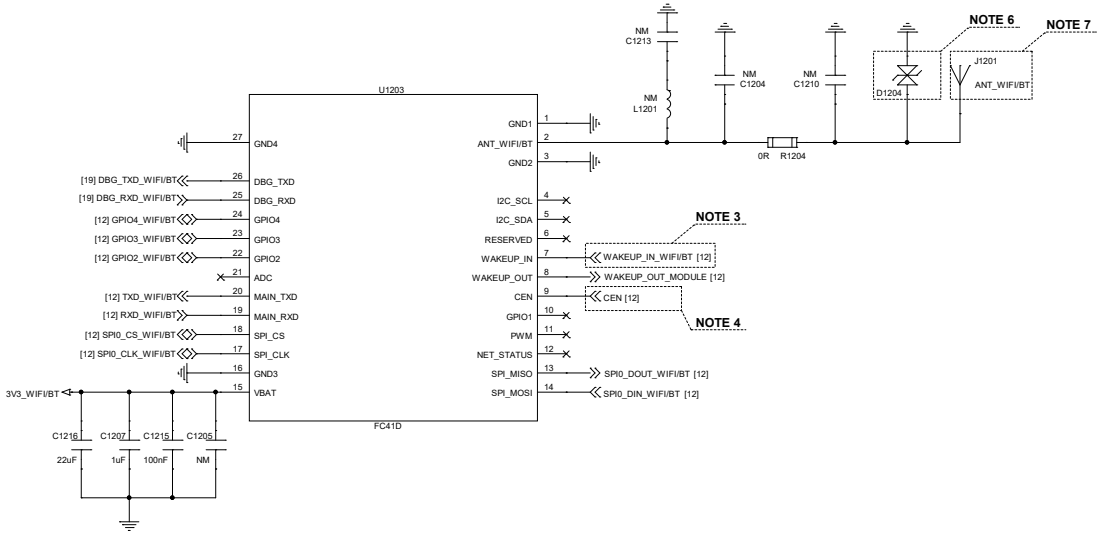
Download Interface For FC41D

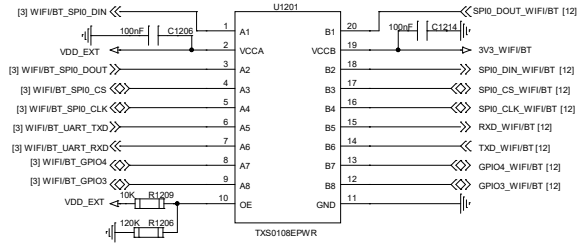


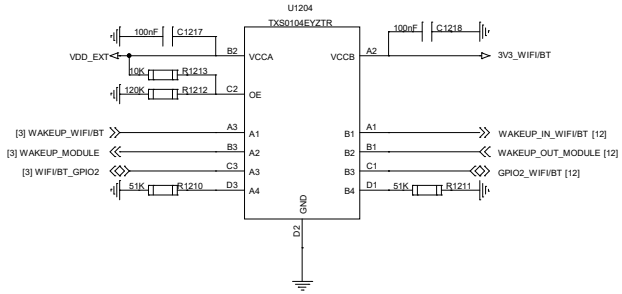
NOTE:

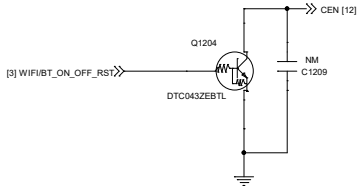
Firmware upgrade steps:

1. Click the "burn" button of the software download tool.
2. Connect the CEN to GND at STA mode for two seconds.
3. Release CEN.









NOTE:

1. 3V3_WIFI/BT trace is recommended to be wider than 0.3 mm. In principle, the longer the 3V3_WIFI/BT trace is, the wider it should be.
2. The main UART or SPI can be selected to transmit Wi-Fi and bluetooth data from the module to FC41D according to your actual design, but based on the software version, main UART will be selected by default.
3. You can use the rising edge of WAKEUP_IN (pin 7) to wake up the FC41D.
4. Pull down CEN pin and then cut off 3V3_WIFI/BT to turn off the module to save power.
5. When using the PCB antenna, the module should be placed at the side of the motherboard and kept away from metal components, and the clearance of PCB antenna should be kept as large as possible.
6. It is recommended to reserve an ESD protection component for the antenna interface and the junction capacitance should not exceed 0.05 pF.
7. The single-ended impedance of the RF antenna is 50 Ω, and length should be minimized.

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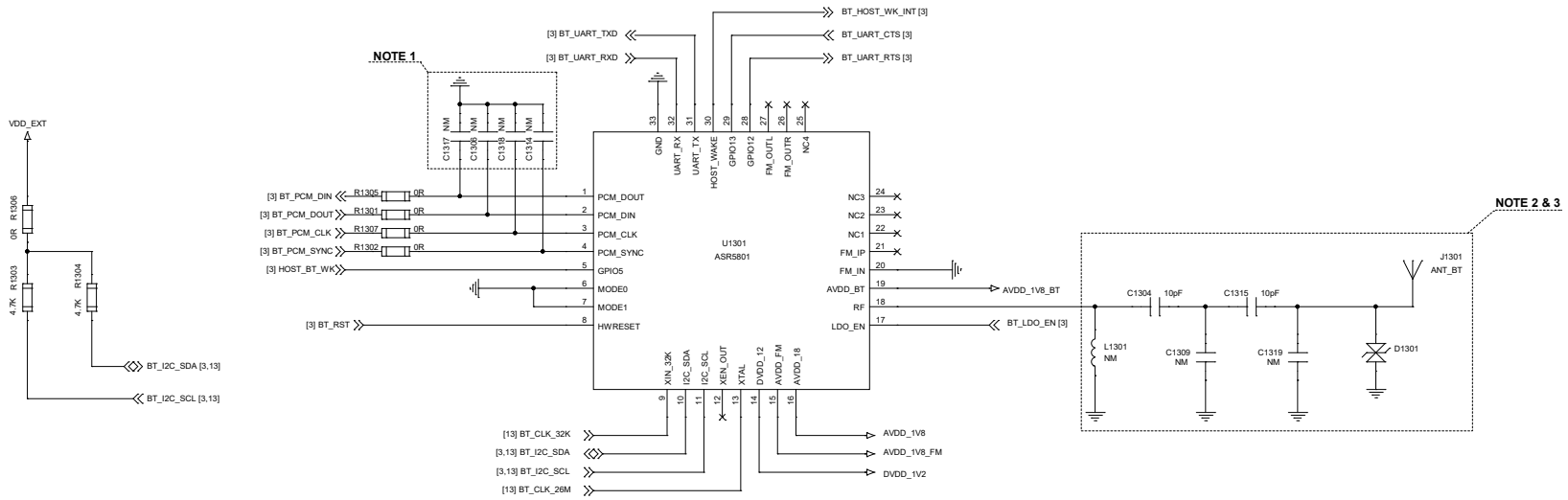
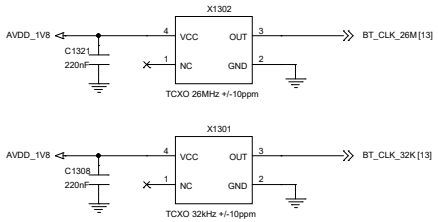
Bluetooth Interface Design



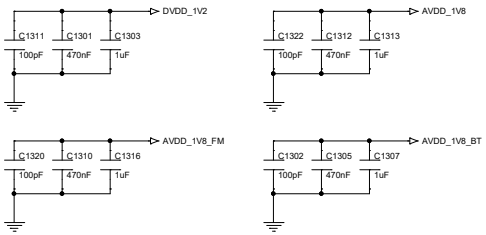
NOTE:

1. Reserve 33 pF capacitors for the signal pins for debugging.
2. It is recommended to reserve an ESD protection component for the antenna interface and the junction capacitance should not exceed 0.05 pF.
3. The single-ended impedance of the RF antenna is 50 Ω, and length should be minimized.



NOTE:

26 MHz and 32 kHz oscillators are recommended to be used and you need to design power supply circuits by yourself.



NOTE:

Design the 1.8 V ±0.1 V (at least 150 mA external current should be provided) power supply (AVDD_1V8) for the Bluetooth chip to provide the required voltage for its operation, and the remaining three power supply pins (DVDD_1V2, AVDD_1V8_FM and AVDD_1V8_BT) are internal power supply pins of the chip to be connected to external filter capacitors.

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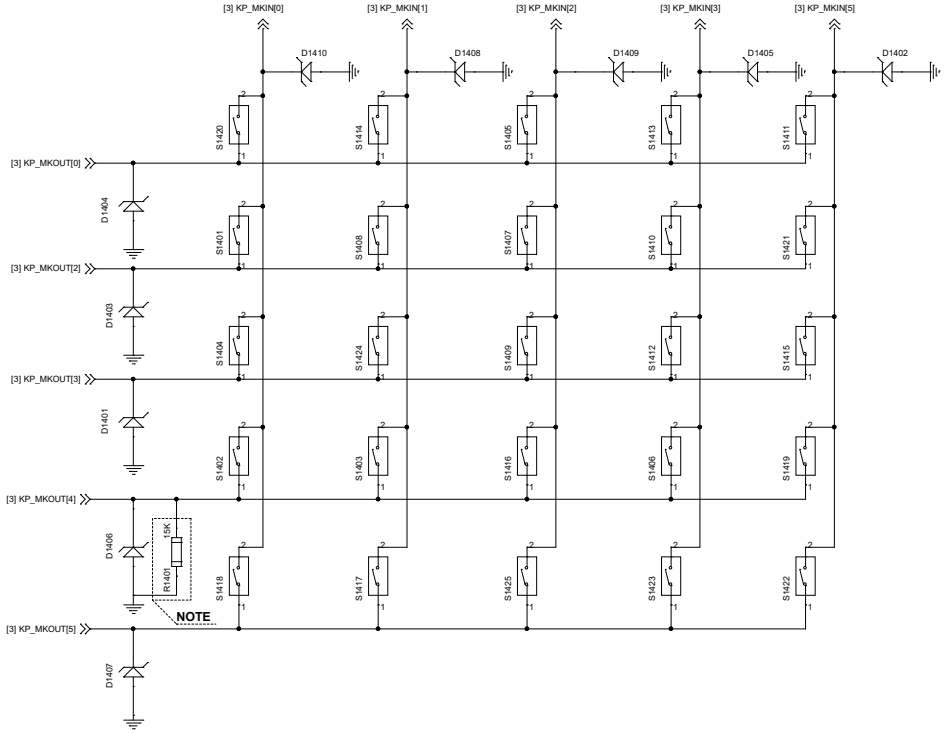
Matrix Keypad Interface Design



NOTE:

When pin 55 of the module is multiplexed into KP_MKOUT[4], it must be pulled down to the ground by adding an external 15 kΩ resistor.

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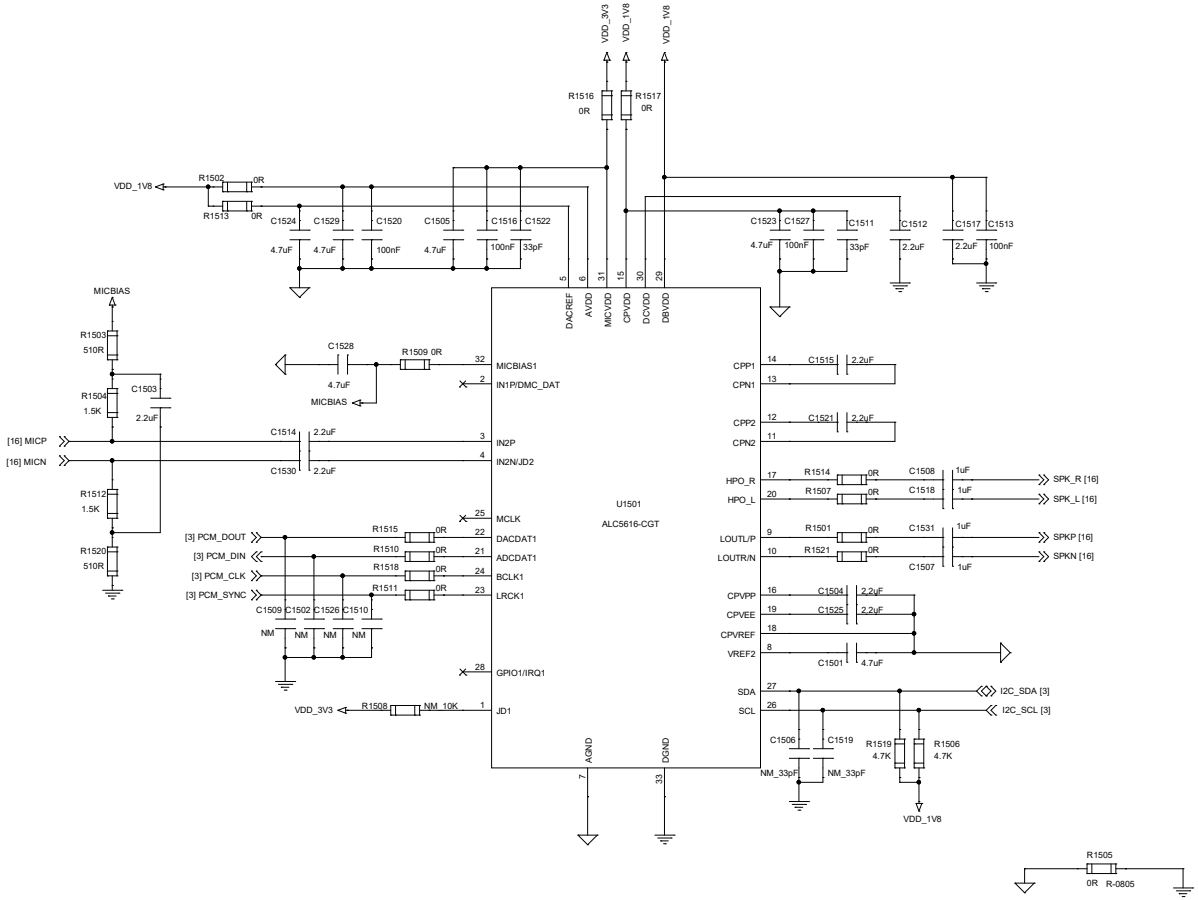
Audio Codec Design (ALC5616)



NOTE:

1. ALC5616 power-up sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD → MICVDD → software initialization.
2. ALC5616 power-down sequence: disable Codec function by software → MICVDD → DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.
3. Ensure all power supplies for the codec are powered on before the module automatically initializes the Codec via the I2C interface.
4. Differentiate between analog ground and digital ground. Connect analog ground and digital ground using a 0 Ω resistor (R-0805). Refer to "Audio Codec Interface Design" for more details.
5. For more details, please refer to the datasheet of ALC5616.
6. Reserve 33 pF capacitors for the signal pins for debugging.

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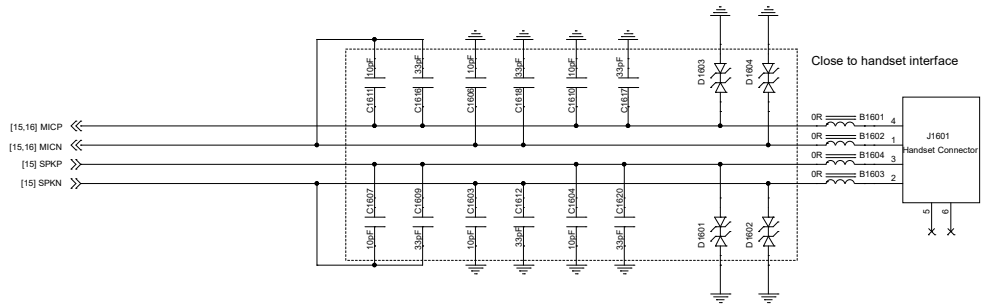
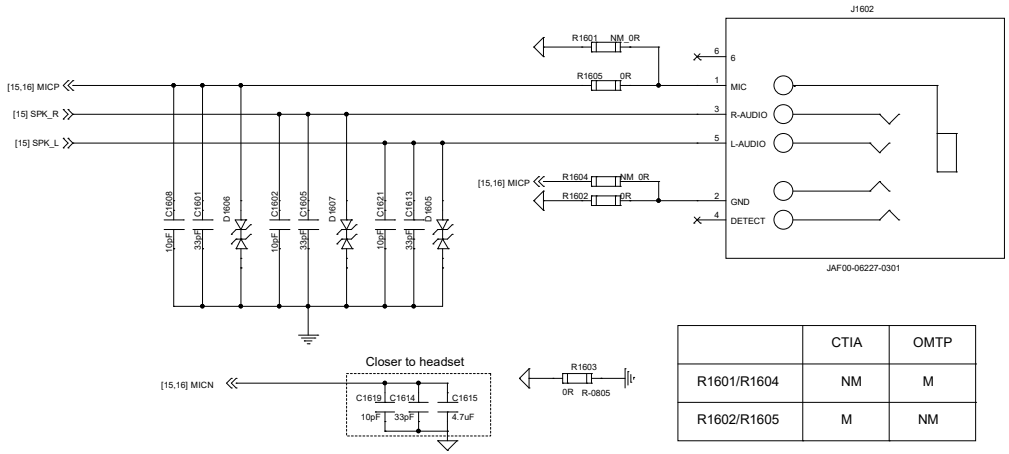
Audio Codec Interface Design

Handset Application



Headset Application

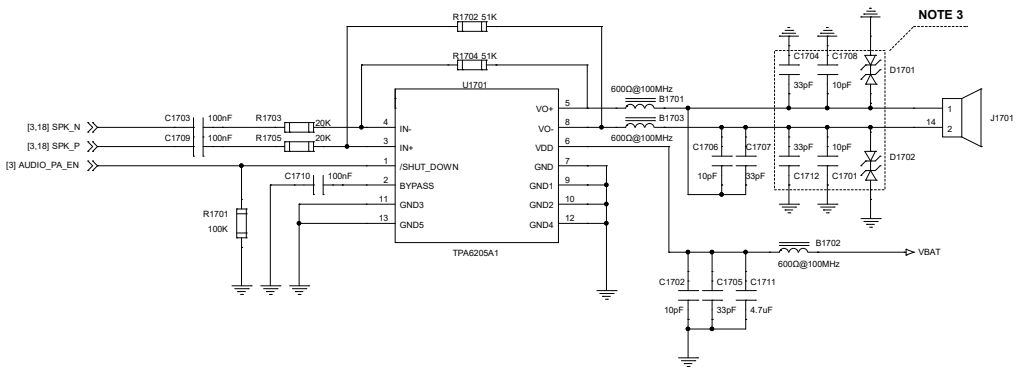


	CTIA	OMTP
R1601/R1604	NM	M
R1602/R1605	M	NM

NOTE:

1. The Codec analog output can drive handset and headset. For larger power loads such as loudspeaker, add an audio power amplifier in the design.
2. In handset application, route the MIC and SPK signal traces as differential pairs.
3. In headset application, route the MIC signal traces as a differential pair.
4. Surround all MIC and SPK signal traces with ground on the same layer and with ground planes above and below to minimize noise interference, such as clock and DC-DC signals.
5. Differentiate between analog ground and digital ground. Analog ground should have a direct via to digital ground through a 0 Ω resistor (R-0805).

Analog Audio Design (Audio Power Amplifier)



NOTE:

1. SPK_P and SPK_N channels are differential output channels intended for connecting to an external audio power amplifier.

   To eliminate Pop noise, it is recommended to utilize MAIN_DCD of the module as the control signal for the audio power amplifier's enable pin.

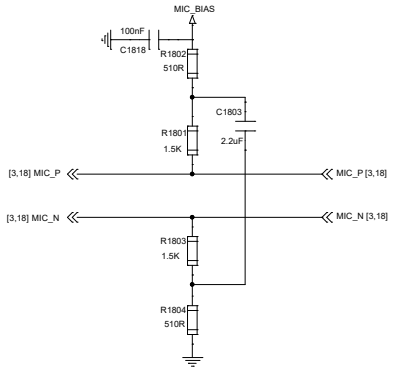
   For more information about AUDIO_PA_EN, please contact Quectel Technical Support.

2. The type of power amplifier in this design is for reference only. Select the appropriate audio power amplifier according to actual needs.
3. When designing the layout, ensure that filter capacitors and ESD protection components are placed close to the loudspeaker to filter out interference and provide adequate protection.
4. The selection of ESD protection components should consider the output voltage range of the audio power amplifier. Ensure that the output voltage of the amplifier remains

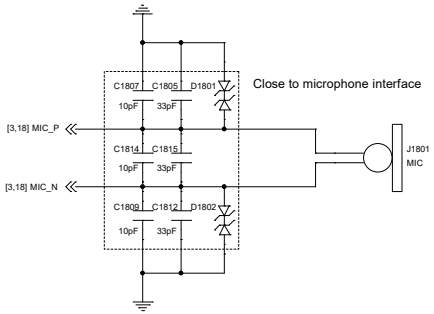
   within the maximum reverse working voltage range of the selected ESD protection components under normal operating conditions. This precaution helps prevent damage to the ESD protection components.

Analog Audio Design

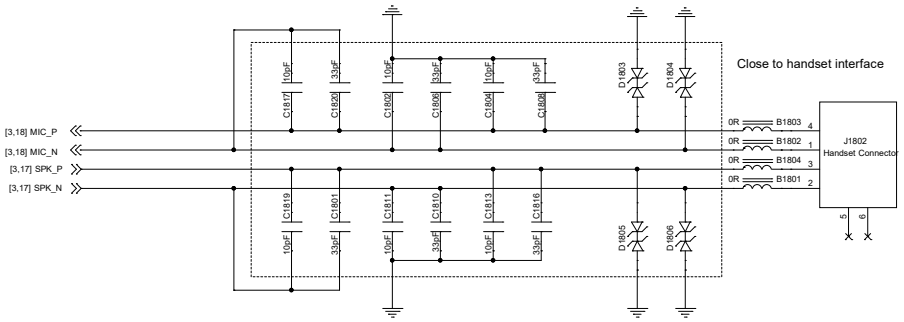
Microphone Bias Circuit



Microphone Application



Handset Application



NOTE:

1. Both the MIC and SPK signal traces need to be routed as differential pairs.
2. Surround all MIC and SPK signal traces with ground on the same layer and with ground planes above and below to minimize noise interference.
3. An external microphone bias circuit must be added when using electret microphone.
4. It is recommended to use 10 pF and 33 pF capacitors to filter RF interference.

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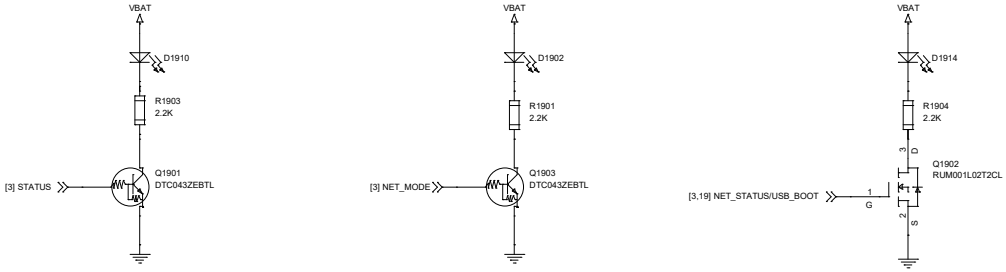
Other Designs

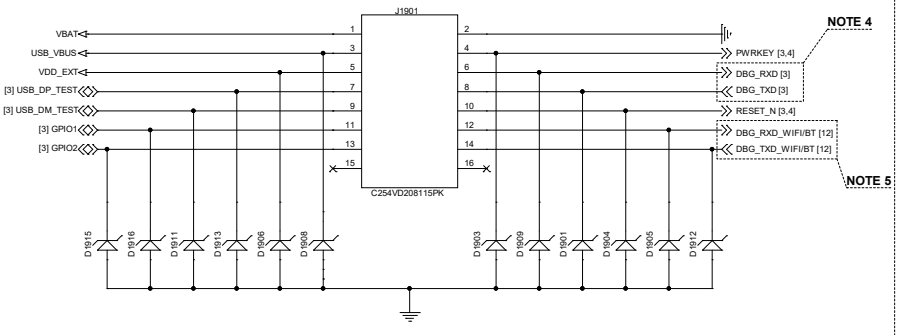
Indicators



NOTE:

1. For more details about STATUS , NET_MODE and NET_STATUS/USB_BOOT, see the hardware design document of the module.
2. To minimize the module's power consumption during the sleep mode of your device, replace the power supply (VBAT) of the STATUS, NET_MODE and NET_STATUS/USB_BOOT indicators with externally controllable sources and turn off the indicators when the module is in sleep mode.
3. Note that the maximum value of the MOSFET Q1902's Vgs (th) should not exceed 1 V, since the NET_STATUS/USB_BOOT pin of the module outputs high level by default. If a transistor such as Q1901 and Q1903 is used to replace the MOSFET, the NET_STATUS/USB_BOOT pin will be pulled down to low-level, and the module will enter the forced download mode and cannot be turned on normally.

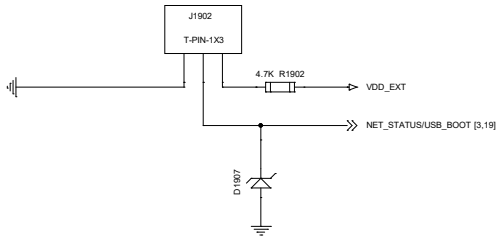
Reserved Test Points



NOTE:

1. Test points for both USB and debug UART interfaces are reserved for capturing logs.
2. Test points for USB interface can also be reserved for firmware upgrading.
3. The junction capacitance of the ESD protection components on USB data traces should be less than 2 pF.
4. The debug UART interface of EC600M supports a 1.8 V power domain. If your application operates at 3.3 V, use a voltage-level translator.
5. The debug UART interface of FC41D supports a 3.3 V power domain. If your application operates at 1.8 V, use a voltage-level translator.

USB_BOOT Interface



NOTE:

1. Make sure to reserve the USB_BOOT interface design and it is recommended to reserve a test point for NET_STATUS/USB_BOOT.
2. Before turning on the module, pull NET_STATUS/USB_BOOT down to GND to activate the forced download mode. This mode enables firmware upgrades via the USB interface.
3. The 6.0 and above version of QFlash tool must be used for firmware upgrading.

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