EC600M Series
QuecOpen&QuecPython Hardware Design

LTE Standard Module Series

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The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-05-19	Howell KANG/ Stefan FAN/ Jerry LIN	Creation of the document
1.0	2024-02-03	Howell KANG/ Stefan FAN/ Ronter ZHANG/ Jerry LIN/ Felix YE	First official release

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1 Introduction

This document defines the EC600M series module in QuecOpen® or QuecPython® solution and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module.

1.1. QuecOpen® Solution Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle.
- Simplify circuit and hardware structure design to reduce engineering costs.
- Miniaturize products.
- Reduce product power consumption.
- Apply OTA technology.
- Enhance product competitiveness and price-performance ratio.

1.2. QuecPython® Solution Introduction

QuecPython® is a Python runtime environment transplanted from MicroPython® open-source library. It is a new IoT development solution based on Quectel's module that uses MircroPython® to invoke the module's software functions and external hardware interfaces to help users perform the secondary development of embedded applications. Its main advantages are as follows:

- Efficient and convenient Python development: provide abundant API to ensure the stability and functionality of the interfaces to the greatest extent.
- Compatible with MicroPython®, easy to update and iterate.
- High data security for its architecture.
- Strong portability for its design architecture can be quickly transplanted and adapted to other application platforms.

1.3. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO_DATA pins, SDIO_DATA0, SDIO_DATA1, SDIO_DATA2 and SDIO_DATA3.

2 Product Overview

The module is an SMD type module with compact packaging, which is engineered to meet the demands in M2M applications.

Table 2: Basic Information

EC600M Series	
Packaging type	LCC + LGA
Pin counts	EC600M-CN: 100
	EC600M-EU: 106
Dimensions	(21.9 ±0.15) mm × (22.9 ±0.15) mm × (2.4 ±0.2) mm
Weight	Approx. 2.0 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

	EC600M-CN	EC600M-EU
LTE-FDD	B1/B3/B5/B8	B1/B3/B5/B7/B8/B20/B28
LTE-TDD	B34/B38/B39/B40/B41	B38/B40/B41

NOTE

Band 41 only supports 140 MHz (2535–2675 MHz).

2.2. Key Features

Table 4: Key Features

Categories	Descriptions
Supply Voltage	● 3.4–4.3 V ● Typ. 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: stored in USIM card and ME, ME by default ● SGS SMS (default), IMS SMS (optional)
USB Interface	● Compliant with USB 2.0 (slave mode only), with data transmission rates up to 480 Mbps ● Used for data transmission, software debugging and firmware upgrade ● Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–6.5 and Android 4.x–13.x
Forced Download Interface	Supports one forced download interface
USIM Interfaces	● Supports two USIM interfaces: 1.8 V and 3.0 V ● Supports dual USIM single standby function
UART	**Main UART:** ● Used for data transmission ● Baud rate: 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for partial log output ● Baud rate: 115200 bps **Auxiliary UART:** ● Used for communication with peripherals ● Baud rate: 115200 bps ● Multiplexed from SPI_RXD/SPI_TXD or MAIN_CTS/MAIN_RTS
PCM Interface	● Used for audio data transmission with external codec ● Supports 16-bit linear data format ● Supports short frame synchronization: the module only works as a master device
I2C Interface	● Supports one I2C interface ● Complies with I2C-bus specification
LCM Interface	● Supports LCD display module with a maximum resolution of 240 × 320 ● Supports SPI four-wire single data line transmission ● Supports RGB565 format output

SPI	Supports slave* and master mode , with a maximum clock frequency of 26 MHz
Matrix Keypad Interface	Supports 5 × 5 matrix keypad
Camera Interface	● Supports up to 0.3 MP ● Supports the single data line or dual data line transmission of SPI
Audio Features	● Supports one digital audio interface: PCM interface ● Supports one analog audio input and one analog audio output ● LTE: AMR/AMR-WB ● Supports echo cancellation and noise suppression
ADC Interface	Supports two ADC interfaces
Network Indication	● NET_MODE indicates the network registration status ● NET_STATUS/USB_BOOT indicates the network operation status
Antenna Interface	● LTE/Wi-Fi Scan antenna interface (ANT_MAIN) ● 50 Ω characteristic impedance
Position Fixing	Supports Wi-Fi scan function by using the main antenna interface
Transmitting Power	● LTE-FDD: Class 3 (23 dBm ±2 dB) ● LTE-TDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Supports 3GPP Rel-13 Cat 1 bis FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidths ● Supports UL QPSK, 16QAM modulations ● Supports DL QPSK, 16QAM, 64QAM modulations ● Max. transmission data rates: – LTE-FDD: 10 Mbps (DL)/5 Mbps (UL) – LTE-TDD: 8.96 Mbps (DL)/3.1 Mbps (UL)
Internet Protocol Features [1]	● Compliant with TCP/UDP/NTP/NITZ/FTP/HTTP/PING/HTTPS/FTPS/SSL/FILE/MQTT/CMUX*/MMS*/ PPP*/SMTP*/SMTPS* protocols ● Supports PAP and CHAP for PPP connections
Temperature Ranges	● Operating temperature range [2]: -35 °C to +75 °C ● Extended temperature range [3]: -40 °C to +85 °C ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	Use USB 2.0 interface or DFOTA to upgrade
RoHS	All hardware components fully compliant with EU RoHS directive

[1] PPP*/NTP/NITZ/CMUX*/HTTPS/FTPS/SSL/FILE/MMS*/SMTP*/SMTPS* are optional, please consult Quectel Technical Support for details.
[2] Within this range, the module's indicators comply with 3GPP specification requirements.
[3] Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

NOTE

1. Wi-Fi Scan that only supports receiving, shares the same antenna interface with main antenna. The two functions cannot be used at the same time.
2. Different tools must be used for firmware upgrade for QuecOpen and QuecPython solutions.
   - QuecOpen: The 6.0 and above version QFlash tool must be used for firmware upgrade.
   - QuecPython: The 3.0 and above version QPYcom tool must be used for firmware upgrade.

   For more details about QPYcom tool, please visit https://python.quectel.com/doc/Application_guide/zh/dev-tools/QPYcom/index.html.

2.3. Functional Diagram

The block diagram illustrates the following major functional parts:

- Power management
- Baseband part
- Flash
- Radio frequency part
- Peripheral interfaces

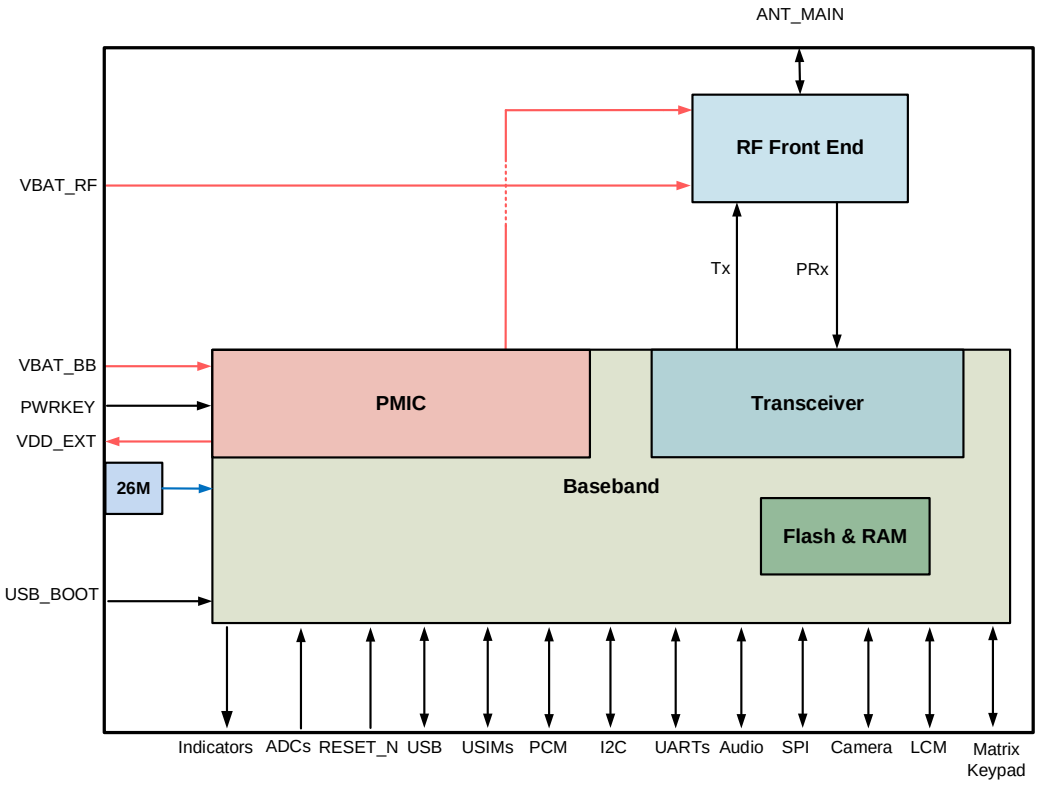


Figure 1: Functional Diagram

2.4. Pin Assignment

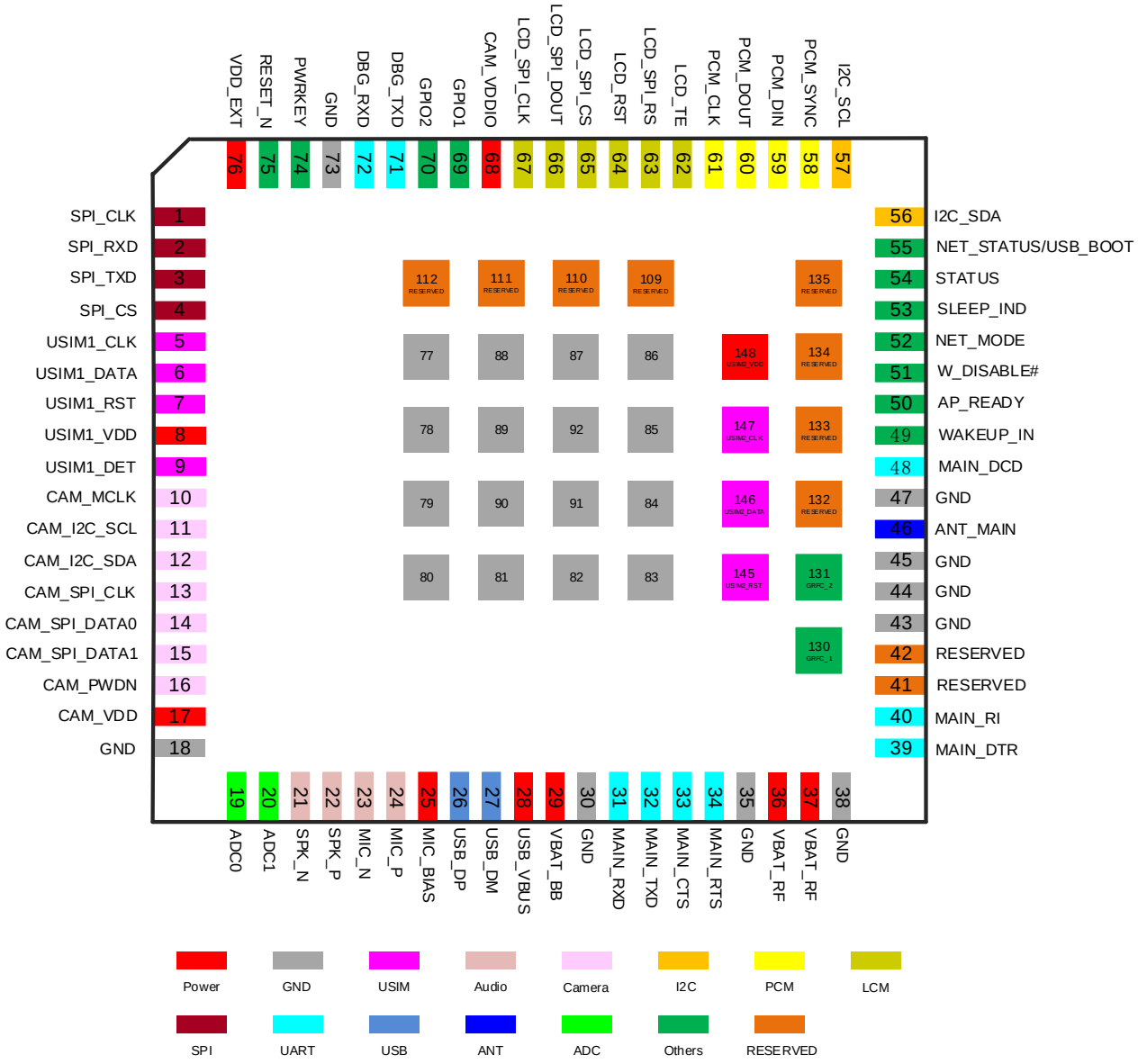


Figure 2: Pin Assignment (Top View)

NOTE

1. Do not pull NET_STATUS/USB_BOOT to low level before the module starts up successfully.
2. Keep all RESERVED pins and unused pins open.
3. Ensure that there is a complete reference ground plane under the module, and the plane shall be placed as close to the module layer as possible. At least 4-layer board is recommended.
4. Different tools must be used for firmware upgrade for QuecOpen and QuecPython solutions.
   - QuecOpen: The 6.0 and above version QFlash tool must be used for firmware upgrade.

- QuecPython: The 3.0 and above version QPYcom tool must be used for firmware upgrade. For more details about QPYcom tool, please visit https://python.quectel.com/doc/Application_guide/zh/dev-tools/QPYcom/index.html.

5. EC600M-CN does not have pins 130–135.

2.5. Pin Description

Table 5: Parameter Definition

Parameters	Descriptions
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	29	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.4 V Vnom = 3.8 V	External power supply must be provided with

VBAT_RF	36, 37	PI	Power supply for the module's RF part		sufficient current of at least 2.0 A. It is recommended to add a TVS externally. Test points are recommended to be reserved.
GND	18, 30, 35, 38, 43–45, 47, 73, 77–92				
Power Supply Output					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_EXT	76	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
Turn On/Off/Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	74	DI	Turn on/off the module	V_{IL}max = 0.5 V Vnom = VBAT_BB	Turn on/off the module. A test point is recommended to be reserved.
RESET_N	75	DI	Reset the module	V_{IL}max = 0.5 V Vnom = 1.8 V	Active low. A test point is recommended to be reserved if unused.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_MODE	52	DO	Indicate the module's network registration mode	1.8 V	If unused, keep them open.
STATUS	54	DO	Indicate the module's operation status		

SLEEP_IND*	53	DO	Indicate the module's sleep mode		
NET_STATUS/ USB_BOOT	55	DO	Indicate the module's network activity status		After the module is turned on normally, this pin is used as a network status indicator. Do not pull down this pin before the module is powered on normally. A test point is recommended to be reserved.
Forced Download Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_STATUS/ USB_BOOT	55	DI	Force the module into download mode	1.8 V	Pull this pin down to ground before turning on the module, and the module will enter the forced download mode when turning on. Active low. A test point is recommended to be reserved.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_DP	26	AIO	USB 2.0 differential data (+)		Complies with USB 2.0. A differential impedance of 90 Ω is needed. Test points must be reserved.
USB_DM	27	AIO	USB 2.0 differential data (-)		

USB_VBUS	28	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	A test point must be reserved.
USIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_CLK	5	DO	USIM1 card clock	1.8/3.0 V	
USIM1_DATA	6	DIO	USIM1 card data		
USIM1_RST	7	DO	USIM1 card reset		
USIM1_VDD	8	PO	USIM1 card power supply		Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM1_DET	9	DI	USIM1 card hot-plug detect	1.8 V	If unused, keep it open.
USIM2_RST	145	DO	USIM2 card reset	1.8/3.0 V	
USIM2_DATA	146	DIO	USIM2 card data		
USIM2_CLK	147	DO	USIM2 card clock		
USIM2_VDD	148	PO	USIM2 card power supply		Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RXD	31	DI	Main UART receive	1.8 V	If unused, keep them open.
MAIN_TXD	32	DO	Main UART transmit		
MAIN_CTS	33	DO	Clear to send signal from the module		Connect to the MCU's CTS. If unused, keep it open.

MAIN_RTS	34	DI	Request to send signal to the module		Connect to the MCU's RTS. If unused, keep it open.
MAIN_DTR	39	DI	Main UART data terminal ready		If unused, keep them open.
MAIN_RI*	40	DO	Main UART ring indication		
MAIN_DCD	48	DO	Main UART data carrier detection		
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	71	DO	Debug UART transmit	1.8 V	Test points must be reserved.
DBG_RXD	72	DI	Debug UART receive		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SDA	56	OD	I2C serial data	1.8 V	An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SCL	57	OD	I2C serial clock		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	58	DO	PCM data frame sync	1.8 V	If unused, keep them open.
PCM_DIN	59	DI	PCM data input		
PCM_DOUT	60	DO	PCM data output		
PCM_CLK	61	DO	PCM clock		
SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CLK	1	DIO	SPI clock	1.8 V	When the module

SPI_RXD	2	DI	SPI data input		is used as master device, SPI_CLK and SPI_CS pins are output signals; when the module is used as slave device*, SPI_CLK and SPI_CS pins are input signals. If unused, keep them open.
SPI_TXD	3	DO	SPI data output		
SPI_CS	4	DIO	SPI chip select		
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_SPI_CS	65	DO	LCD SPI chip select	1.8 V	If unused, keep them open.
LCD_TE	62	DI	LCD tearing effect		
LCD_SPI_CLK	67	DO	LCD SPI clock		
LCD_SPI_RS	63	DO	LCD SPI register select		
LCD_RST	64	DO	LCD reset		
LCD_SPI_DOUT	66	DO	LCD SPI data output		
Camera Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CAM_VDD	17	PO	Camera Power supply	2.8 V/ 100 mA	If unused, keep them open.
CAM_MCLK	10	DO	Camera master clock	1.8 V	
CAM_SPI_CLK	13	DI	Camera SPI clock		
CAM_SPI_DATA0	14	DI	Camera SPI data bit 0		
CAM_SPI_DATA1	15	DI	Camera SPI data bit 1		
CAM_I2C_SCL	11	OD	Camera I2C clock		

CAM_I2C_SDA	12	OD	Camera I2C data		
CAM_PWDN	16	DO	Camera power down		
CAM_VDDIO	68	PO	Camera I/O power supply	Vnom = 1.8 V	
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPK_N	21	AO	Analog audio differential output (-)		Used for earpiece interface. Class AB power amplifier, with maximum output power 37 mW @ THD = 1 %, R = 32 Ω. If the output power cannot meet the demand, this interface can be used to drive an external power amplifier device. If unused, keep them open.
SPK_P	22	AO	Analog audio differential output (+)		
MIC_N	23	AI	Microphone analog input (-)		Electret microphones are usually used. If unused, keep them open.
MIC_P	24	AI	Microphone analog input (+)		
MIC_BIAS	25	PO	Bias voltage output for microphone	Vnom = 1.8 V	
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	19	AI	General-purpose ADC interface	0–1.2 V	If unused, keep them open.
ADC1	20	AI			
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

ANT_MAIN	46	AIO	Main antenna/Wi-Fi Scan antenna interface		50 Ω characteristic impedance.
Antenna Tuner Control Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC_1	130	DO	Generic RF controller	1.8 V	EC600M-CN does not have pins 130 and 131. If unused, keep them open.
GRFC_2	131	DO	Generic RF controller		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN*	49	DI	Wake up the module	1.8 V	If unused, keep them open.
AP_READY*	50	DI	Application processor ready		
W_DISABLE#*	51	DI	Airplane mode control		
GPIO					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	69	DIO	General-purpose input/output	1.8 V	If unused, keep them open.
GPIO2	70	DIO			
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	41, 42, 109–112, 132–135				Keep them open. EC600M-CN does not have pins 132–135.

2.6. EVB Kit

Quectel supplies an evaluation board (LTE OPEN EVB) with accessories to develop and test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Overview of Operating Modes

Modes	Functions	
Full Functionality Mode	Idle	Software is active. The module is registered on the network but there is no data interaction.
	Voice/Data	Network connection is ongoing. Power consumption is decided by the network setting and data transmission rate.
Minimum Functionality Mode	● Use API can set the module to the minimum functionality mode without removing the power supply. ● Both RF function and USIM card are disabled.	
Airplane Mode	● Use API can set the module to airplane mode. ● RF function is disabled.	
Sleep Mode	Power consumption of the module will be reduced to a minimal level. The module can still receive paging, SMS, voice call and TCP/UDP data from network.	
Power Down Mode	PMIC shuts down the power supply. Software is not active. However, operating voltage connected to VBAT_BB/VBAT_RF remains applied.	

The following table shows the related API used for operating modes.

Table 8: Related API of Operating Modes

		QuecOpen	QuecPython
	API	*ql_dev_set_modem_fun()*	*net.setModemFun()*
Minimum Functionality Mode (Both RF function and USIM card are disabled)	Values of *function/fun*	*QL_DEV_MODEM_MIN_FUN*	0

Full Functionality Mode (Default)	*QL_DEV_MODEM_FULL_FUN*	1
Airplane Mode (RF function is disabled)	*QL_DEV_MODEM_DISBLE_TRANSMIT_AND_RECEIVE_RF_CIRCUITS*	4

NOTE

For more details about API of operating modes:

- QuecOpen: See ***document [2]***;
- QuecPython: Please visit https://python.quectel.com/doc/API_reference/zh/iotlib/net.html.

3.2. Sleep Mode

In sleep mode, power consumption of the module can be reduced to a minimal level.

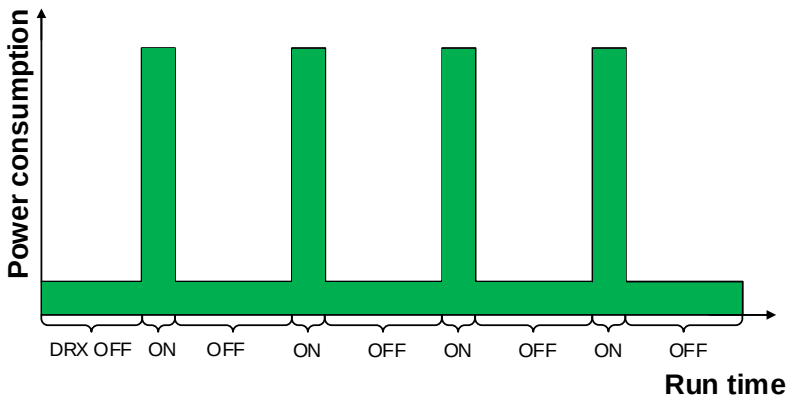


Figure 3: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

The following three conditions should be met to set the module into sleep mode.

- Enable sleep function through API.
- All GPIOs which can be configured as interrupt wake-up function are in non-wake-up state.
- Disconnect USB_VBUS.

The following table shows the related API used to enabling sleep mode.

Table 9: Related API of Enabling Sleep Mode

	QuecOpen	QuecPython
API	*ql_autosleep_enable()*	*pm.autosleep()*

The following figure shows the connection between the module and the host.

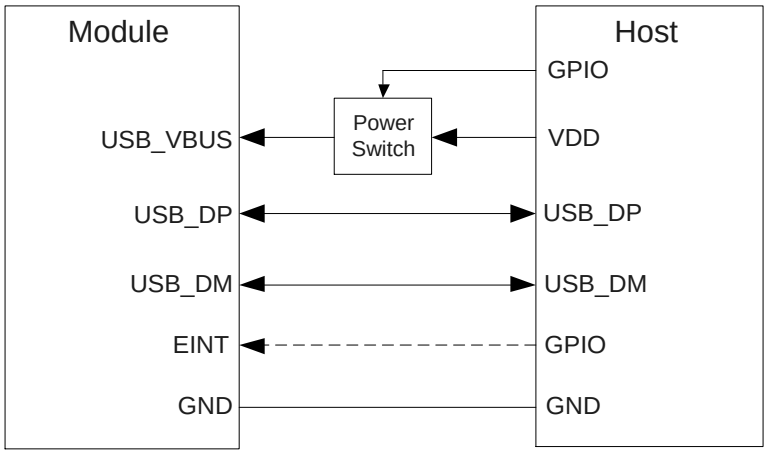


Figure 4: Sleep Mode Application

You can wake up the module by turning on the power switch to power the USB_VBUS or by using GPIO interrupts.

NOTE

1. Pay attention to the level matching shown in the dotted line between the module and the host in the circuit diagrams.
2. For more details about API of enabling sleep mode:
   - QuecOpen: See ***document [3]***.
   - QuecPython: Please visit https://python.quectel.com/doc/API_reference/zh/syslib/pm.html.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all API related to it will be inaccessible. This mode can be set via following ways:

Software:

The airplane mode can be set through API. For more details, see ***Table 8***.

3.4. Power Supply

3.4.1. Power Supply Interface

The module provides three VBAT pins dedicated for connecting with the external power supply:

Table 10: Pin Description of Power Supply Interface

Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	29	PI	Power supply for the module's baseband part	External power supply must be provided with sufficient current of at least 2.0 A. It is recommended to add a TVS externally. Test points are recommended to be reserved.
VBAT_RF	36, 37	PI	Power supply for the module's RF part	
GND	18, 30, 35, 38, 43–45, 47, 73, 77–92			

3.5. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of at least 2 A. If the voltage difference between input voltage and the desired output VBAT is small, it is suggested to use an LDO; if the voltage difference is large, then a buck converter is suggested to use.

The following figure illustrates a reference design for 5 V input power supply.

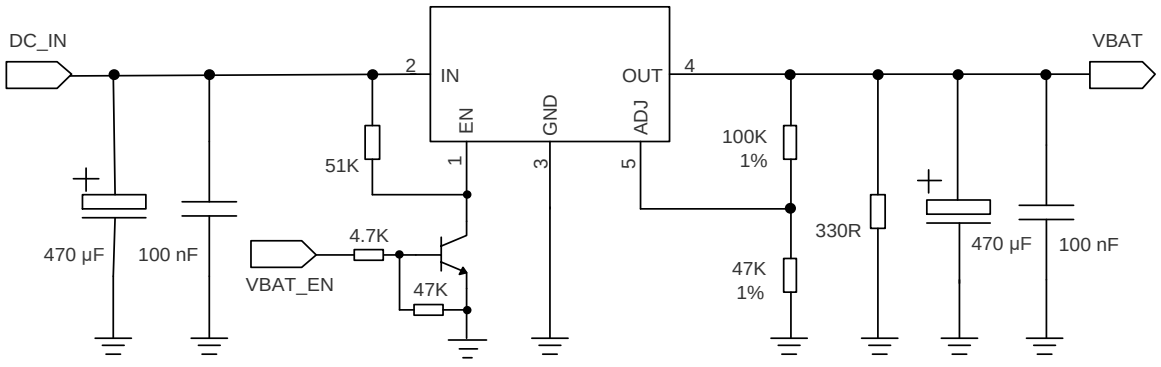


Figure 5: Reference Design of Power Input

3.5.1. Power Supply Voltage Monitoring

You can use the following API to monitor and query the VBAT_BB voltage.

Table 11: Related API of Monitoring Power Supply Voltage

	QuecOpen	QuecPython
API	*ql_get_battery_vol()*	*Power.getVbatt()*

NOTE

For more details about API of monitoring power supply voltage:

- QuecOpen: See ***document [4]***;
- QuecPython: Please visit https://python.quectel.com/doc/API_reference/zh/peripherals/misc.Power.html.

3.5.2. Requirements for Voltage Stability

The power supply range of the module is from 3.4 V to 4.3 V. Ensure the input voltage never drops below 3.4 V.

To decrease the voltage drop, use bypass capacitors of about 100 µF with low ESR (ESR ≤ 0.7 Ω) and reserve a multi-layer ceramic chip (MLCC) capacitor array due to their ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array respectively, and place these capacitors close to the VBAT pins. When the external power supply is connected to the module, VBAT_BB and VBAT_RF need to be routed in star configuration. The width of VBAT_BB trace and VBAT_RF trace should be at least 1 mm and 2 mm respectively. In principle, the longer the VBAT trace is, the wider it will be.

In order to avoid the ripple and surge and ensure the stability of the power supply to the module, add a TVS diode with V_{RWM} = 4.7 V, low-clamp voltage and peak pulse current Ipp at the front end of the power supply.

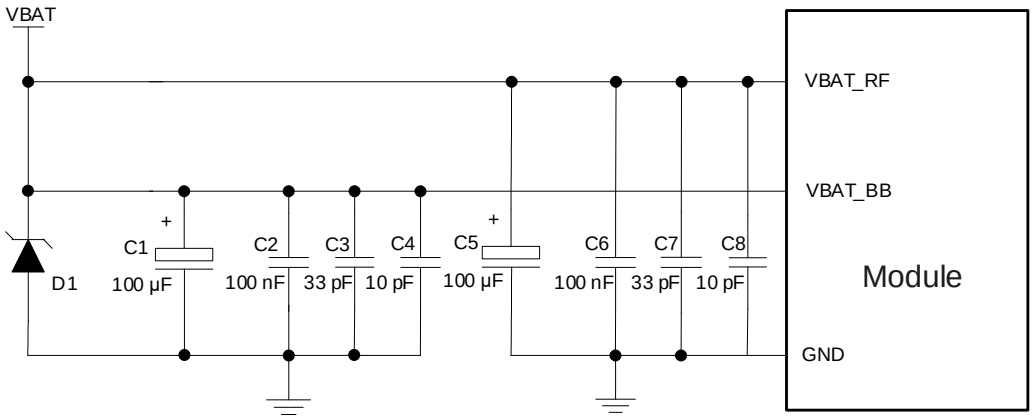


Figure 6: Reference Design of Power Supply

3.6. Turn On

3.6.1. Turn On with PWRKEY

Table 12: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	74	DI	Turn on/off the module.	A test point is recommended to be reserved.

When the module is in power-down state, it can be turned on by driving PWRKEY low for at least 700 ms. It is recommended to use an open drain/collector driver to control PWRKEY.

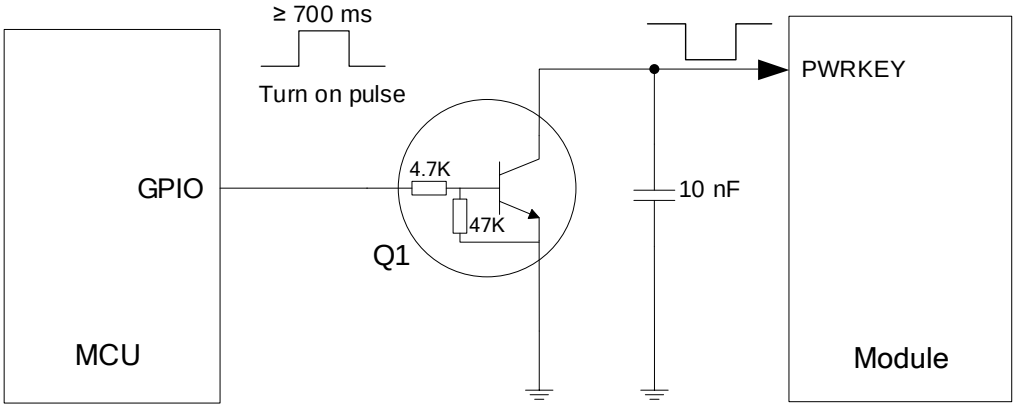


Figure 7: Reference Design of Turn-on with Driving Circuit

Another way to control PWRKEY is by using a push button directly. When pressing the button, an electrostatic strike may be generated from finger. Therefore, a TVS should be placed near the push button.

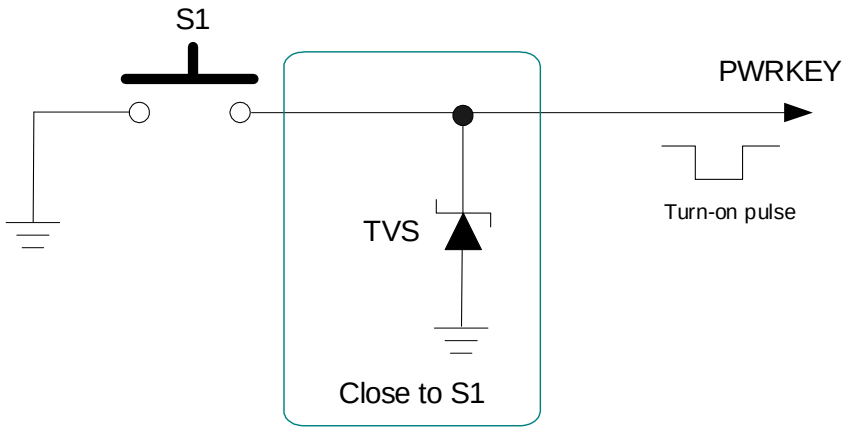


Figure 8: Reference Design of Turn-on with a Button

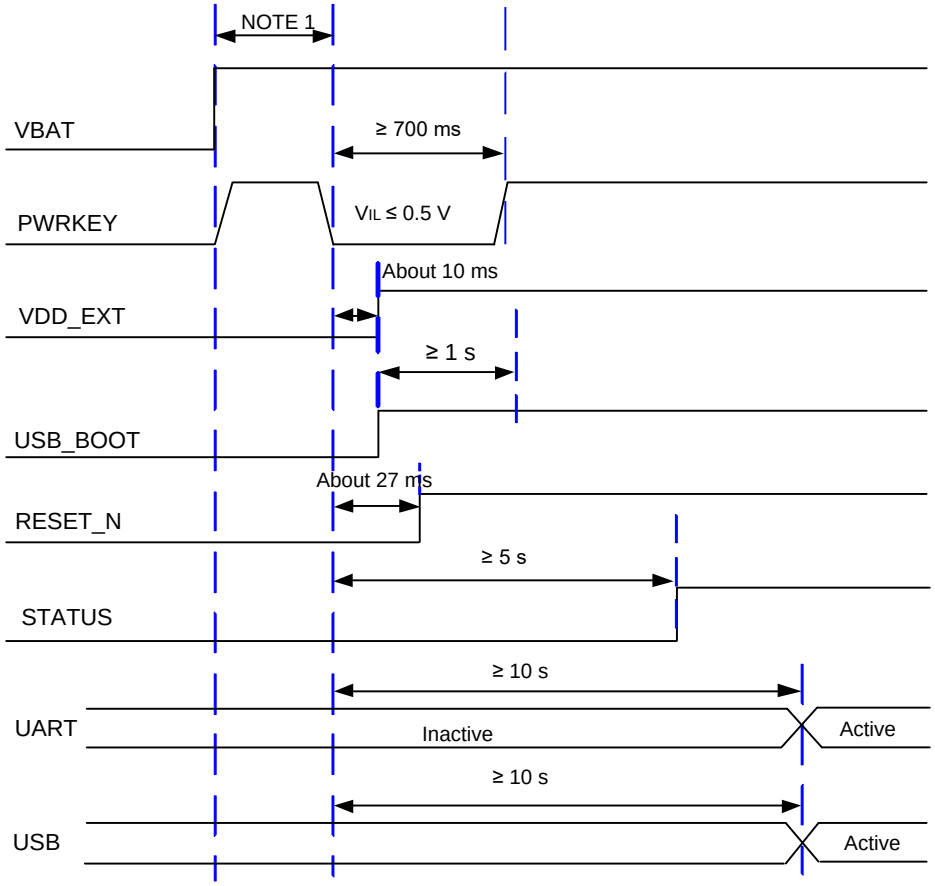


Figure 9: Timing Sequence of Turn-on with PWRKEY

NOTE

1. Ensure that VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to be turned on automatically when powered up while turn-off function is not needed, PWRKEY can be driven low directly to ground with a recommended 4.7 kΩ resistor.

3.7. Turn Off

3.7.1. Turn Off with PWRKEY

Drive PWRKEY low for at least 650 ms and then release it, the module will execute power-down procedure.

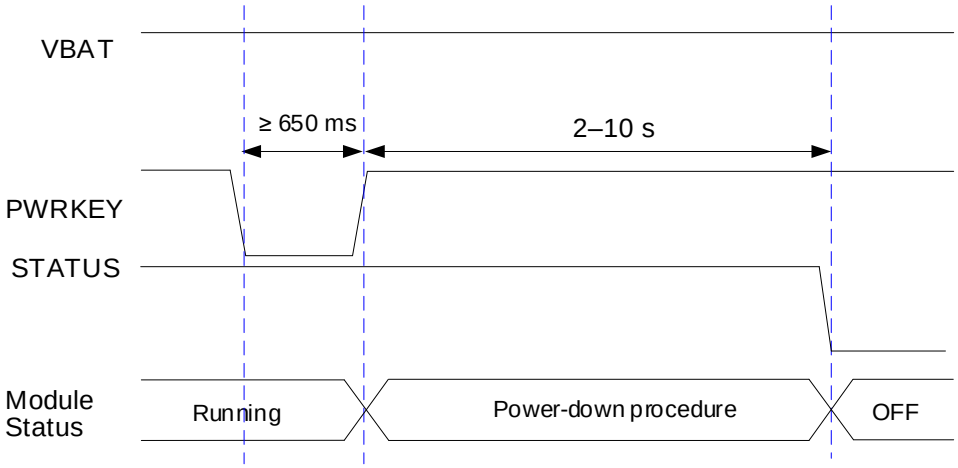


Figure 10: Timing Sequence of Turn-off with PWRKEY

3.7.2. Turn Off with API

To turn off the module, you can also execute API, which has similar timing and effect as turning off the module through driving PWRKEY low.

Table 13: Related API of Turning off the Module

	QuecOpen	QuecPython
API	*ql_power_down()*	*Power.powerDown()*

NOTE

1. To avoid corrupting the data in the internal flash, do not cut off the power supply when the module works normally. Only after shutting down the module with PWRKEY or API, can you cut off the power supply.
2. When turning off module with the API, keep the PWRKEY at high level, otherwise the module will be turned on again automatically after successful turn-off.
3. For more details about API of turning off the module:
   - QuecOpen: See ***document [5]***;
   - QuecPython: Please visit https://python.quectel.com/doc/API_reference/zh/peripherals/misc.Power.html.

3.8. Reset

Drive RESET_N low for at least 300 ms and then release it can reset the module. RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 14: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	75	DI	Reset the module	Active low. A test point is recommended to be reserved if unused.

The recommended circuit for reset function is similar to PWRKEY control circuit, you can use open drain/collector driver or button to control RESET_N.

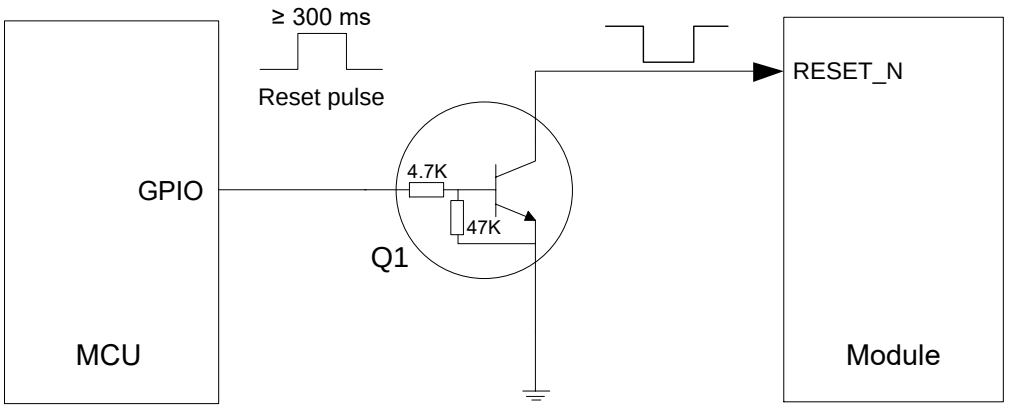


Figure 11: Reference Design of Reset with Driving Circuit

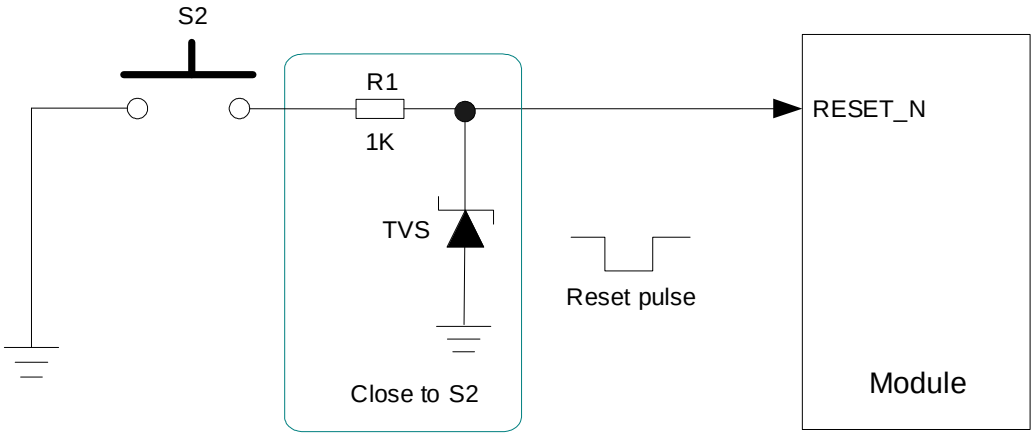


Figure 12: Reference Design of Reset with a Button

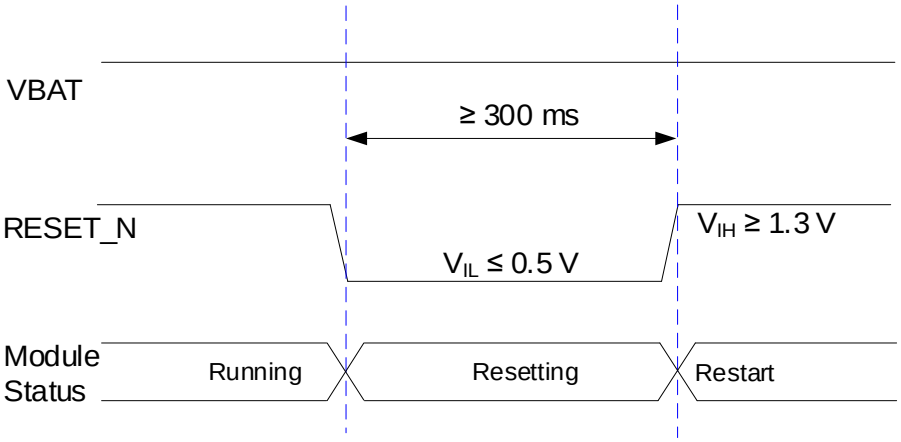


Figure 13: Timing Sequence of Reset

NOTE

1. Use RESET_N only when you fail to turn off the module with the API or PWRKEY.
2. Make sure the capacitance on PWRKEY and RESET_N never exceeds 10 nF.

4 Application Interfaces

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specifications and supports High-Speed (480 Mbps) and Full-Speed (12 Mbps) modes. The USB interface can only serve in the slave mode. It can be used for data transmission, software debugging and firmware upgrade.

Table 15: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	26	AIO	USB 2.0 differential data (+)	Complies with USB 2.0. A differential impedance of 90 Ω is needed. Test points must be reserved.
USB_DM	27	AIO	USB 2.0 differential data (-)	
USB_VBUS	28	AI	USB connection detect	A test point must be reserved.

Reserve test points for debugging and firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

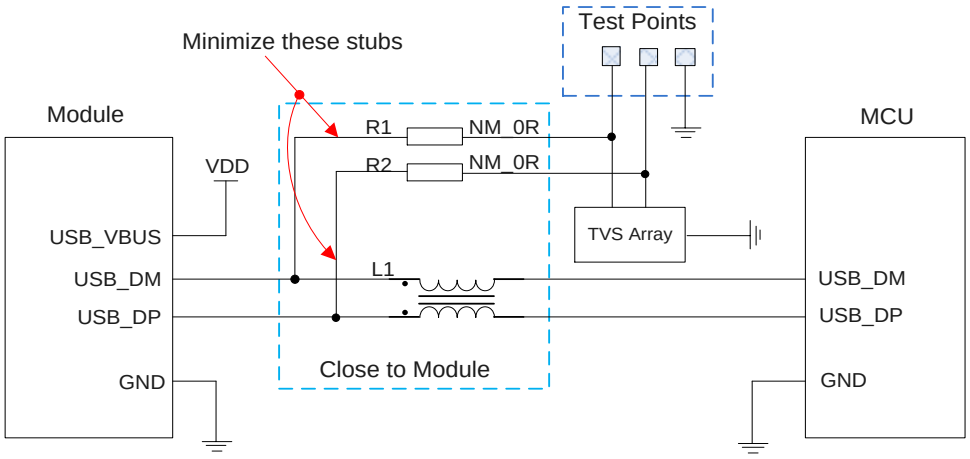


Figure 14: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI. Meanwhile, the R1 and R2 should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. To ensure the signal integrity of USB data traces, L1, R1 and R2 must be placed close to the module, and the resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

When designing the USB interface, you should follow the following principles to meet USB 2.0 specification.

- Route the USB signal traces as differential pairs in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. The impedance of USB differential trace is 90 Ω.
- To preserve signal quality, do not route signal traces under or near crystals, oscillators, magnetic devices and RF signal traces.
- Pay attention to the selection of the ESD component on the USB data traces. Its stray capacitance should not exceed 2 pF and should be placed as close as possible to the USB connector.

For more details about the USB specifications, visit http://www.usb.org/home.

4.2. Forced Download Interface

The module provides a NET_STATUS/USB_BOOT for forced download. You can make the module enter forced download mode by driving NET_STATUS/USB_BOOT low to GND before turning on the module. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 16: Pin Description of NET_STATUS/USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS/ USB_BOOT	55	DI	Force the module into download mode	1.8 V power domain. Pull this pin down to ground before turning on the module, and the module will enter the forced download mode when turning on. Active low. A test point is recommended to be reserved.

The following figure shows a reference design of NET_STATUS/USB_BOOT interface.

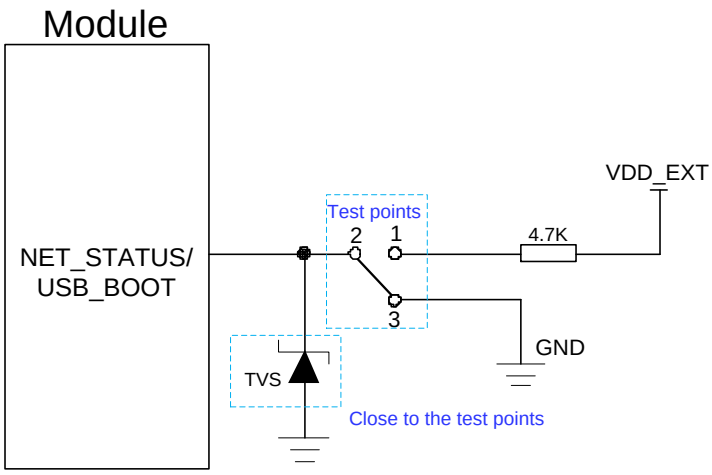


Figure 15: Reference Design of USB_BOOT

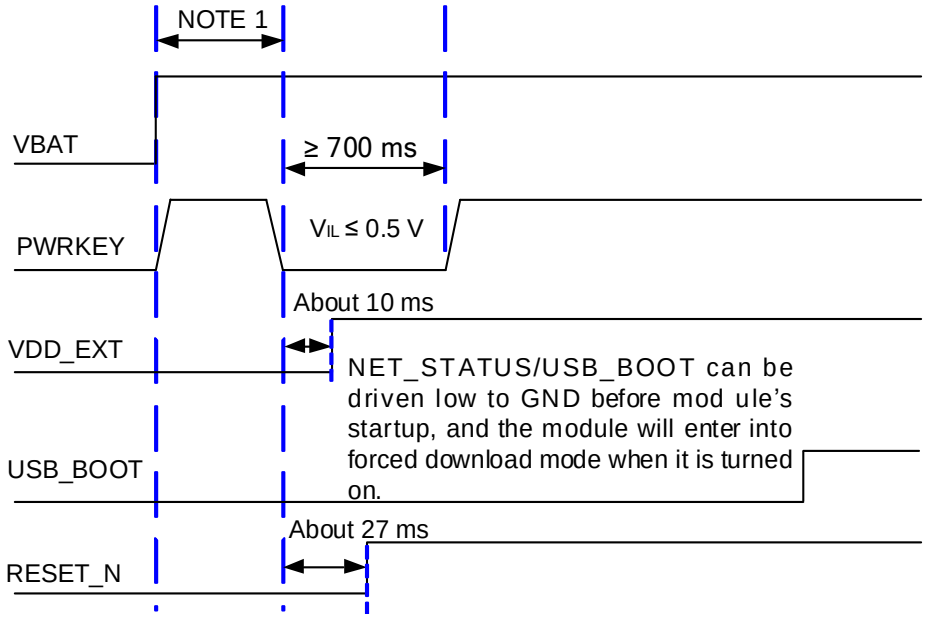


Figure 16: Timing Sequence of Entering Forced Download Mode

NOTE

1. Ensure VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low shall be not less than 30 ms.
2. Follow the above timing sequence when using MCU to control module to enter the forced download mode. Directly connect the test points as shown in ***Figure 15*** can manually force the module to enter download mode.
3. Different tools must be used for firmware upgrade for QuecOpen and QuecPython solutions.
   - QuecOpen: The 6.0 and above version QFlash tool must be used for firmware upgrade.

- QuecPython: The 3.0 and above version QPYcom tool must be used for firmware upgrade.

For more details about QPYcom tool, please visit https://python.quectel.com/doc/Application_guide/zh/dev-tools/QPYcom/index.html.

4.3. USIM Interfaces

The module has two USIM interfaces, and it meets ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V USIM card is supported, and the module supports dual USIM card single standby function.

Table 17: Pin Description of USIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_CLK	5	DO	USIM1 card clock	
USIM1_DATA	6	DIO	USIM1 card data	
USIM1_RST	7	DO	USIM1 card reset	
USIM1_VDD	8	PO	USIM1 card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM1_DET	9	DI	USIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM2_RST	145	DO	USIM2 card reset	
USIM2_DATA	146	DIO	USIM2 card data	
USIM2_CLK	147	DO	USIM2 card clock	
USIM2_VDD	148	PO	USIM2 card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.

The module supports USIM card hot-plug via USIM_DET (level trigger pin), and both high-level and low-level detections are supported.

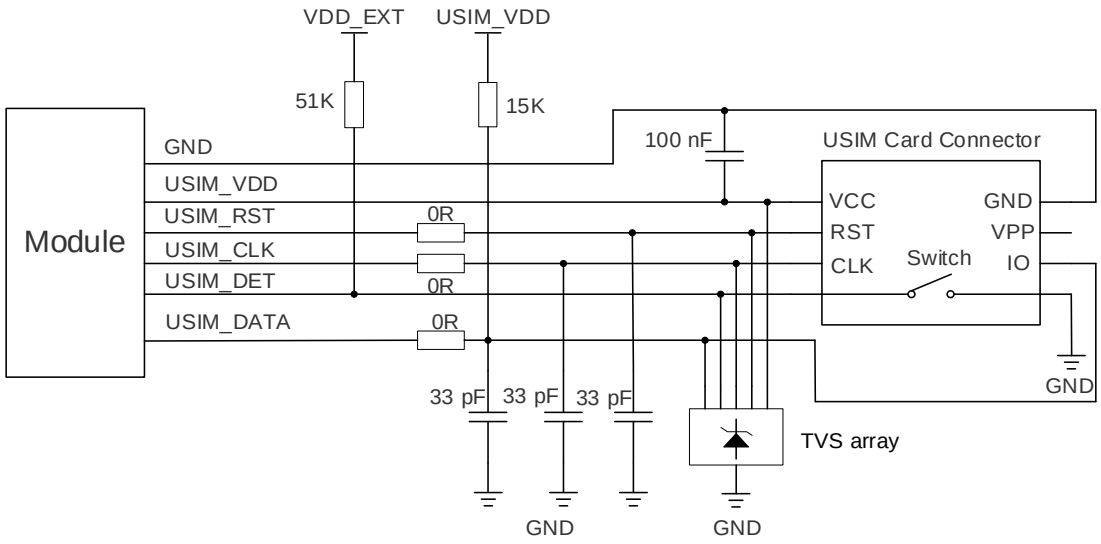


Figure 17: Reference Design of USIM Interface with an 8-pin USIM Card Connector

If the USIM card detection function is not needed, keep USIM_DET open.

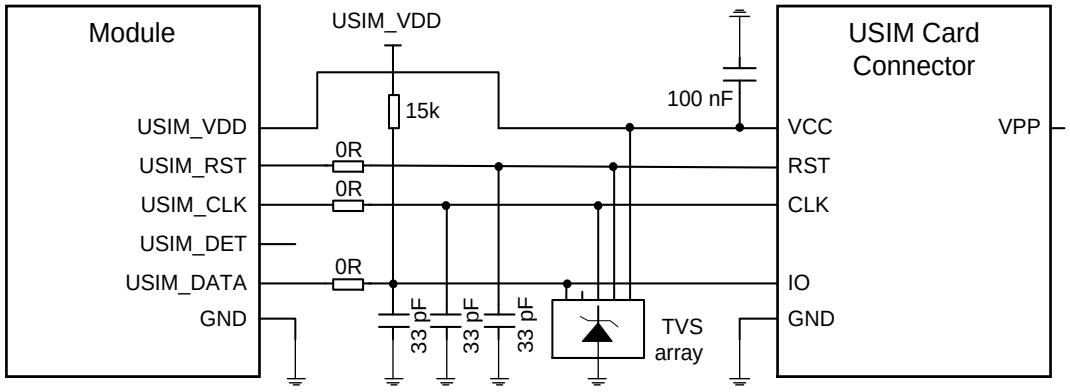


Figure 18: Reference Design of USIM Interface with a 6-pin USIM Card Connector

To enhance the reliability and availability of the USIM card in applications, follow the notes below for the USIM circuit design:

- Place USIM card connector close to the module. Keep the trace length less than 200 mm if possible.
- Keep USIM card signals away from RF and power supply traces.
- Ensure the bypass capacitor between USIM_VDD and GND is less than 1 μF, and the capacitor should be placed close to the USIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, add a TVS array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the USIM card to facilitate debugging. The 33 pF capacitors in parallel on USIM_DATA, USIM_CLK and USIM_RST traces are

used for filtering RF interference. Additionally, keep the USIM peripheral circuit close to the USIM card connector.

- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the USIM card. If the USIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the USIM card connector.

NOTE

Only USIM1 supports hot-plug function.

4.4. UART

The module provides three UART, and the auxiliary UART is multiplexed by SPI_RXD/SPI_TXD or MAIN_CTS/MAIN_RTS.

Table 18: Information of UART

UART Types	Supported Baud Rates (bps)	Default Baud Rates (bps)	Functions
Main UART	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	115200	Supports CTS and RTS hardware flow control; Data transmission
Debug UART	115200	115200	Output of partial log
Auxiliary UART	115200	115200	Communication with peripherals

Table 19: Pin Description of UART

Pin Name	Pin No.	Multiplexed Function	I/O	Description	Comment
MAIN_RXD	31	-	DI	Main UART receive	1.8 V power domain. If unused, keep them open.
MAIN_TXD	32	-	DO	Main UART transmit	
MAIN_CTS	33	-	DO	Clear to send signal from the module	1.8 V power domain. Connect to the MCU's CTS. If unused, keep it open.
MAIN_RTS	34	-	DI	Request to send signal to the	1.8 V power domain. Connect to the MCU's RTS.

				module	If unused, keep it open.
MAIN_DTR	39	-	DI	Main UART data terminal ready	1.8 V power domain. If unused, keep them open.
MAIN_RI*	40	-	DO	Main UART ring indication	
MAIN_DCD	48	-	DO	Main UART data carrier detection	
DBG_TXD	71	-	DO	Debug UART transmit	1.8 V power domain. Test points must be reserved.
DBG_RXD	72	-	DI	Debug UART receive	
SPI_RXD/ MAIN_RTS	2/34	UART3_RXD	DI	Auxiliary UART receive	1.8 V power domain. If unused, keep them open.
SPI_TXD/ MAIN_CTS	3/33	UART3_TXD	DO	Auxiliary UART transmit	

The module provides 1.8 V UART. You can use a voltage-level translator between the module and MCU's UART if the application is equipped with a 3.3 V UART. The following figure shows a reference design:

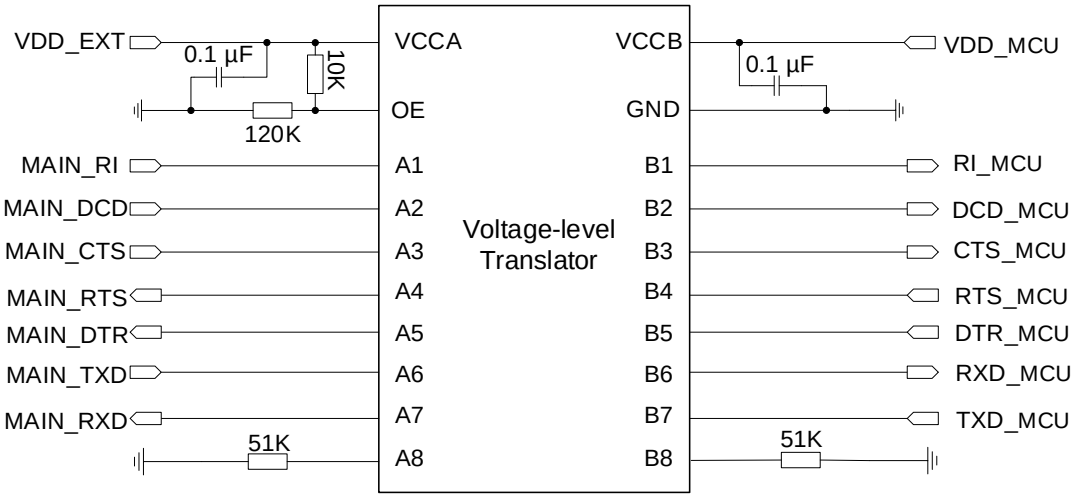


Figure 19: Reference Design of UART Interface with a Voltage-level Translator

Another example of level-shifting circuit is shown as below. Refer to the solid line for input/output circuit design in the dotted line below, but remember to follow the input/output sequence from or towards the module.

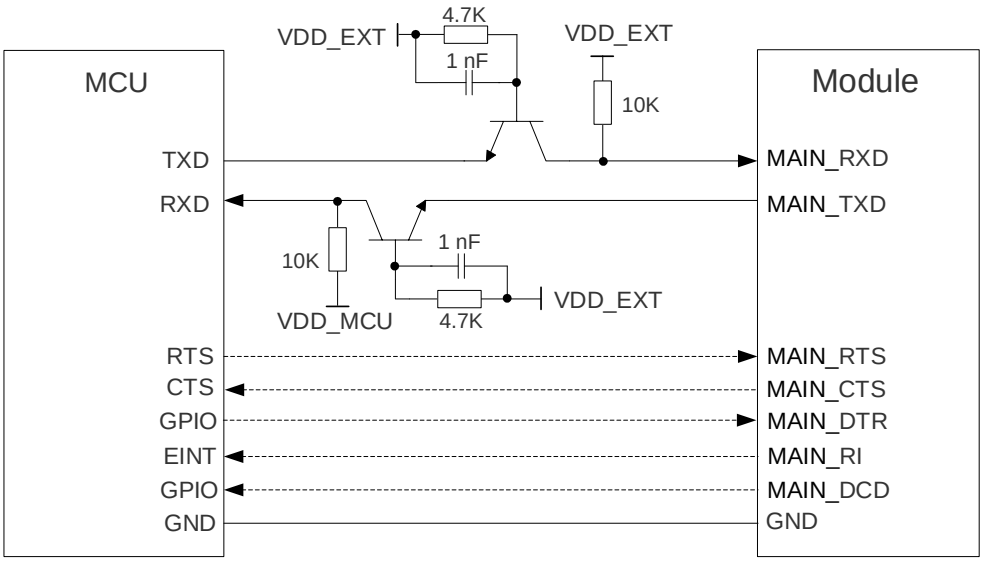


Figure 20: Reference Design of UART Interface with Transistor Circuit

NOTE

1. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
2. Transistor circuit above is not suitable for applications with baud rates exceeding 460 kbps.

4.5. PCM and I2C Interfaces

The module provides one PCM interface and one I2C interface:

Table 20: Pin Description of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	58	DO	PCM data frame sync	1.8 V power domain. If unused, keep them open.
PCM_DIN	59	DI	PCM data input	
PCM_DOUT	60	DO	PCM data output	
PCM_CLK	61	DO	PCM clock	

Table 21: Pin Description of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C_SDA	56	OD	I2C serial data	An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SCL	57	OD	I2C serial clock	

The PCM interface supports primary mode (short frame synchronization), and the module only works as a master device.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK.

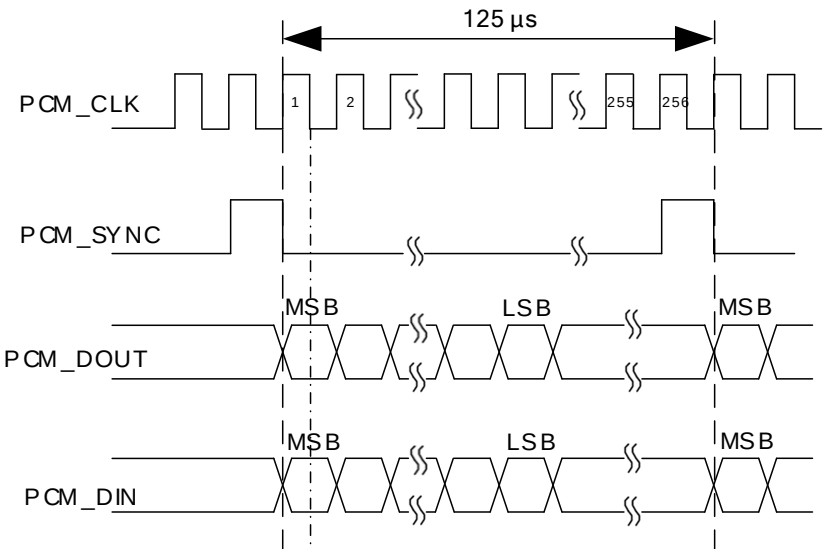


Figure 21: Timing Sequence of Primary Mode

In short frame mode, data is sampled on the falling edge of PCM_CLK, and sent on the rising edge. The falling edge of PCM_SYNC represents the high effective bit. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz, and 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

The default configuration is short frame mode, PCM_CLK = 2048 kHz, PCM_SYNC = 8 kHz.

The following figure shows a reference design of PCM interface with an external codec IC.

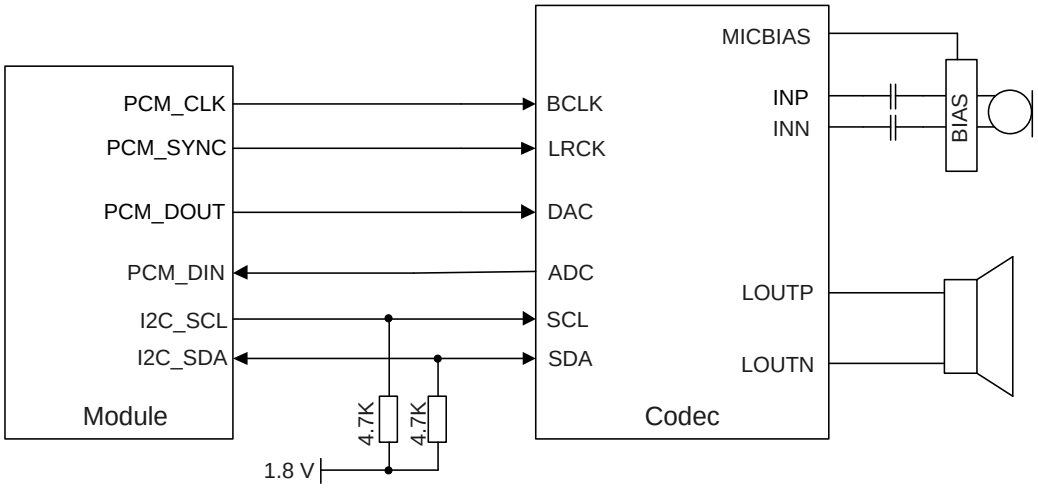


Figure 22: Reference Design of PCM and I2C Interfaces

NOTE

1. It is recommended to reserve an RC (R = 0 Ω, C = 33 pF) circuit on the PCM traces, especially for PCM_CLK.
2. The module can only be used as a master device in applications related to PCM and I2C interfaces.

4.6. LCM Interface

The module's LCD interface supports display module with a maximum resolution of 240 × 320. The module supports four-wire single data line transmission of SPI, and supports RGB565 format output.

Table 22: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_SPI_CS	65	DO	LCD SPI chip select	1.8 V power domain. If unused, keep them open.
LCD_TE	62	DI	LCD tearing effect	
LCD_SPI_CLK	67	DO	LCD SPI clock	
LCD_SPI_RS	63	DO	LCD SPI register select	
LCD_RST	64	DO	LCD reset	
LCD_SPI_DOUT	66	DO	LCD SPI data output	

4.7. SPI

The module's SPI supports slave* and master mode, the power domain of SPI is 1.8 V and a maximum clock frequency is 26 MHz.

Table 23: Pin Description of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	1	DIO	SPI clock	1.8 V power domain. When the module is used as master device, SPI_CLK and SPI_CS pins are output signals; when the module is used as slave device*, SPI_CLK and SPI_CS pins are input signals. If unused, keep them open.
SPI_RXD	2	DI	SPI data input	
SPI_TXD	3	DO	SPI data output	
SPI_CS	4	DIO	SPI chip select	

The following figure shows a reference design of SPI connected peripherals' circuit:

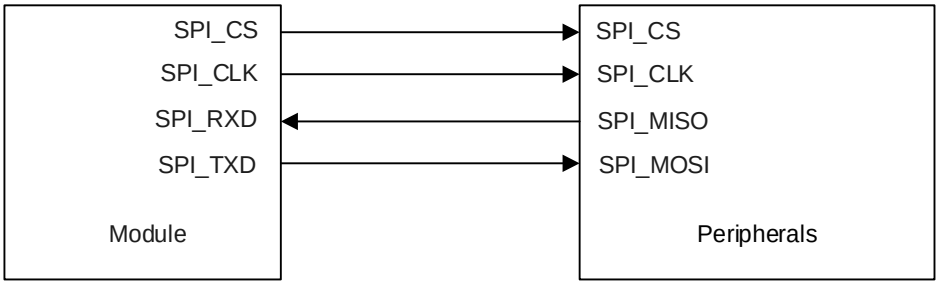


Figure 23: Reference Design of SPI Circuit (Module as Master Device)

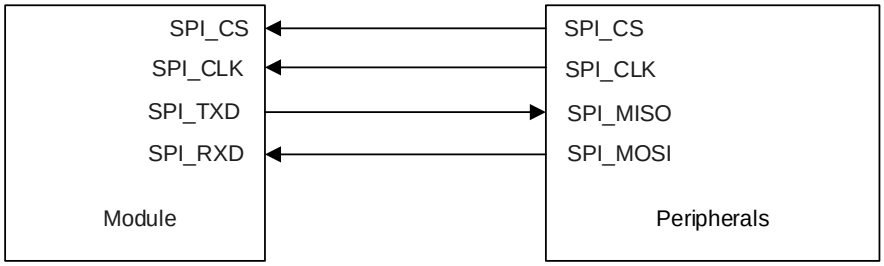


Figure 24: Reference Design of SPI Circuit (Module as Slave Device*)

NOTE

The module provides 1.8 V SPI. Use a voltage-level translator if the application is equipped with a 3.3 V system.

4.8. Matrix Keypad Interfaces

The module supports 5 × 5 matrix keypad interfaces. The matrix keyboard function can be realized by configuring the following pins. See the table below for details.

Table 24: Pin Definition of Matrix Keypad Interfaces

Pin Name	Pin No.	Multiplexing Function	I/O	Description	Comment
MAIN_DCD	48	KP_MKIN[1]	DI	matrix keypad input 1	1.8 V power domain. If unused, keep them open.
WAKEUP_IN	49	KP_MKOUT[2]	DO	matrix keypad output 1	
AP_READY	50	KP_MKIN[0]	DI	matrix keypad input 2	
W_DISABLE#	51	KP_MKOUT[0]	DO	matrix keypad output 2	
NET_MODE	52	KP_MKIN[3]	DI	matrix keypad input 3	
SLEEP_IND	53	KP_MKOUT[3]	DO	matrix keypad output 3	
STATUS	54	KP_MKIN[2]	DI	matrix keypad input 4	
NET_STATUS /USB_BOOT	55	KP_MKOUT[4]	DO	matrix keypad output 4	
I2C_SCL	57	KP_MKIN[5]	DI	matrix keypad input 5	

I2C_SDA	56	KP_MKOUT[5]	DO	matrix keypad output 5

NOTE

1. When pin 55 is multiplexed as KP_MKOUT[4], it must be pulled down to ground with a 15 kΩ resistor externally.
2. KP_MKIN and KP_MKOUT can be combined flexibly, for example, KP_MKIN[1] and KP_MKOUT[2] can be used together.
3. For more information about multiplexing, see ***document [6].***

4.9. Camera Interface

The module's camera interface supports up to 0.3 MP and supports the single data line or dual data line transmission of SPI.

Table 25: Pin Definition of Camera Interface

Pin Name	Pin No.	I/O	Description	Comment
CAM_VDD	17	PO	Camera Power supply	2.8 V/ 100 mA. If unused, keep it open.
CAM_MCLK	10	DO	Camera master clock	1.8 V power domain. If unused, keep them open.
CAM_SPI_CLK	13	DI	Camera SPI clock	
CAM_SPI_DATA0	14	DI	Camera SPI data bit 0	
CAM_SPI_DATA1	15	DI	Camera SPI data bit 1	
CAM_I2C_SCL	11	OD	Camera I2C clock	
CAM_I2C_SDA	12	OD	Camera I2C data	
CAM_PWDN	16	DO	Camera power down	
CAM_VDDIO	68	PO	Camera I/O power supply	

4.10. Analog Audio Interfaces

The module provides one analog input channel and one analog output channel.

Table 26: Pin Description of Analog Audio Interface

Pin Name	Pin No.	I/O	Description	Comment
SPK_N	21	AO	Analog audio differential output (-)	Used for earpiece interface. Class AB power amplifier, with maximum output power 37 mW @ THD = 1 %, R = 32 Ω. If the output power cannot meet the demand, this interface can be used to drive an external power amplifier device. If unused, keep them open.
SPK_P	22	AO	Analog audio differential output (+)	
MIC_N	23	AI	Microphone analog input (-)	If unused, keep them open.
MIC_P	24	AI	Microphone analog input (+)	
MIC_BIAS	25	PO	Bias voltage output for microphone	

- AIN channel is a differential input channel, which can be applied to the input from a microphone (usually an electret microphone is used).
- AOUT channel is a differential output channel, which can be applied to the output through a loudspeaker or an earpiece.
- The module's internal audio amplifier is configured as Class AB by default.

4.10.1. Audio Interface Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) to filter out RF interference, thus reducing noise. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor to filter out high-frequency noises.

The filter capacitor on the PCB should be placed as close as possible to the audio device or audio interface, and the trace should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To decrease radio or other signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.10.2. Microphone Interface Reference Design

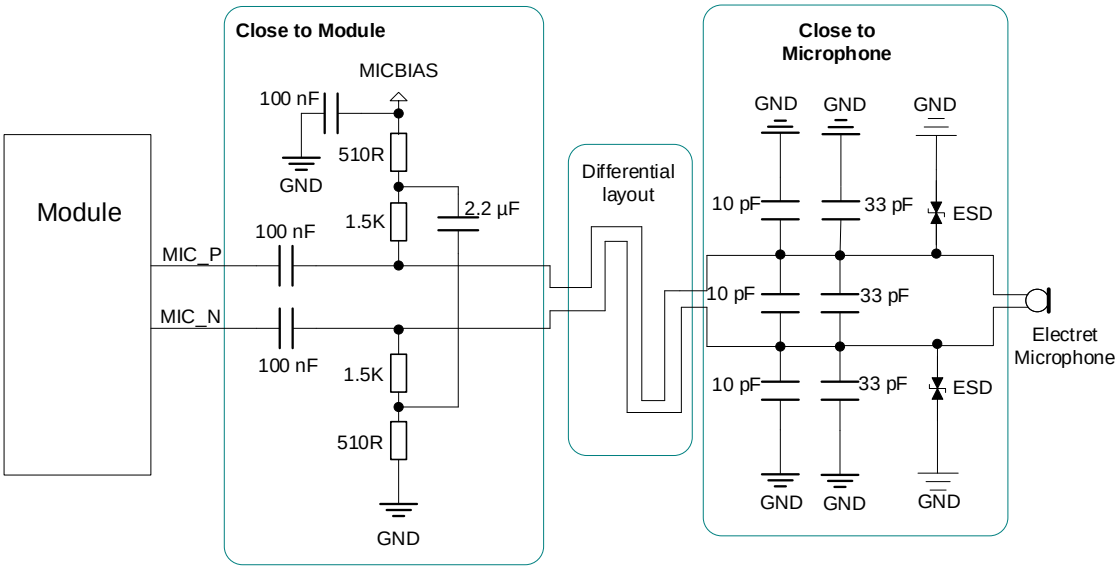


Figure 25: Reference Design of Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD protection components used to protect the MIC.

4.10.3. Earpiece and Loudspeaker Interface Reference Design

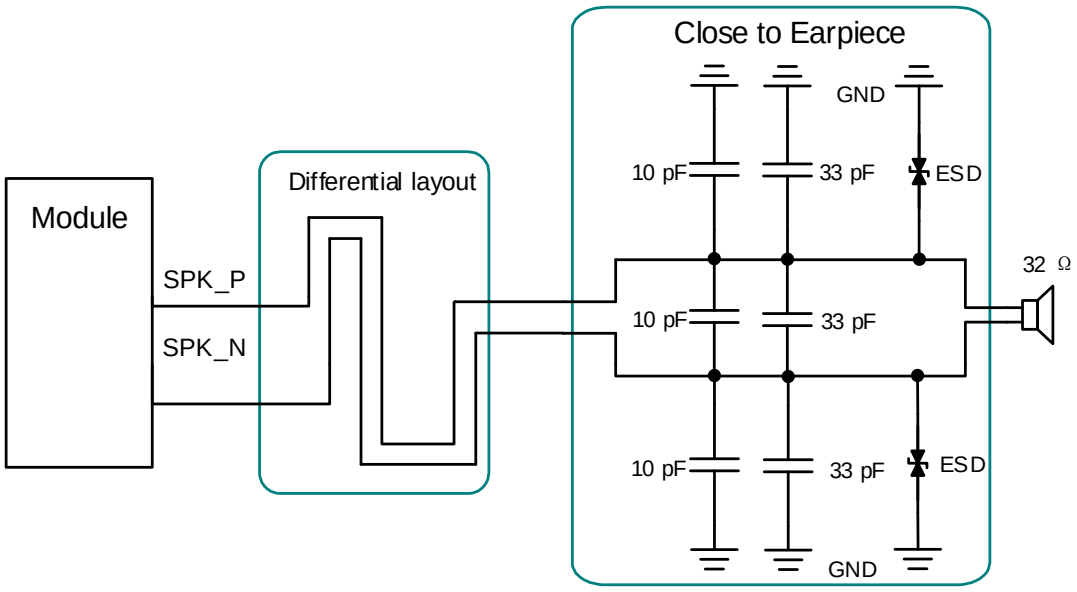


Figure 26: Reference Design of Earpiece Interface

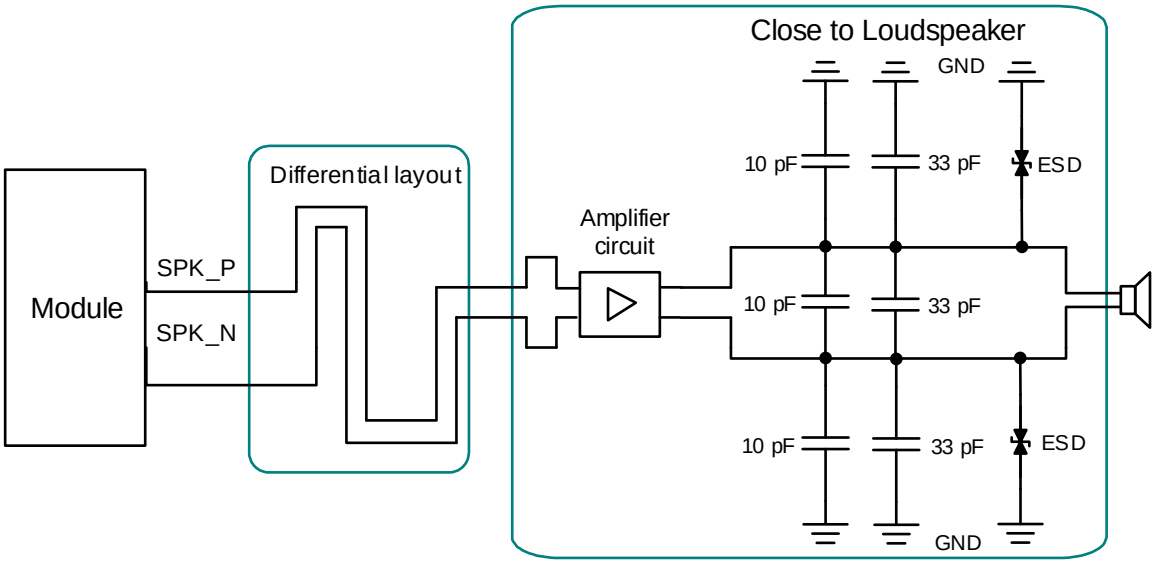


Figure 27: Reference Design of Loudspeaker Interface (external power amplifier)

If the external power amplifier is needed, see ***Figure 27***. For differential input and output audio power amplifiers, please visit http://www.ti.com/ to obtain the required devices. There are also many audio power amplifiers with the same performance to choose from the market.

4.11. ADC Interfaces

The module provides two ADC interfaces. To improve the accuracy of ADC, the trace of ADC interfaces should be surrounded by ground.

Table 27: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	19	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	20	AI		

You can use the following API to read the voltage value of ADC0 and ADC1.

Table 28: Related API of ADC Interfaces

	QuecOpen	QuecPython
API	*ql_adc_read()*	*ADC.read()*

Table 29: Characteristics of ADC Interface

Parameters	Min.	Typ.	Max.	Units
ADC0 input voltage range	0	-	1.2	V
ADC1 input voltage range	0	-	1.2	V
ADC resolution	-	12	-	bit

NOTE

1. A voltage divider with resistance of more than 100 kΩ must be used for ADC interface application.
2. The accuracy of the two resistors in each voltage divider affects the sampling error of the ADC. It is recommended to use resistors with an accuracy of 1%, if the accuracy of the ADC needs to be higher, resistors with an accuracy of 0.5% are recommended.
3. For more details about API of ADC Interfaces:
   - QuecOpen: See ***document [4]***;
   - QuecPython: Please visit https://python.quectel.com/doc/API_reference/zh/peripherals/misc.ADC.html.

4.12. Indication Signal

Table 30: Pin Description of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	52	DO	Indicate the module's network registration mode	1.8 V power domain. If unused, keep it open.
NET_STATUS/ USB_BOOT	55	DO	Indicate the module's network activity status	1.8 V power domain. After the module is turned on normally, this pin is used as a network status indicator. Do not pull down this pin before the module is powered on normally. A test point is recommended to be reserved.
STATUS	54	DO	Indicate the module's operation status	1.8 V power domain. If unused, keep it open.

4.12.1. Network Status Indication

As indication pins, NET_MODE and NET_STATUS/USB_BOOT are used to indicate the network registration status and network status of the module respectively, and drive the corresponding LED indicators at the same time.

Table 31: Working Status of Network Status Indication Pins

Pin Name	Level Status	Module Network Status
NET_MODE	High level	Registered on LTE network
	Low level	Others
NET_STATUS/ USB_BOOT	Blink slowly (200 ms high/1800 ms low)	Network searching
	Blink slowly (1800 ms high/200 ms low)	Idle
	Blink quickly (125 ms high/125 ms low)	Data transmitting
	Steady on (high level)	Voice calling

The network status indication reference circuit is shown in the figure below. It is recommended that the NET_STATUS/USB_BOOT pin is externally connected to an NMOS transistor whose maximum value of $V_{GS(TH)}$ (gate threshold voltage) does not exceed 1 V.

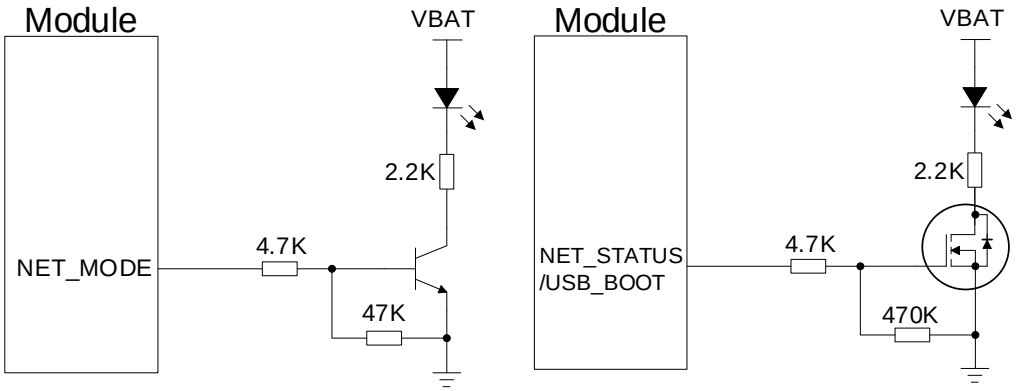


Figure 28: Reference Design of Network Status Indication

NOTE

The network indicator controlled by the NET_STATUS/USB_BOOT pin of the module is always on during the startup process. After the module is powered on normally, please refer to ***Table 31*** for the working status of the pin.

4.12.2. STATUS

STATUS indicates the module's operation status. It will output high level when module is turned on normally.

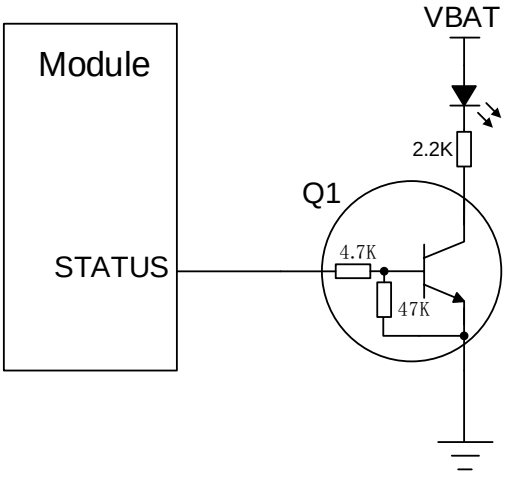


Figure 29: Reference Design of STATUS

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. LTE/Wi-Fi Scan Antenna Interface

5.1.1. Antenna Interface & Frequency Bands

Table 32: Pin Description of LTE/Wi-Fi Scan Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	46	AIO	Main antenna/Wi-Fi Scan antenna interface	50 Ω characteristic impedance.

NOTE

Wi-Fi Scan that only supports receiving, shares the same antenna interface with main antenna. The two functions cannot be used at the same time.

Table 33: EC600M-CN Operating Frequency (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B8	880–915	925–960
LTE-TDD B34	2010–2025	2010–2025

LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

Table 34: EC600M-EU Operating Frequency (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2670
LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2535–2675	2535–2675

NOTE

Band 41 only supports 140 MHz (2535–2675 MHz).

5.1.2. Antenna Tuner Control Interface

The module can use GRFC interfaces to control external antenna tuner.

Table 35: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC_1	130	DO	Generic RF controller	1.8 V power domain. If unused, keep them open.
GRFC_2	131	DO	Generic RF controller	

NOTE

EC600M-CN does not have pins 130 and 131.

Table 36: Truth Table of GRFC Interface (Unit: MHz)

GRFC_1 Level	GRFC_2 Level	Frequency Range	Bands
Low	Low	703–747.9	B28
Low	High	824–861.9	B5/B20
High	Low	880–914.9	B8
High	High	1710–2689.9	B1/B3/B7/B38/B40/B41

5.1.3. Transmitting Power

Table 37: EC600M-CN RF Transmitting Power

Frequency	Max.	Min.
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 38: EC600M-EU RF Transmitting Power

Frequency	Max.	Min.
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38/B40/B41	23 dBm ±2 dB	< -39 dBm

5.1.4. Receiver Sensitivity

Table 39: EC600M-CN Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)	
	Primary	3GPP Requirements
LTE-FDD B1 (10 MHz)	-99	-96.3
LTE-FDD B3 (10 MHz)	-99.5	-93.3
LTE-FDD B5 (10 MHz)	-99	-94.3
LTE-FDD B8 (10 MHz)	-99	-93.3
LTE-TDD B34 (10 MHz)	-100	-96.3
LTE-TDD B38 (10 MHz)	-100	-96.3
LTE-TDD B39 (10 MHz)	-100	-96.3
LTE-TDD B40 (10 MHz)	-100	-96.3
LTE-TDD B41 (10 MHz)	-99.5	-94.3

Table 40: EC600M-EU Conducted RF Receiver Sensitivity (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)	
	Primary	3GPP Requirements
LTE-FDD B1 (10 MHz)	-98.4	-96.3
LTE-FDD B3 (10 MHz)	-98.9	-93.3
LTE-FDD B5 (10 MHz)	-99.8	-94.3
LTE-FDD B7 (10 MHz)	-97.2	-94.3

LTE-FDD B8 (10 MHz)	-98.7	-93.3
LTE-FDD B20 (10 MHz)	-98.2	-93.3
LTE-FDD B28 (10 MHz)	-98.9	-94.8
LTE-TDD B38 (10 MHz)	-99.2	-96.3
LTE-TDD B40 (10 MHz)	-99.7	-96.3
LTE-TDD B41 (10 MHz)	-98.9	-94.3

5.1.5. Reference Design

Use a π-type matching circuit for all the antenna interfaces for better cellular performance. Place the π-type matching components (R1, C1, C2) as close to antennas as possible. Capacitors are not mounted by default.

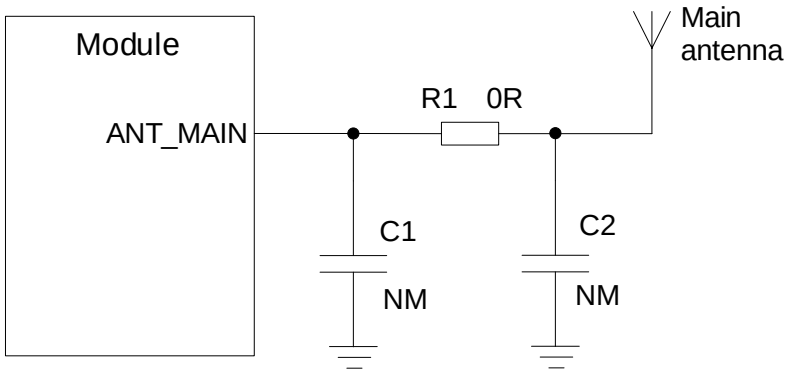


Figure 30: Reference Design of Main Antenna

5.2. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

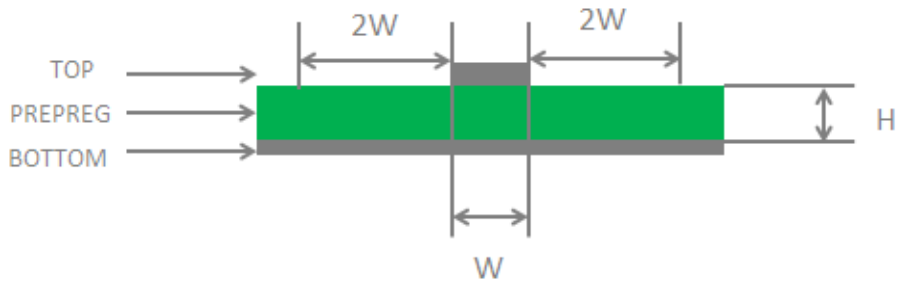


Figure 31: Microstrip Design on a 2-layer PCB

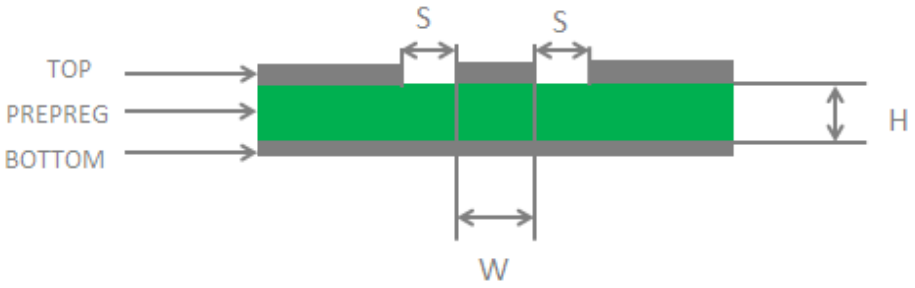


Figure 32: Coplanar Waveguide Design on a 2-layer PCB

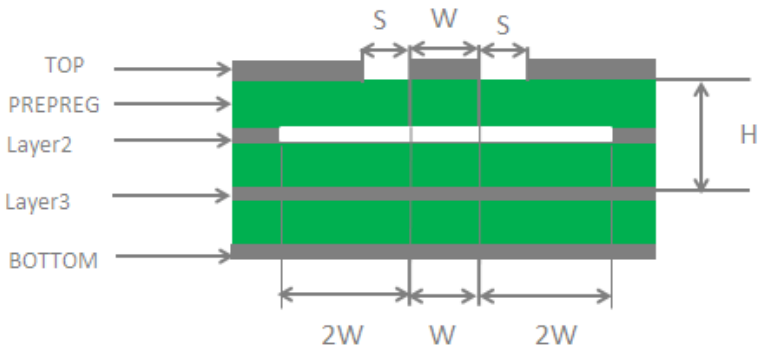


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

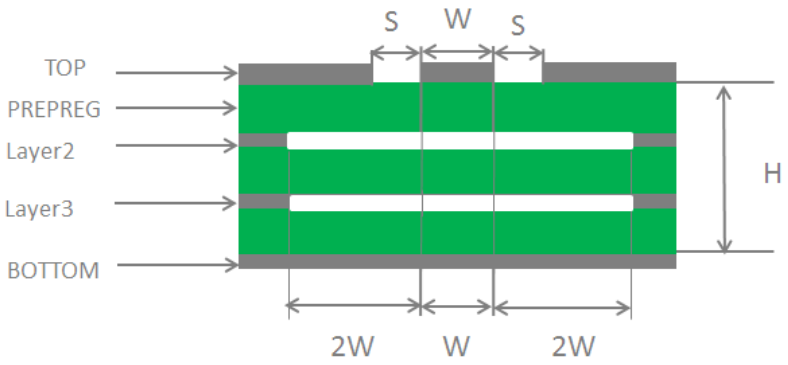


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

  For more details about RF layout, see ***document [7]***.

5.3. Requirements for Antenna Design

Table 41: Requirements for Antenna Design

Antenna Types	Requirements
Cellular	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Max input power: 50 W ● Input impedance: 50 Ω ● Vertical polarization

- Cable insertion loss:
  < 1 dB: LB (< 1 GHz)
  < 1.5 dB: MB (1–2.3 GHz)
  < 2 dB: HB (> 2.3 GHz)

5.4. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

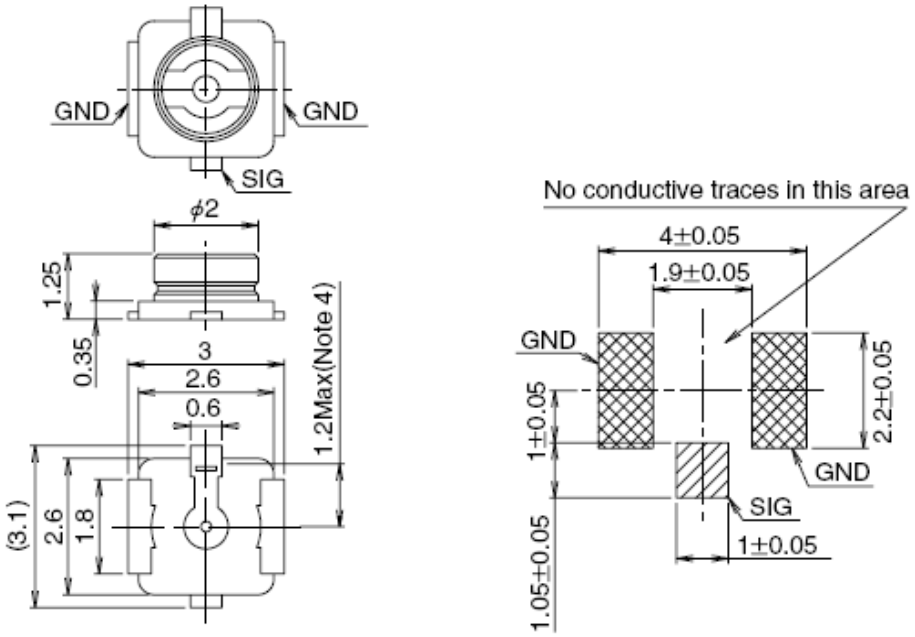


Figure 35: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

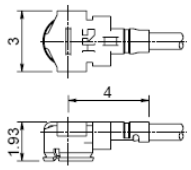
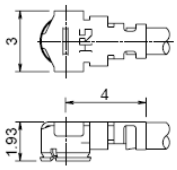
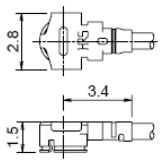
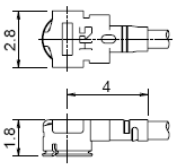
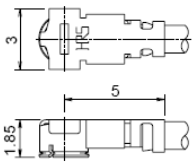
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 36: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connector.

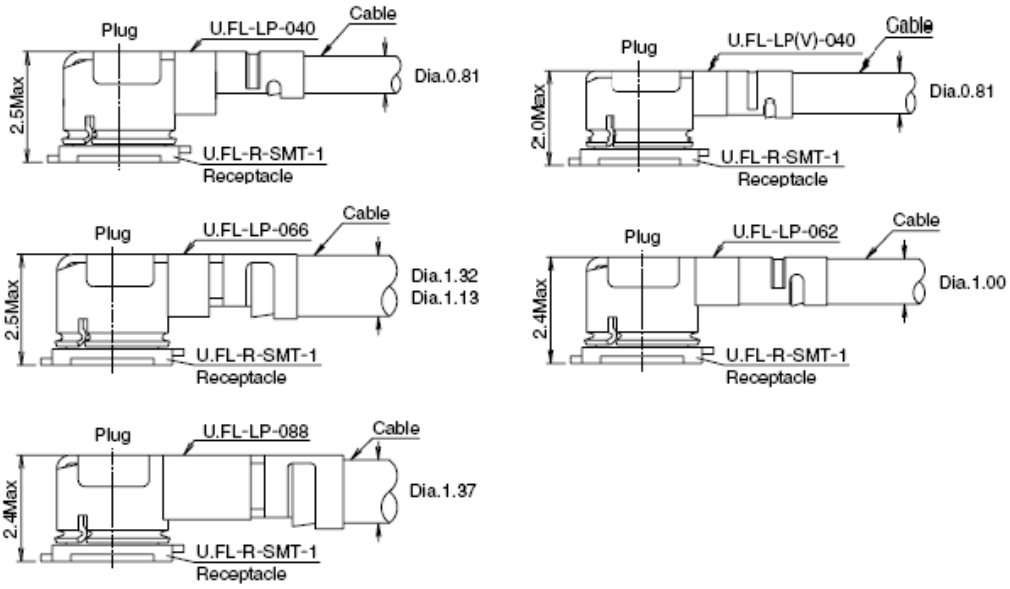


Figure 37: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Table 42: Absolute Maximum Ratings

Parameters	Min.	Max.	Unit
Voltage at VBAT_BB/VBAT_RF	-0.3	6	V
Voltage at USB_VBUS	-0.3	5.5	V
Voltage at digital pins	-0.3	2.2	V
Current at VBAT_BB	-	0.5	A
Current at VBAT_RF	-	1.5	A
Voltage at ADC [0:1]	0	1.2	V

6.2. Power Supply Ratings

Table 43: Module's Power Supply Ratings

Parameters	Descriptions	Conditions	Min.	Typ.	Max.	Units
VBAT	VBAT_BB and VBAT_RF	The actual input voltage must be within this range	3.4	3.8	4.3	V
I_{VBAT}	Peak supply consumption	At maximum power control level	-	1.5	2.0	A
USB_VBUS	USB connection detect		3.0	5.0	5.25	V

6.3. Power Consumption

Table 44: EC600M-CN Power Consumption

State	Conditions	Typ.	Units
OFF state	Power down	36	μA
Sleep state	Minimum Functionality Mode (USB disconnected)	1.04	mA
	Airplane Mode (USB disconnected)	1.18	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.10	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.57	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.35	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.25	mA
	LTE-TDD @ PF = 32 (USB disconnected)	1.98	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.56	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.34	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.24	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	17.50	mA
	LTE-FDD @ PF = 64 (USB connected)	28.90	mA
	LTE-TDD @ PF = 64 (USB disconnected)	17.52	mA
	LTE-TDD @ PF = 64 (USB connected)	28.95	mA
LTE data transmission	LTE-FDD B1	536	mA
	LTE-FDD B3	502	mA
	LTE-FDD B5	480	mA
	LTE-FDD B8	479	mA
	LTE-TDD B34	176	mA
	LTE-TDD B38	170	mA

	LTE-TDD B39	197	mA
	LTE-TDD B40	208	mA
	LTE-TDD B41	205	mA

Table 45: EC600M-EU Power Consumption

State	Conditions	Typ.	Units
OFF state	Power down	20.20	μA
Sleep state	Minimum Functionality Mode (USB disconnected)	0.98	mA
	Airplane Mode (USB disconnected)	1.03	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.90	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.46	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.23	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.12	mA
	LTE-TDD @ PF = 32 (USB disconnected)	1.90	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.46	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.23	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.13	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	17.90	mA
	LTE-FDD @ PF = 64 (USB connected)	29.71	mA
	LTE-TDD @ PF = 64 (USB disconnected)	17.92	mA
	LTE-TDD @ PF = 64 (USB connected)	29.72	mA
LTE data transfer	LTE-FDD B1	513	mA
	LTE-FDD B3	464	mA
	LTE-FDD B5	556	mA
	LTE-FDD B7	732	mA

	LTE-FDD B8	545	mA
	LTE-TDD B20	493	mA
	LTE-FDD B28	516	mA
	LTE-TDD B38	226	mA
	LTE-TDD B40	214	mA
	LTE-TDD B41	221	mA

6.4. Digital I/O Characteristics

Table 46: 1.8 V I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.	Unit
V_{IH}	Input high voltage	0.7 × VDDIO	VDDIO + 0.2	V
V_{IL}	Input low voltage	-0.3	0.3 × VDDIO	V
V_{OH}	Output high voltage	VDDIO - 0.2	-	V
V_{OL}	Output low voltage	-	0.2	V

Table 47: USIM 1.8 V I/O Characteristics

Parameters	Descriptions	Min.	Max.	Unit
USIM_VDD	Power supply	1.62	1.98	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{IL}	Input low voltage	0	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.15 × USIM_VDD	V

Table 48: USIM 3.0 V I/O Characteristics

Parameters	Descriptions	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.3	V
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{IL}	Input low voltage	0	0.15 × USIM_VDD	V
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{OL}	Output low voltage	0	0.15 × USIM_VDD	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 49: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Test Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All antenna interfaces	±4	±8	kV
Other interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 50: Operating and Storage Temperatures (Unit: °C)

Parameters	Min.	Typ.	Max.	Unit
Operating Temperature Range [4]	-35	+25	+75	°C
Extended Temperature Range [5]	-40	-	+85	°C
Storage Temperature Range	-40	-	+90	°C

[4] Within this range, the module's indicators comply with 3GPP specification requirements.

[5] Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

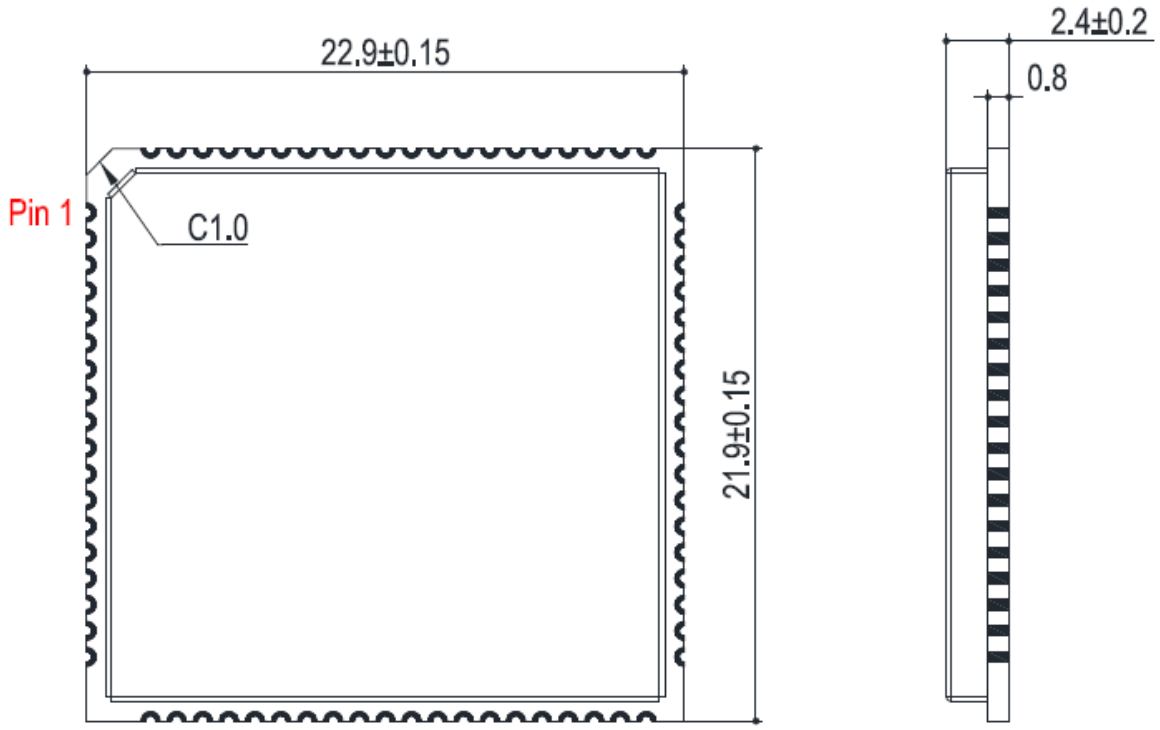


Figure 38: EC600M Series Module Top and Side Dimensions (Unit: mm)

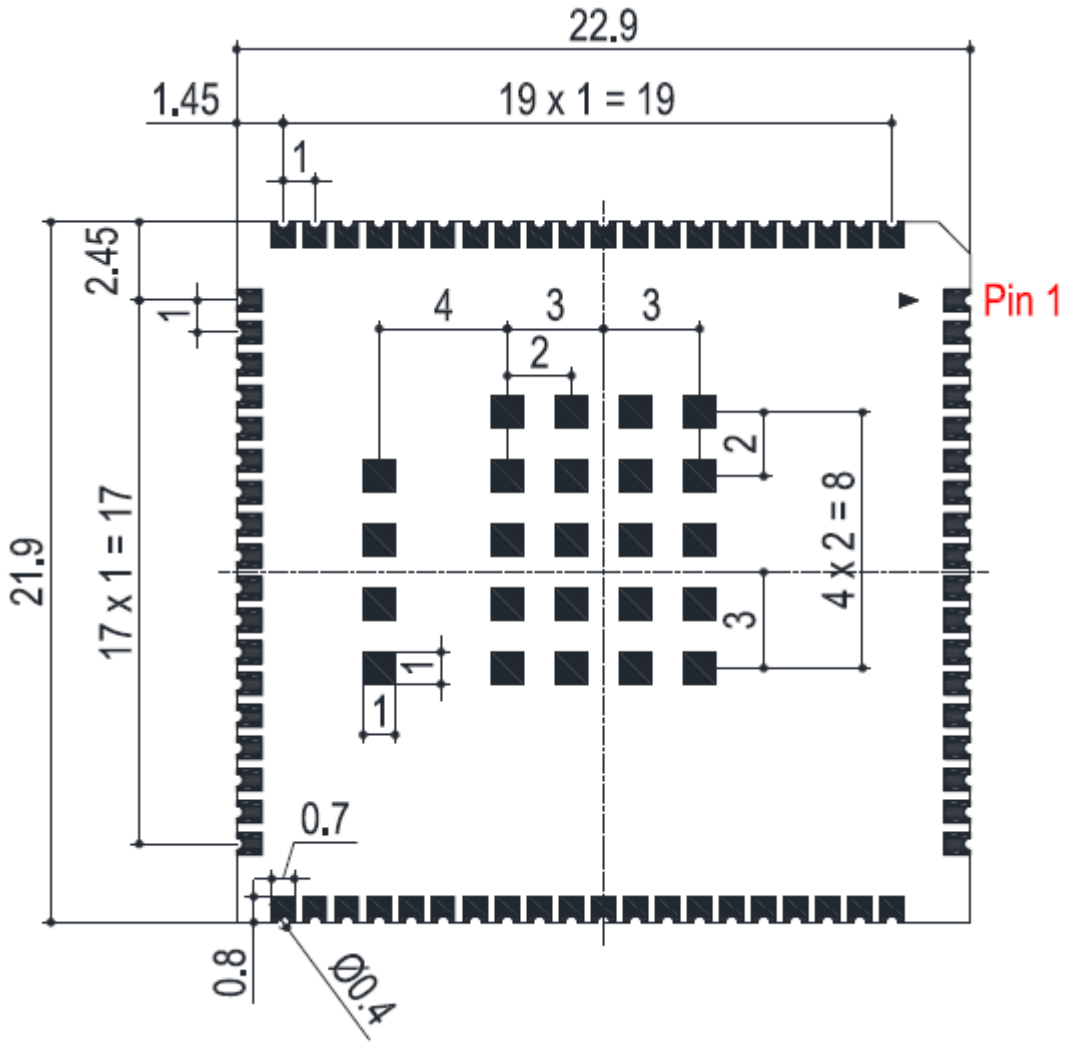


Figure 39: EC600M-CN Module Dimensions (Bottom View)

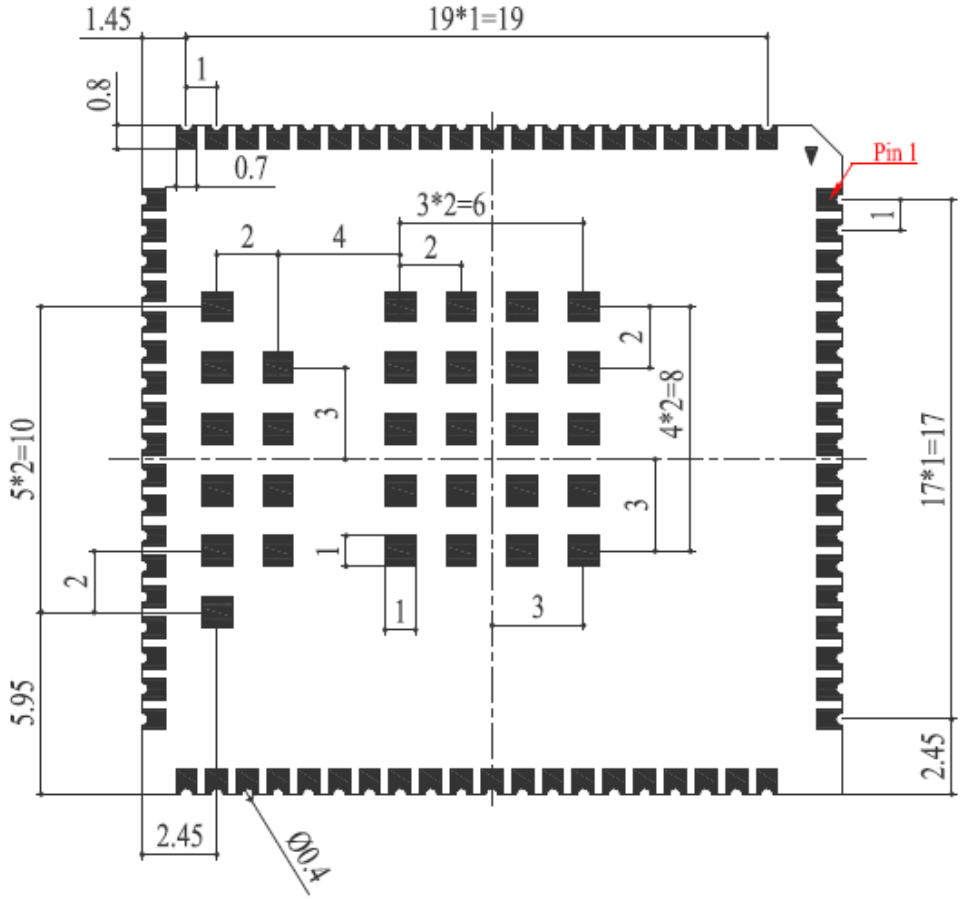


Figure 40: EC600M-EU Module Dimensions (Bottom View)

NOTE

1. The package warpage level of the module EC600M series refers to *JEITA ED-7306* standard.
2. For the stencil design of the module, see the ***document [8]***.

7.2. Recommended Footprint

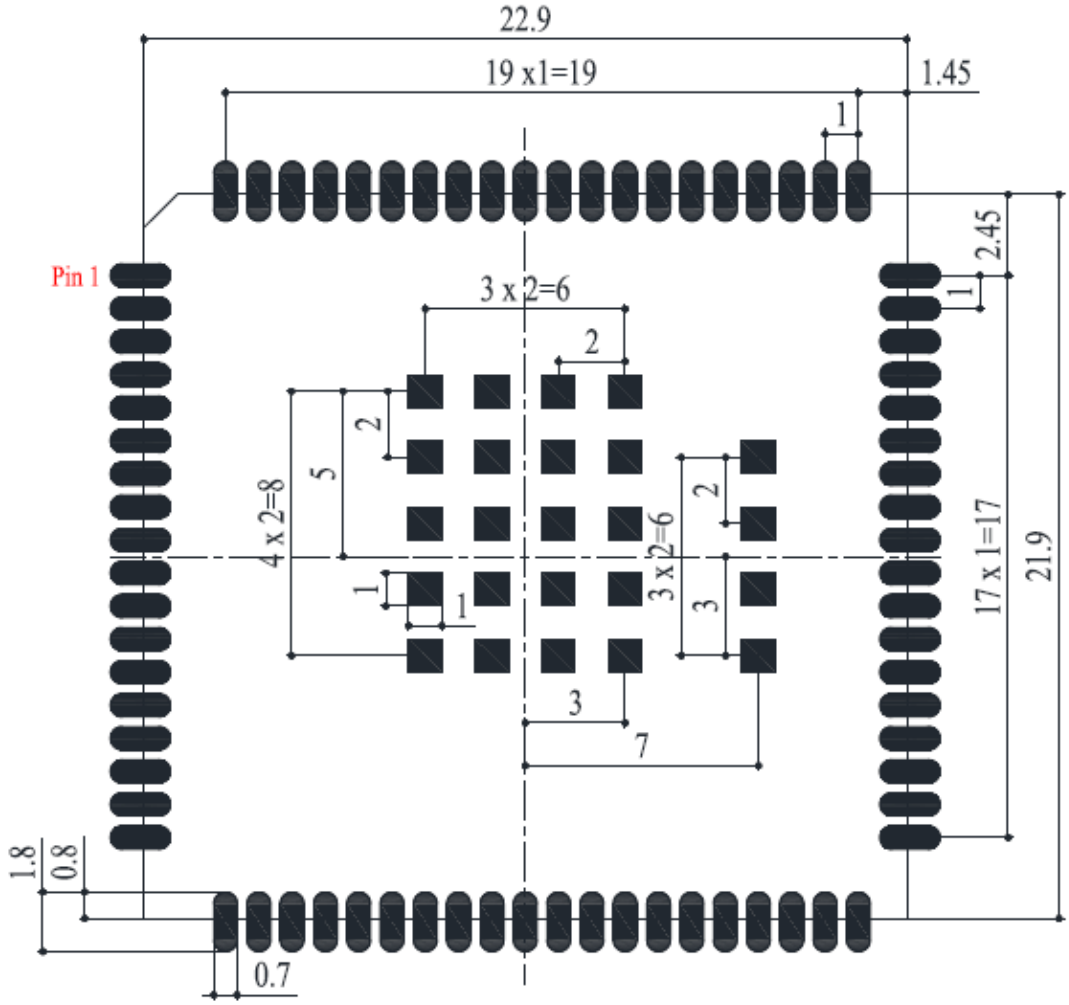


Figure 41: Recommended Footprint of EC600M-CN

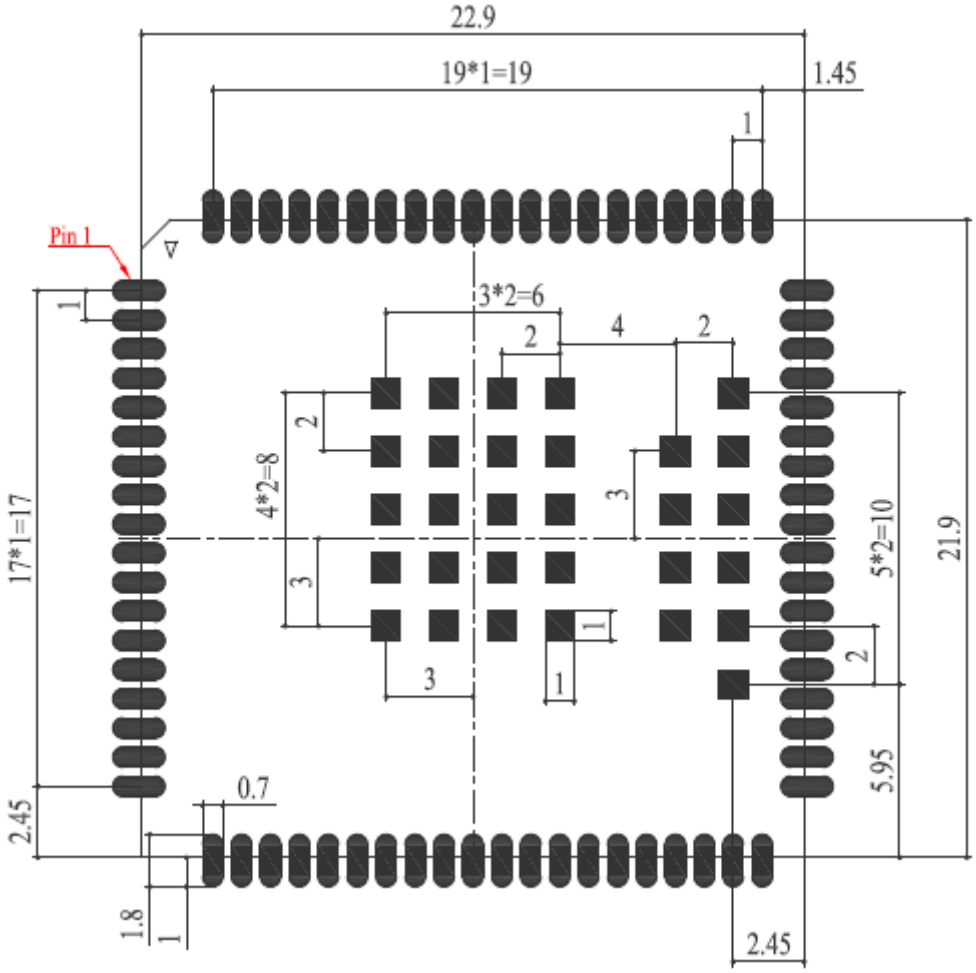


Figure 42: Recommended Footprint of EC600M-EU

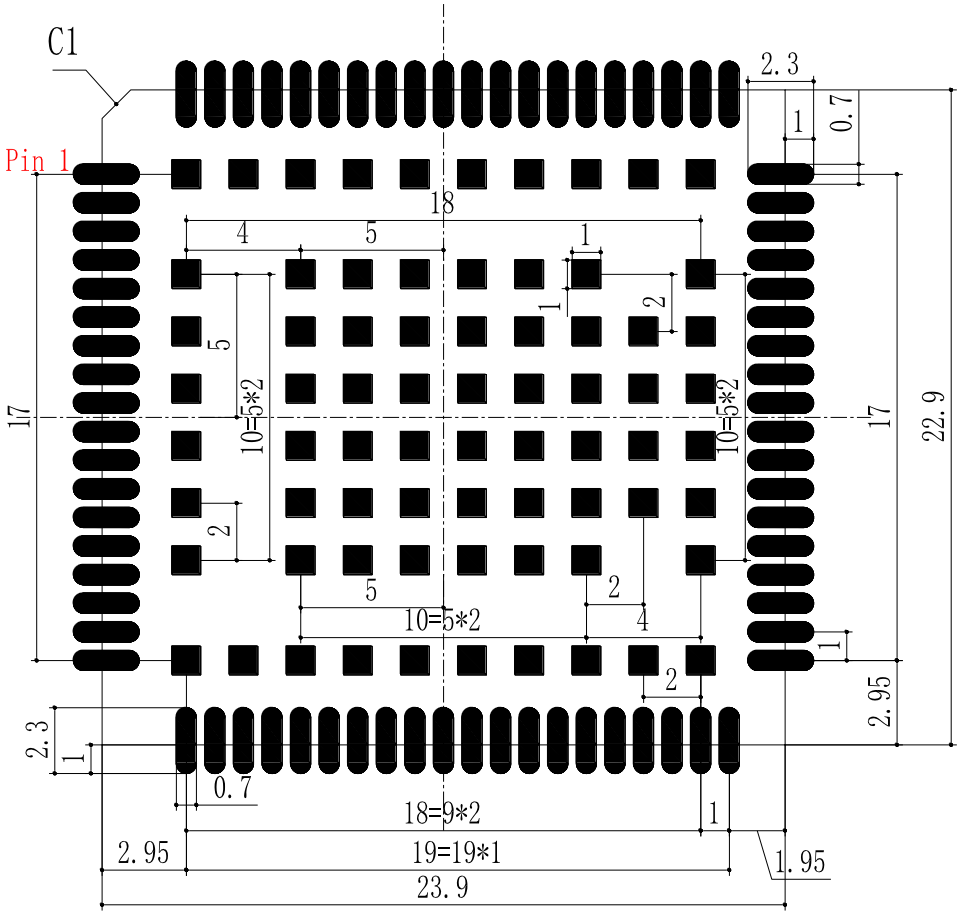


Figure 43: Recommended Compatible Footprint of EC600x Series

NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. If you consider EC600x series compatible design, please refer to the compatible footprint & part. For the stencil design of the module, see the ***document [8].***
3. For pin definitions of compatible footprint, please refer to the hardware design of the module. For details about recommended compatible footprint, see ***document [9]***.

7.3. Top and Bottom Views

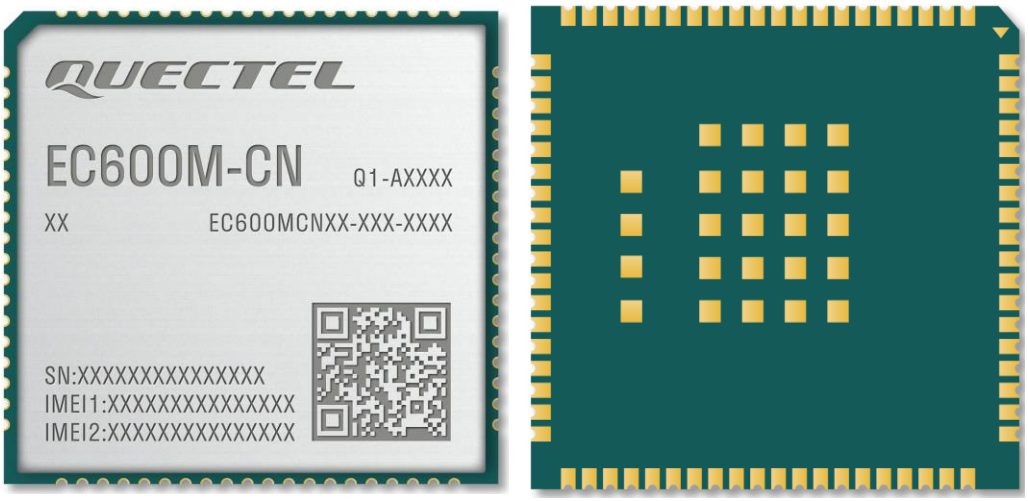


Figure 44: Top and Bottom Views of the EC600M-CN Module

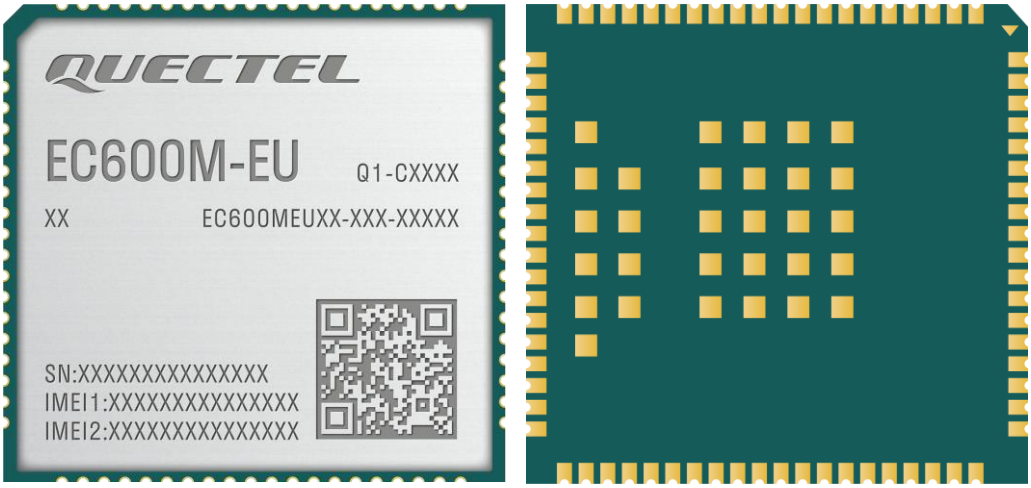


Figure 45: Top and Bottom Views of the EC600M-EU Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [6] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[6] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.20 mm. For more details, see ***document [8]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

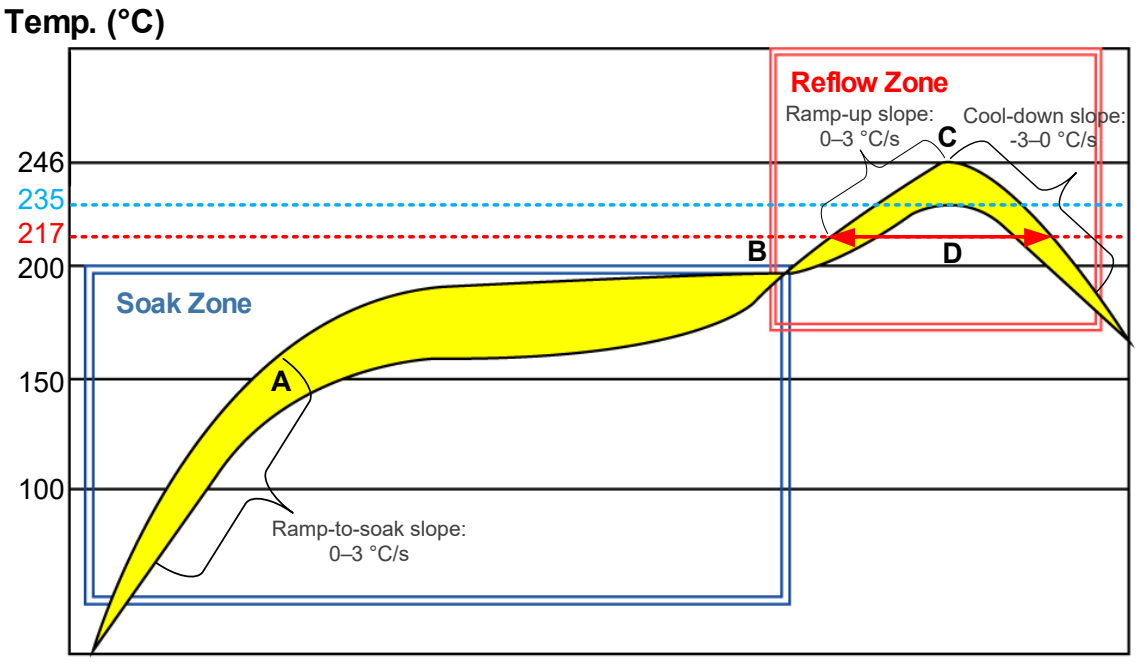


Figure 46: Recommended Reflow Soldering Thermal Profile

Table 51: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	0–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235–246 °C
Cooling down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [8]***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

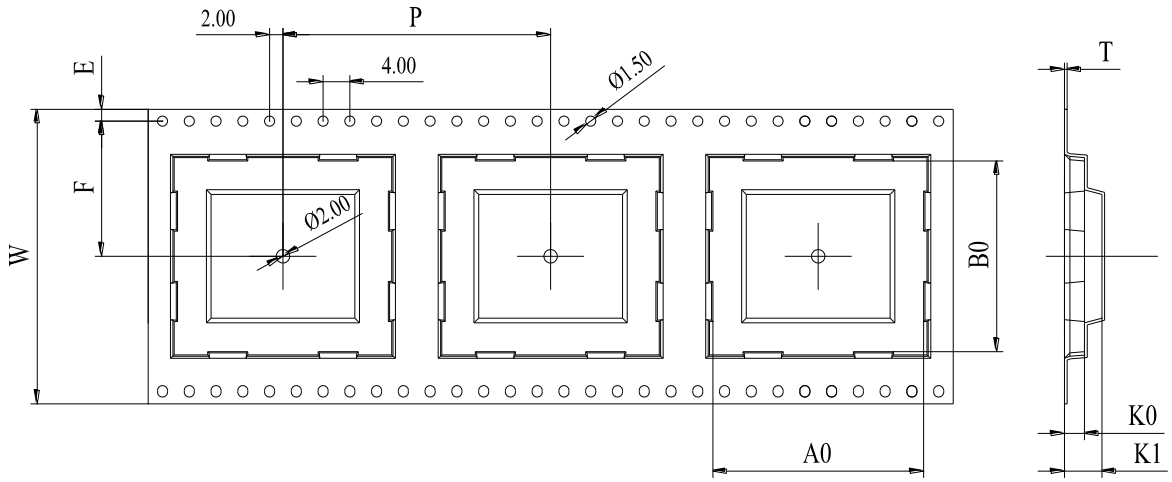


Figure 47: Carrier Tape Dimension Drawing (mm)

Table 52: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.4	23.4	22.4	2.9	6.5	20.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

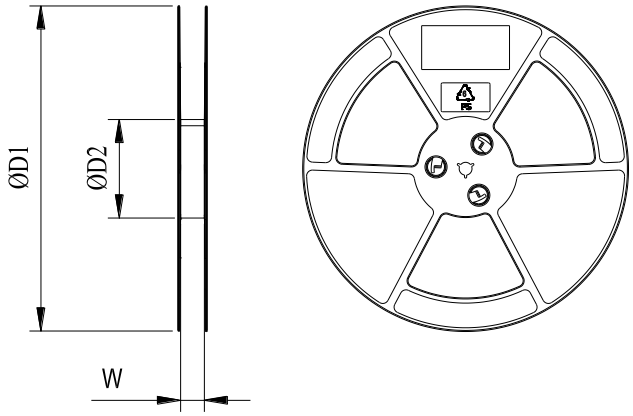


Figure 48: Plastic Reel Dimension Drawing

Table 53: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

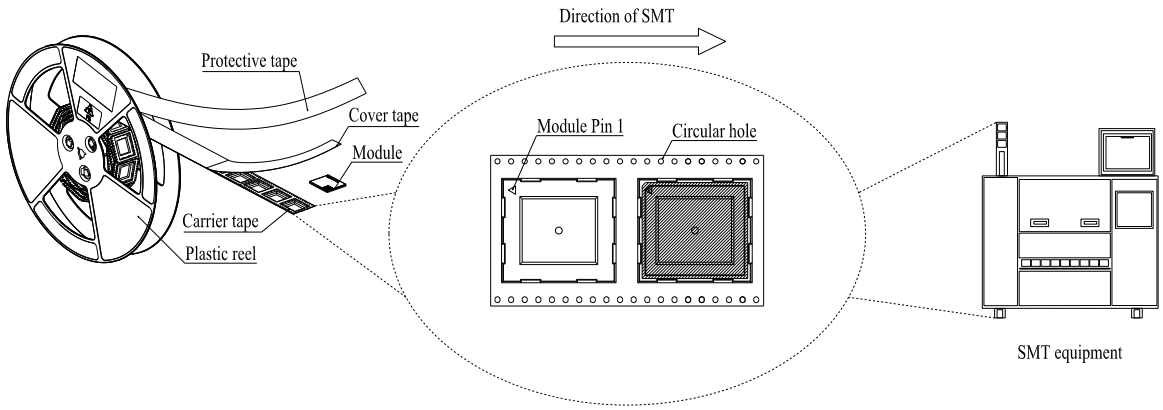
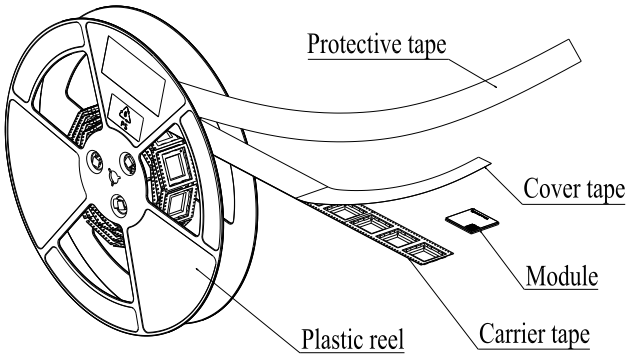


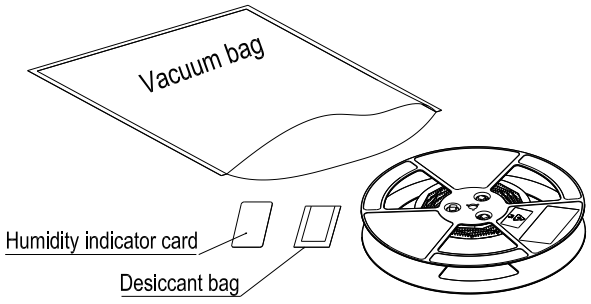
Figure 49: Mounting Direction

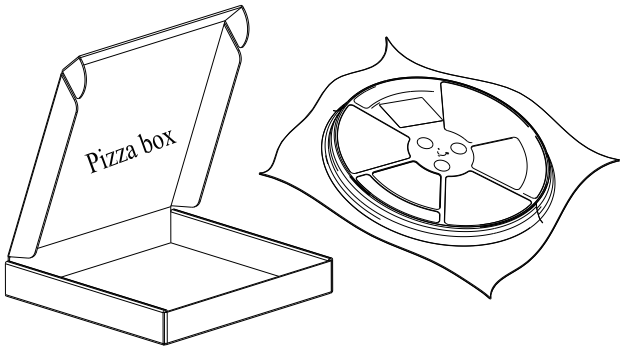
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

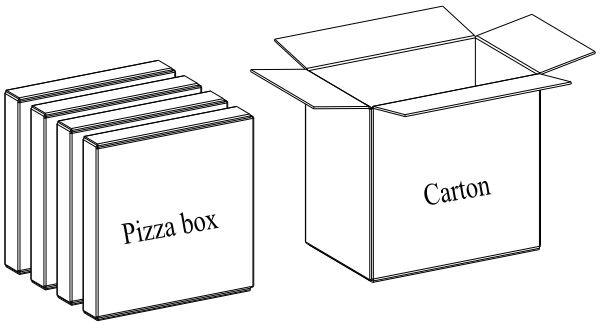


Figure 50: Packaging Process

9 Appendix References

Table 54: Related Documents

Document Name
[1] Quectel_LTE_OPEN_EVB_User_Guide
[2] Quectel_ECx00M&ECx00N_QuecOpen(SDK)_Device_Management_Guide
[3] Quectel_ ECx00M&ECx00N_QuecOpen(SDK)_Low_Power_Mode_Development_Guide
[4] Quectel_ ECx00M&ECx00N_QuecOpen(SDK)_ADC_Development_Guide
[5] Quectel_ ECx00M&ECx00N_QuecOpen(SDK)_Booting&Shutdown_Development_Guide
[6] Quectel_EC600M_Series_QuecOpen_GPIO_Configuration
[7] Quectel_RF_Layout_Application_Note
[8] Quectel_Module_SMT_Application_Note
[9] Quectel_EC600x_Series_QuecOpen_Compatible_Footprint&Part

Table 55: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
AMR	Adaptive Multi-Rate
BB	Baseband
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection MUX

CTS	Clear to Send
DFOTA	Differential Firmware Over-the-Air
DTR	Data Terminal Ready
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FDD	Frequency Division Duplex
FILE	File Protocol
FTP	File Transfer Protocol
FTPS	FTP-over-SSL
GND	Ground
GPIO	General-Purpose Input/Output
HB	High Band
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol over Secure Socket Layer
IMT-2000	International Mobile Telecommunications 2000
$I_O$max	Maximum Output Load Current
IMS	IP Multimedia Subsystem
Ipp	Peak Pulse Current
LB	Low Band
LCC	Leadless Chip Carrier (package)
LCD	Liquid Crystal Display
LCM	LCD Module

LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
M2M	Machine to machine
MB	Medium Band
Mbps	Megabits per second
MCU	Microcontroller Unit/Microprogrammed Control Unit
ME	Mobile Equipment
MIC	Microphone
MLCC	Multi-layer Ceramic Capacitor
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Levels
NITZ	Network Identity and Time Zone
NMOS	N-Metal-Oxide-Semiconductor
NTP	Network Time Protocol
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PF	Paging Frame
PING	Packet Internet Groper

PMIC	Power Management IC
PPP	Point-to-Point Protocol
PRx	Primary Receive
RAM	Random Access Memory
RGB	Red Green Blue
RF	Radio Frequency
RTS	Ready to Send/Request to Send
SIM	Subscriber Identity Module
SMS	Short Message Service
SMT	Surface Mount Technology
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SPI	Serial Peripheral Interface
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
THD	Total Harmonic Distortion
TVS	Transient Voltage Suppressor
Tx	Transmit/Transmission
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
UMTS	Universal Mobile Telecommunications System
USIM	(Universal) Subscriber Identity Module

V_{IL}max	Maximum Low-level Input Voltage
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
VBAT	Voltage at Battery (Pin)
V_{RWM}	Working Peak Reverse Voltage
VSWR	Voltage Standing Wave Ratio