EC200U Series QuecOpen Reference Design

LTE Standard Module Series

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At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

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About the Document

Revision History

Version	Date	Author	Description
-	2021-08-16	Kyle CHEN	Creation of the document
1.0	2021-08-24	Kyle CHEN	First official release
1.1	2022-12-08	Denny QIN	1. Deleted the MAIN_DTR, MAIN_RI, MAIN_DCD, WAKEUP_IN, AP_READY, W_DISABLE#, SLEEP_IND pin functions and related content. 2. Pin names have been updated: a) Pin 38: from SPI_MOSI to SPI_DOUT b) Pin 39: from SPI_MISO to SPI_DIN (Sheet 3). 3. Added ADC voltage divider circuit and updated NOTE 4 (Sheet 3). 4. Added NOTE 7 & 8 for TVS and GPIO pins (Sheet 3). 5. Added NOTE 5 for R0207 resistance value (Sheet4). 6. Updated NOTE 3 for ESD of audio circuits (Sheet 9). 7. Changed the resistance value of R0904–R0908 from 100 kΩ to 4.7 kΩ and R0910 from 0 Ω to 33 Ω for SD card circuit (Sheet 11). 8. Added the design for LCM MIPI (Sheet 12). 9. Added the design for camera MIPI (Sheet 13). 10. Added NOTE 4 for FLASH signal cable(Sheet 16).

Contents

1 Reference Design

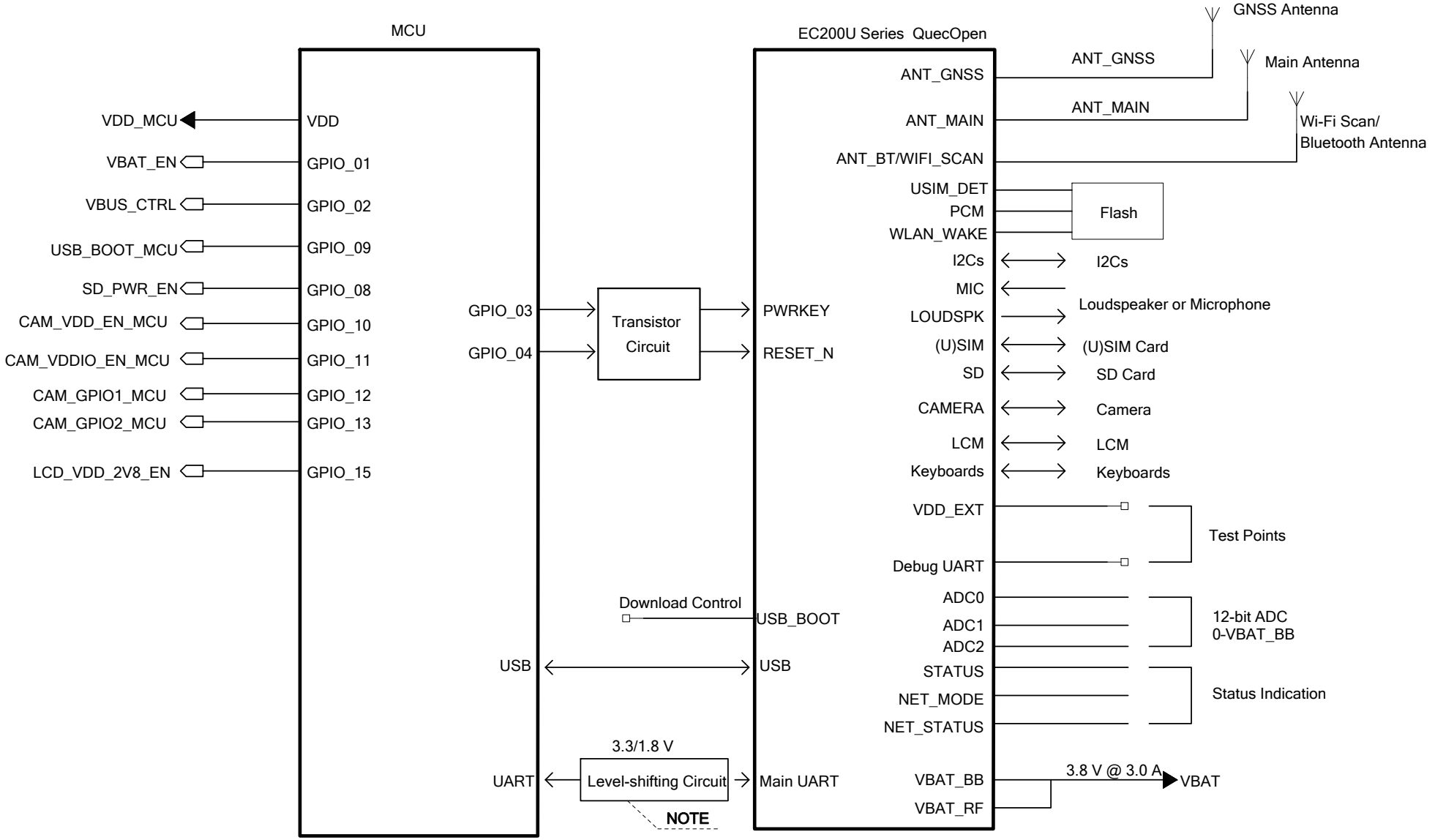
1.1. Introduction

This document provides the reference design for Quectel EC200U series QuecOpen® module, including block diagram, module interface, MCU interface, power supply design, antenna interface, (U)SIM interface, analog audio, UART interface, SD card interface, LCM, camera, matrix keyboard, flash interface, USB_BOOT download interface and other designs.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



NOTE:

It is recommended to use a level-shifting circuit or a voltage level translator TXS0108EPWR provided by Texas Instruments.

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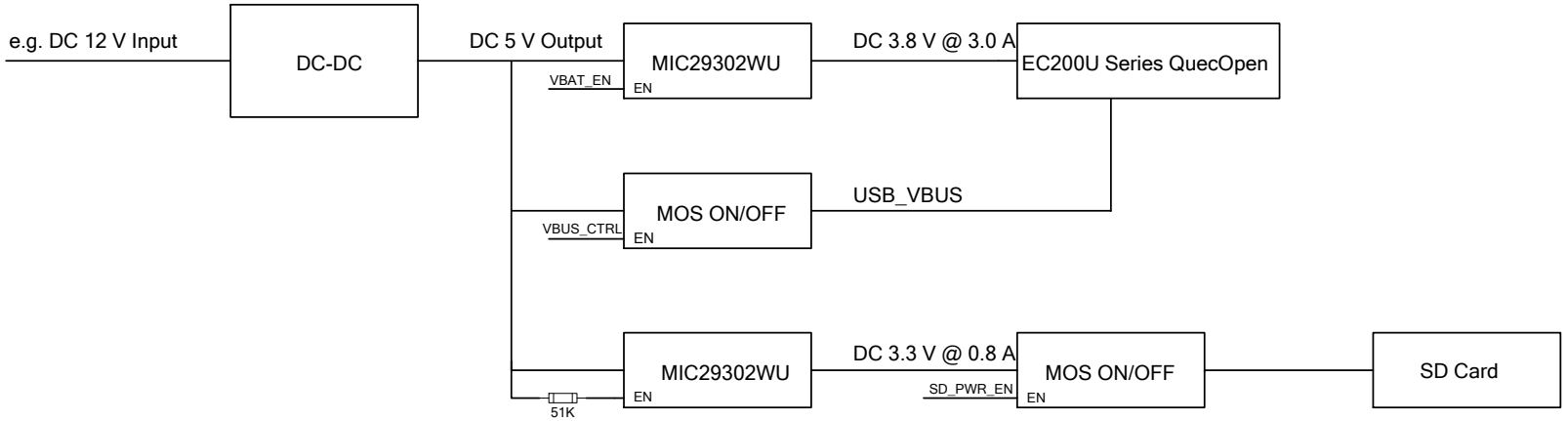
Power Supply Block Diagram



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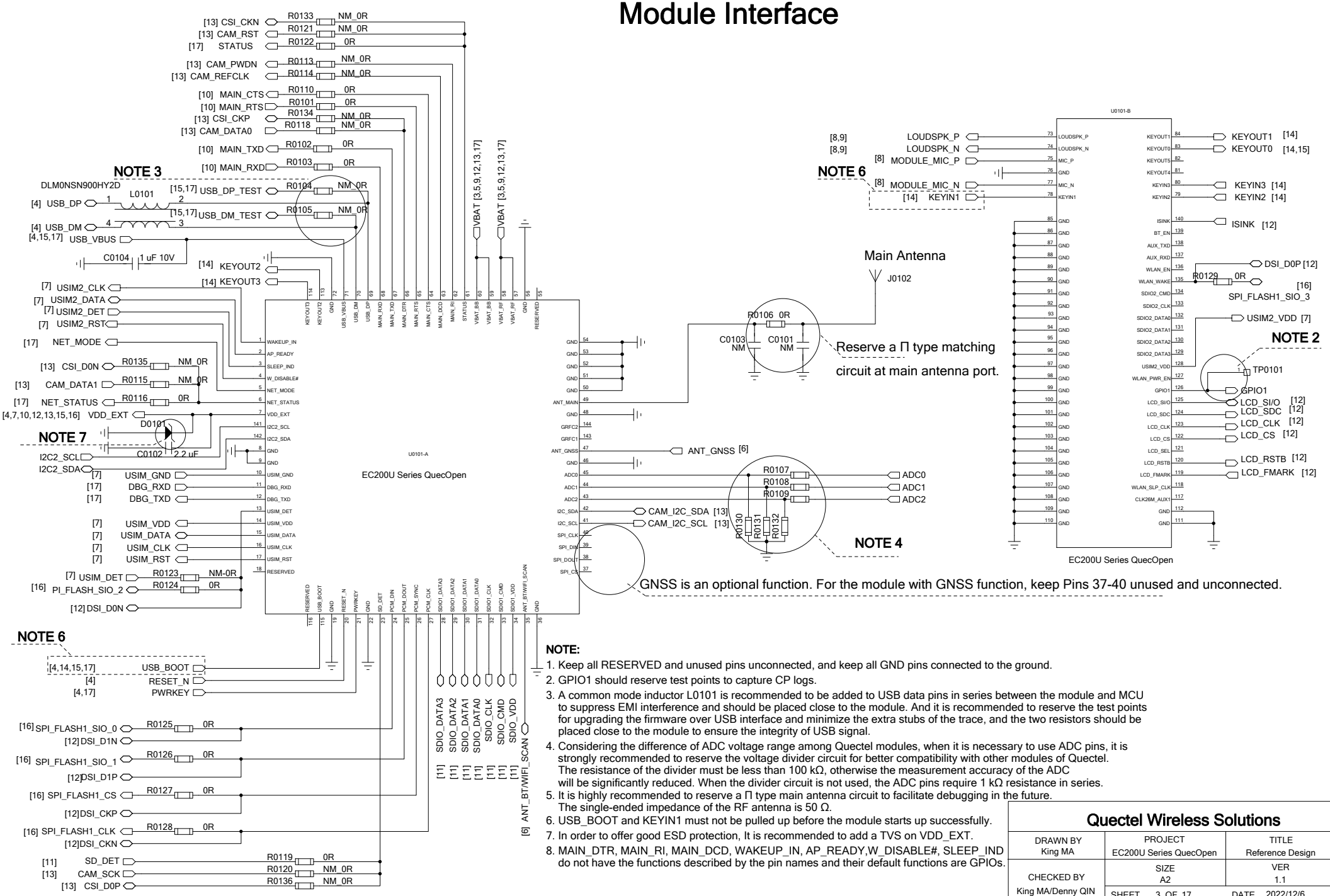
Module Interface



NOTE:

1. Keep all RESERVED and unused pins unconnected, and keep all GND pins connected to the ground.
2. GPIO1 should reserve test points to capture CP logs.
3. A common mode inductor L0101 is recommended to be added to USB data pins in series between the module and MCU to suppress EMI interference and should be placed close to the module. And it is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the extra stubs of the trace, and the two resistors should be placed close to the module to ensure the integrity of USB signal.
4. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins, it is strongly recommended to reserve the voltage divider circuit for better compatibility with other modules of Quectel. The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced. When the divider circuit is not used, the ADC pins require 1 kΩ resistance in series.
5. It is highly recommended to reserve a Π type main antenna circuit to facilitate debugging in the future. The single-ended impedance of the RF antenna is 50 Ω.
6. USB_BOOT and KEYIN1 must not be pulled up before the module starts up successfully.
7. In order to offer good ESD protection, It is recommended to add a TVS on VDD_EXT.
8. MAIN_DTR, MAIN_RI, MAIN_DCD, WAKEUP_IN, AP_READY,W_DISABLE#, SLEEP_IND do not have the functions described by the pin names and their default functions are GPIOs.

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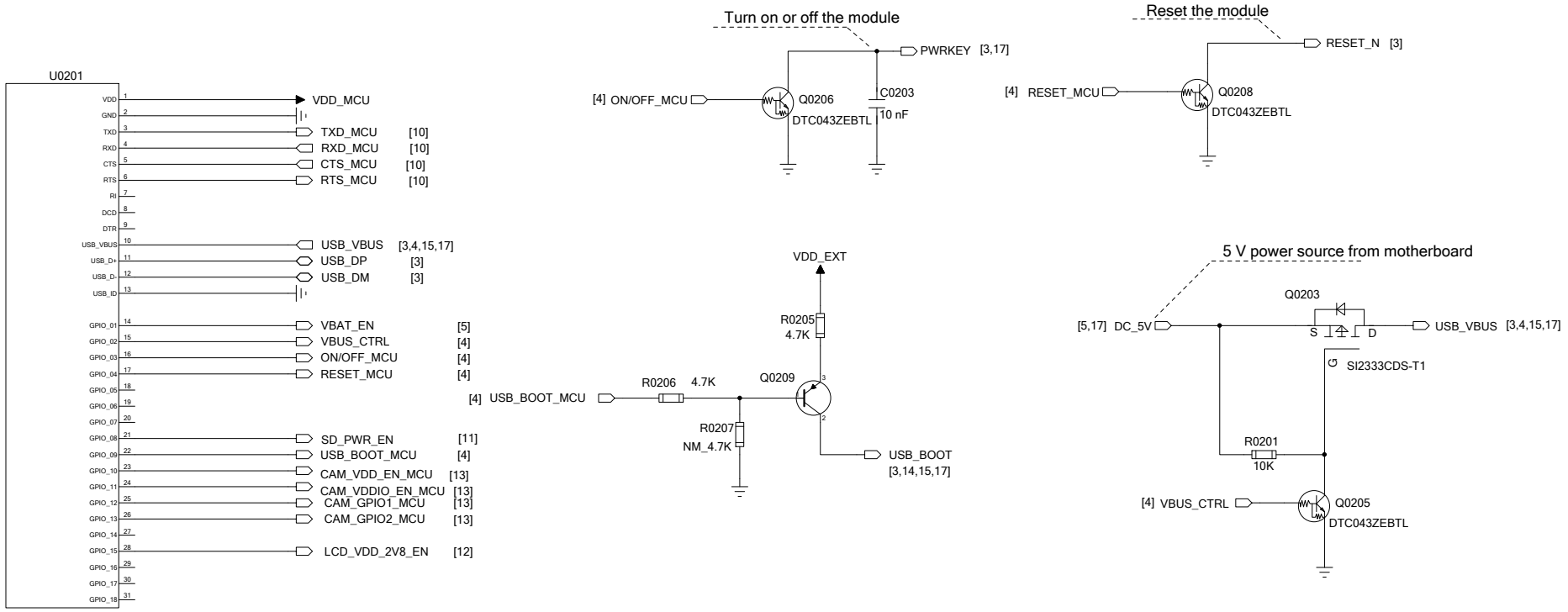
MCU Interface



NOTE:

1. U0201 represents your MCU. The power domain of GPIO interfaces of EC200U series QuecOpen is 1.8 V; if the GPIO interfaces of U0201 share the same power domain, then the related level-shifting circuit can be omitted.
2. The USB interface of EC200U series QuecOpen can only serves as a slave device and supports full-speed and high-speed modes of USB 2.0. To communicate with the USB interface, MCU needs to support USB host or OTG function. The USB_VBUS pin of the module should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the default low-level GPIO pins of MCU as the control pins for PWRKEY and RESET_N of the module. Please ensure that there is no capacitance with the maximum value exceeding 10 nF on PWRKEY and RESET_N pins.
4. The USB_BOOT_MCU pin is at high level by default when the MCU is powered on to prevent the MCU from powering on the transistor Q0209 to conduct the module in the download mode. Transistor or reserving through-hole or keys can be applied to avoid such situation.
5. The resistance value of R0207 is selected according to the level of the USB_BOOT_MCU pin.

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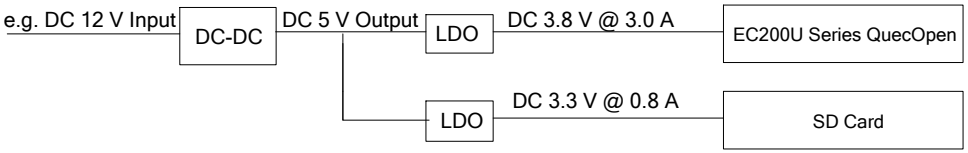
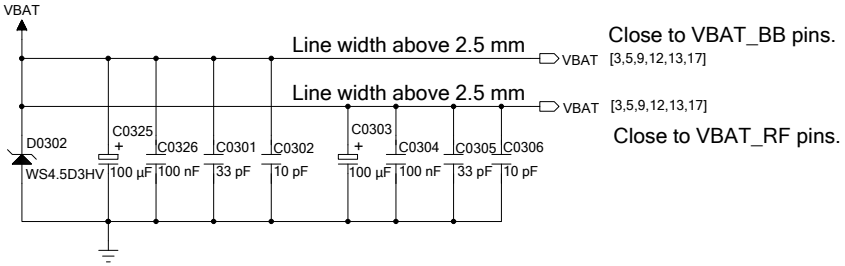
Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert a high input voltage into a 5.0 V first, and then respectively convert to 3.8 V and 3.3 V typical voltages by LDOs.



VBAT Design

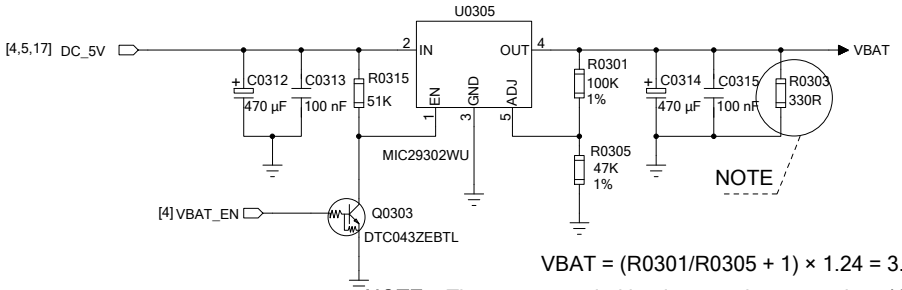


NOTE:

1. VBAT current should meet the rated output capacity of 3.0 A. If you select the module that does not support the GSM frequency band, you can select a power supply with a current capability of 2.0 A.
2. VBAT_BB and VBAT_RF pins should be divided into two separated paths in star structure.
3. The recommended operating voltage of VBAT is 3.3-4.3 V.

LDO Application

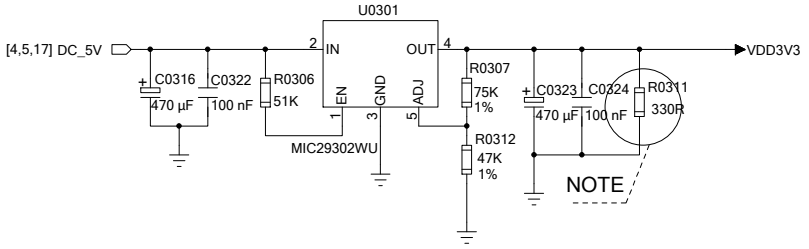
When the input voltage is below 7.0 V, convert to 3.8 V power supply for the module by LDO.



VBAT = (R0301/R0305 + 1) × 1.24 = 3.88 V

NOTE: The recommended load current is greater than 10 mA.

Power Supply for SD Card



VDD3V3 = (R0307/R0312 + 1) × 1.24 = 3.3 V

NOTE: The recommended load current is greater than 10 mA.

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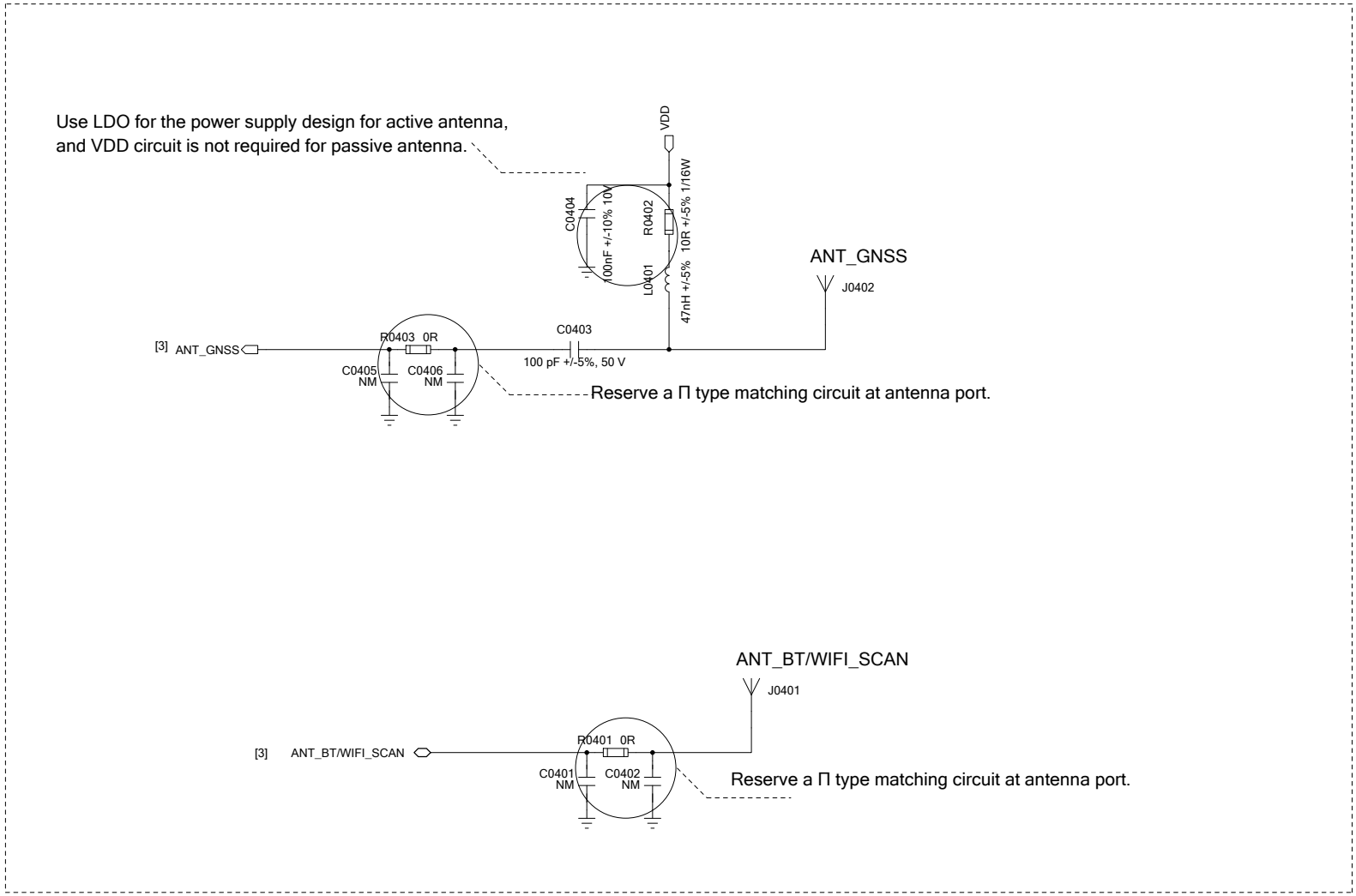
Antenna Interface



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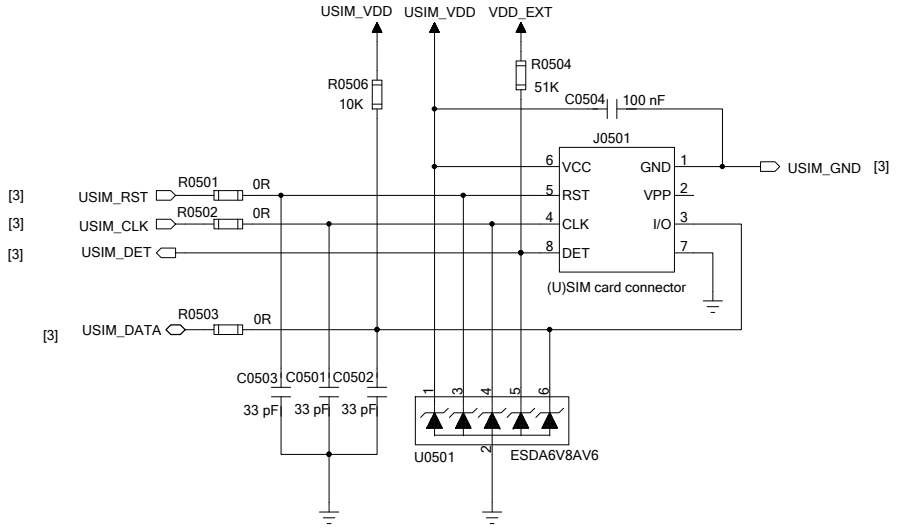
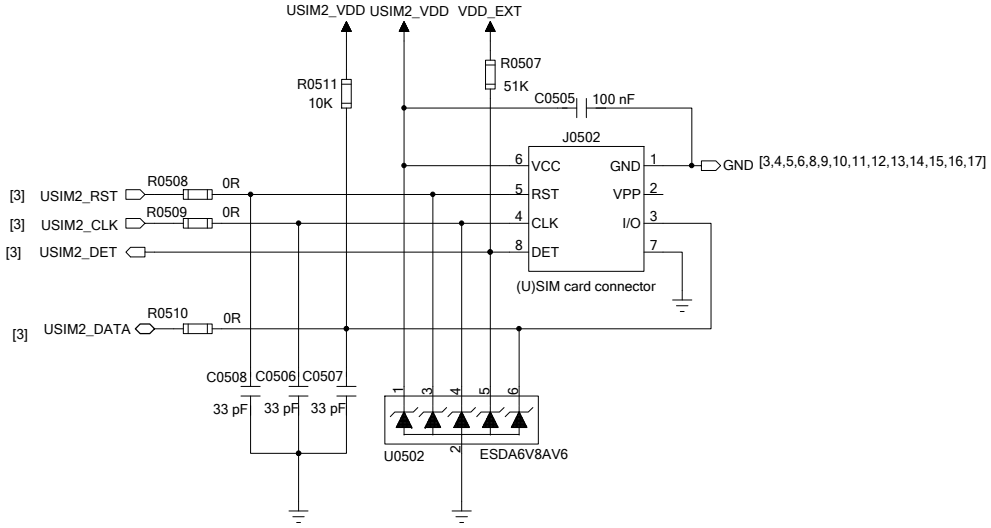
(U)SIM Interface Design

(U)SIM1



(U)SIM2



NOTE:

1. U0501 and U0502 are recommended to be used to offer good ESD protection, and the parasitic capacitance should not be more than 15 pF.
2. The GND of the (U)SIM card connector is recommended to be connected to the module's USIM_GND to avoid being interfered by the ground of (U)SIM card connector, and also can be connected to the ground of PCB if your PCB has a complete ground plane.
3. The pull-up resistors R0506 and R0511 can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.
4. R0501-R0503 and R0508-R0510 are used for debugging, and C0501-C0503 and C0506-C0508 are used for filtering out EGSM900 interference.
5. The capacitances of C0504 and C0505 should be less than 1 μF and the two capacitors should be placed close to the (U)SIM card connector.
6. For more information about the layout of (U)SIM interface, please refer to *Quectel_EC200U Series QuecOpen_Hardware_Design.*

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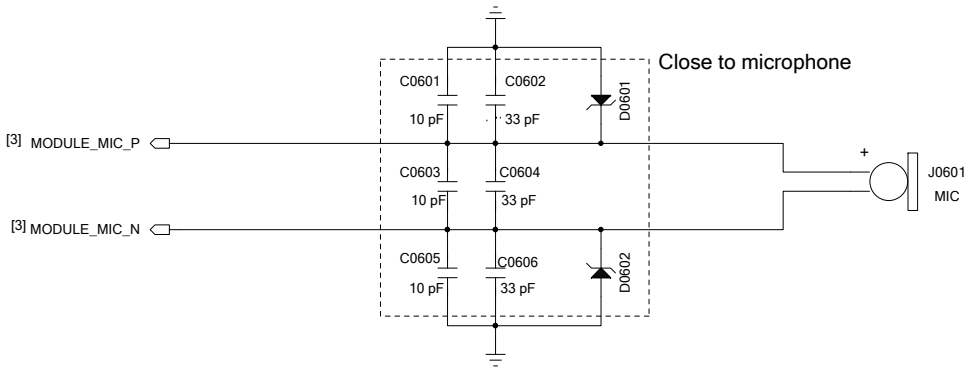
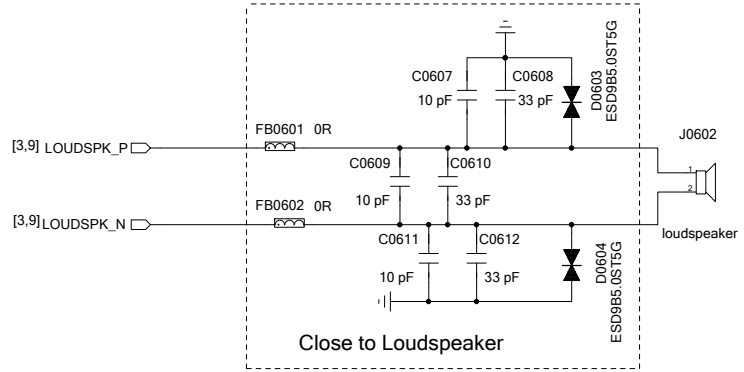
Analog Audio Design

Microphone Application



Loudspeaker Interface



NOTE:

1. Both the MIC and SPK signal traces need to be routed as differential pairs.
2. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noises.
3. The loudspeaker has a built-in power amplifier with a default configuration of Class AB. And the output power of such power amplifier is 500 mW for Class AB and 800 mW for Class D.

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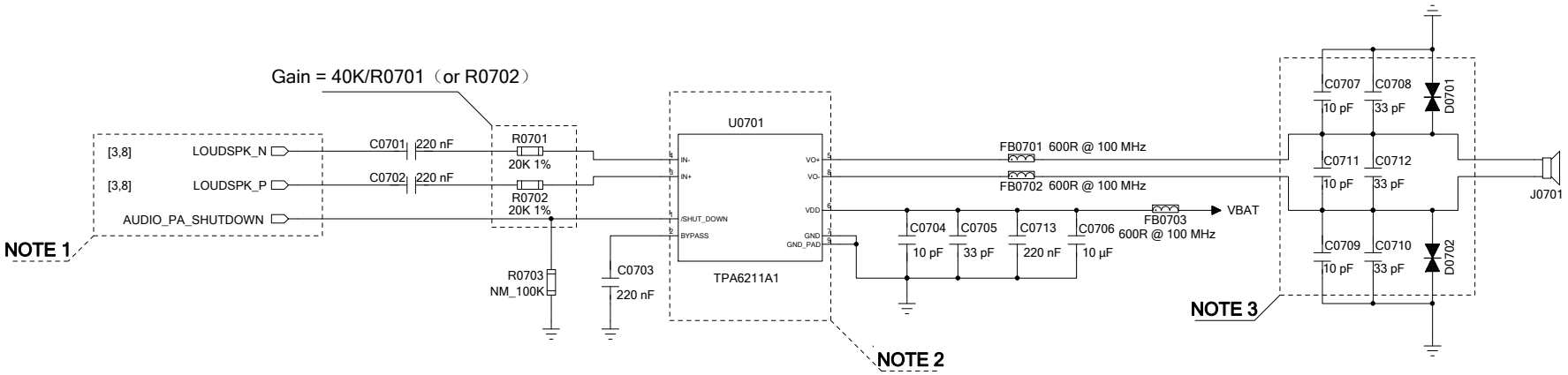
Analog Audio Design (Audio Power Amplifier)



NOTE:

1. LOUDSPK_N and LOUDSPK_P are differential output channels, which can be used for external audio amplifiers.
   In order to eliminate POP sound, the AUDIO_PA_SHUTDOWN signal of the enable pin of the power amplifier is recommended to be controlled by the GPIO pin of the module. Please contact Quectel Technical Support for details.
2. Choose the audio power amplifier with appropriate power according to the actual demand.
3. Place filter capacitors and ESD protection components close to the speaker. Choose ESD protection components according to the output voltage amplitude of the PA. To avoid damages to the ESD protection components, please ensure that the output voltage amplitude of the PA is within their maximum reverse working voltage under normal working conditions.

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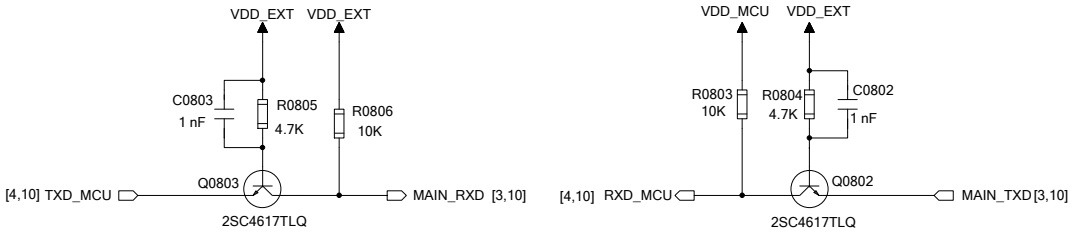
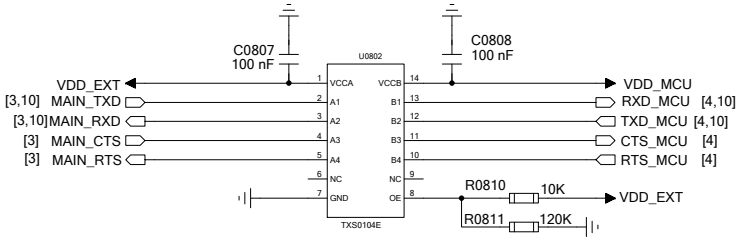
UART Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



NOTE:

1.There are two translation solutions: transistor solution and IC solution, and it is recommended to select the latter.

2.The power supply of TXS0104E's VCCA should not exceed that of VCCB. For more information, please refer to the TXS0104E datasheet.

3.The transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps. The 1 nF capacitors C0802 and C0803 can improve the signal quality.

4.The serial port hardware flow control pins CTS and RTS adopt direct connection mode, that is, the RTS of the module is connected to the RTS of the MCU, and the CTS of the module is connected to the CTS of the MCU. Pay attention to the direction of signal input and output. TXD and RXD adopt a cross connection mode, that is, the TXD and RXD of the module are respectively connected to the RXD and TXD of the MCU.

5.The MAIN_RTS transistor circuits is similar to that of the MAIN_RXD.
The MAIN_CTS transistor circuits is similar to that of the MAIN_TXD.

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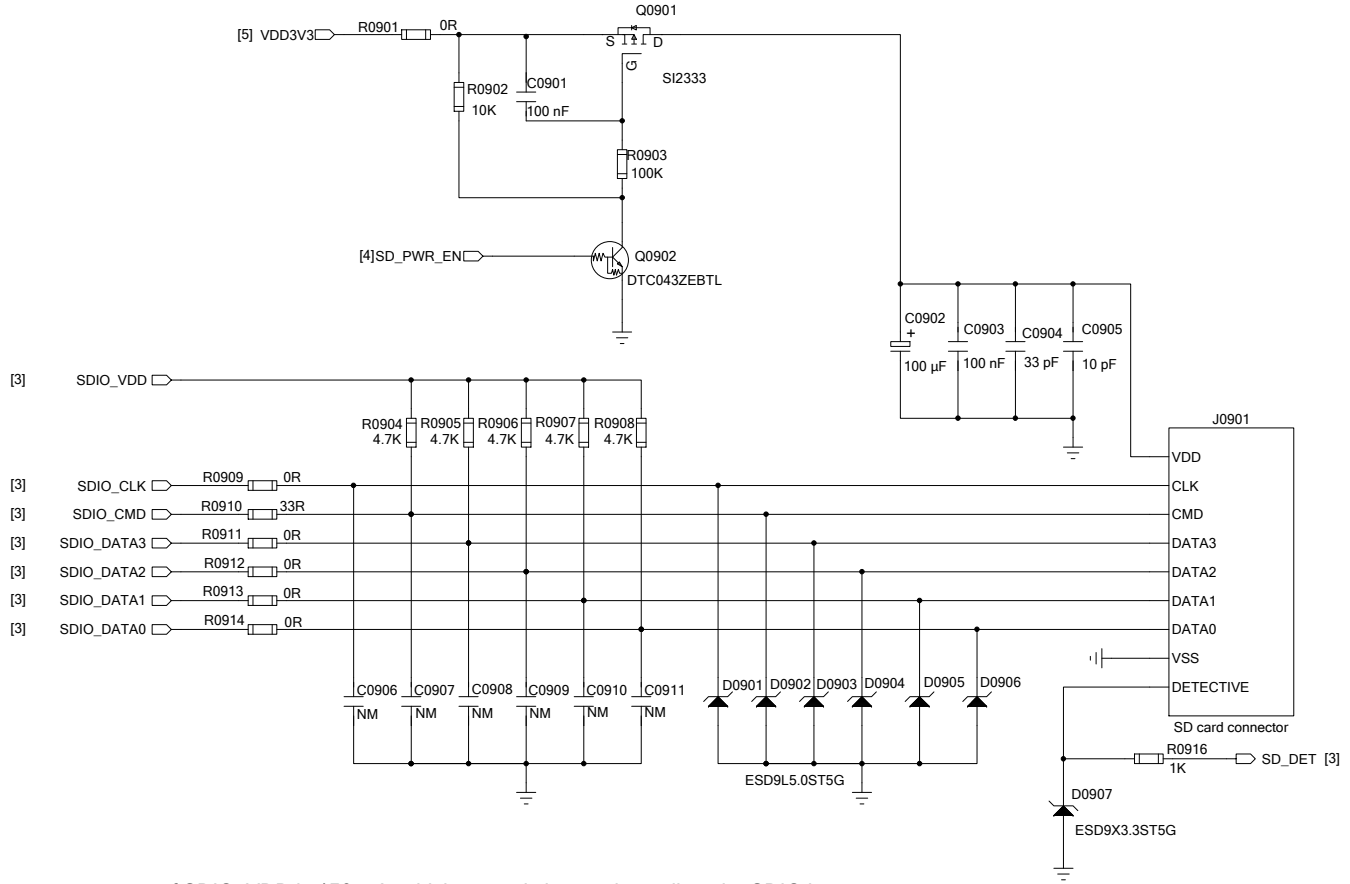
SD Card Interface Design



NOTE:

1. The maximum output current of SDIO_VDD is 150 mA, which can only be used to pull up the SDIO bus.
2. The voltage range of SD card power supply VDD is 2.7-3.6 V and a sufficient current up to 0.8 A should be provided.
3. To avoid the jitter of bus, pull-up resistors R0904-R0908 are recommended to be added to SDIO date lines. SDIO_VDD should be used as the pull-up power. The recommended value of these resistors is 4.7 kΩ.
4. In order to adjust the signal quality, it is recommended to connect resistors in series between the module and the SD card connector. The recommended value of R0909, R0911-R0914 are 0 Ω, and the recommended resistance value of R0910 is 33 Ω. The bypass capacitors C0906-C0911 are reserved and not mounted by default.
5. It is recommended to add ESD protection components near the pins of SD card connector. The parasitic capacitance of ESD protection components should be less than 15 pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, as well as noise signals such as clock and DC-DC signals.
7. Route SDIO signals with 50 Ω ±10 % impedance. It is important to route SDIO signals surrounded with ground on the layer and ground planes above and below, and the total trace length should be less than 50 mm.
8. It is recommended to keep the trace length difference among SDIO_CLK and SDIO_DATA[0:3] as well as SDIO_CMD less than 1 mm.
9. Make sure the adjacent trace spacing is twice the trace width and the load capacitance of SDIO bus should be less than 15 pF.

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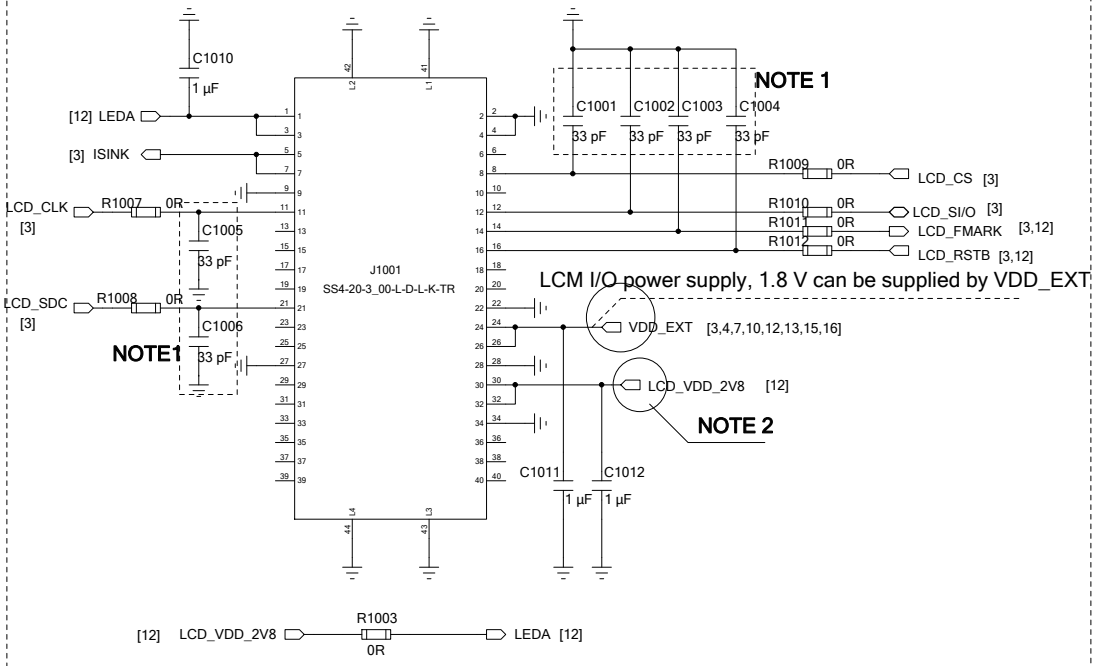
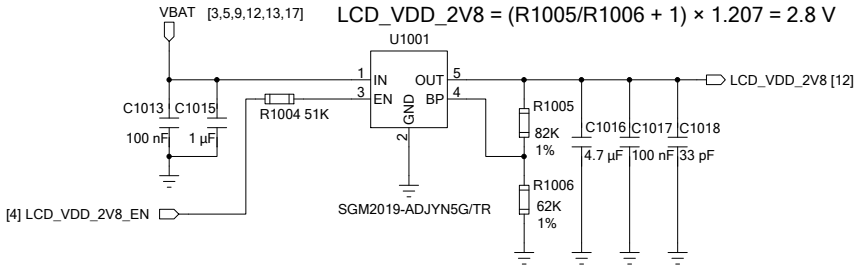
LCM Interface Design

SPI

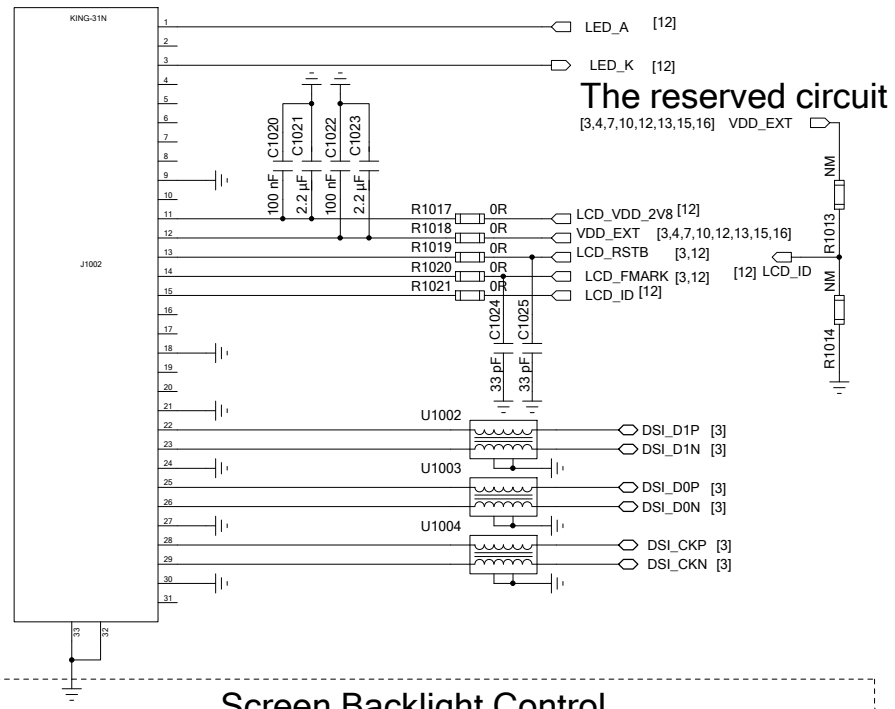




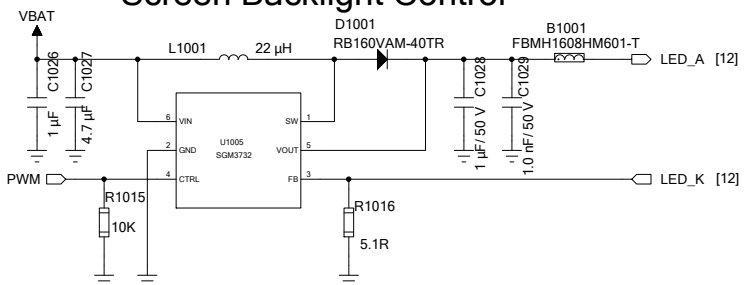
NOTE:

1. The 33 pF capacitors of the signal pins are reserved, and can be mounted or not mounted according to the actual debugging situation.
2. The power supply LCD_VDD_2V8 can be designed by yourselves.

MIPI



Screen Backlight Control



NOTE:

1. Please select the resistance value of R1016 according to the current value in the backlight chip data sheet.
2. The PWM pin can be connected to any available GPIO of the module, and the GPIO pin can be used to simulate the frequency and duty cycle. The recommended value is 3-5 kHz. Contact Quectel Technical Support for details on this pin.

NOTE:

You can use either SPI or MIPI in the LCM interface design.

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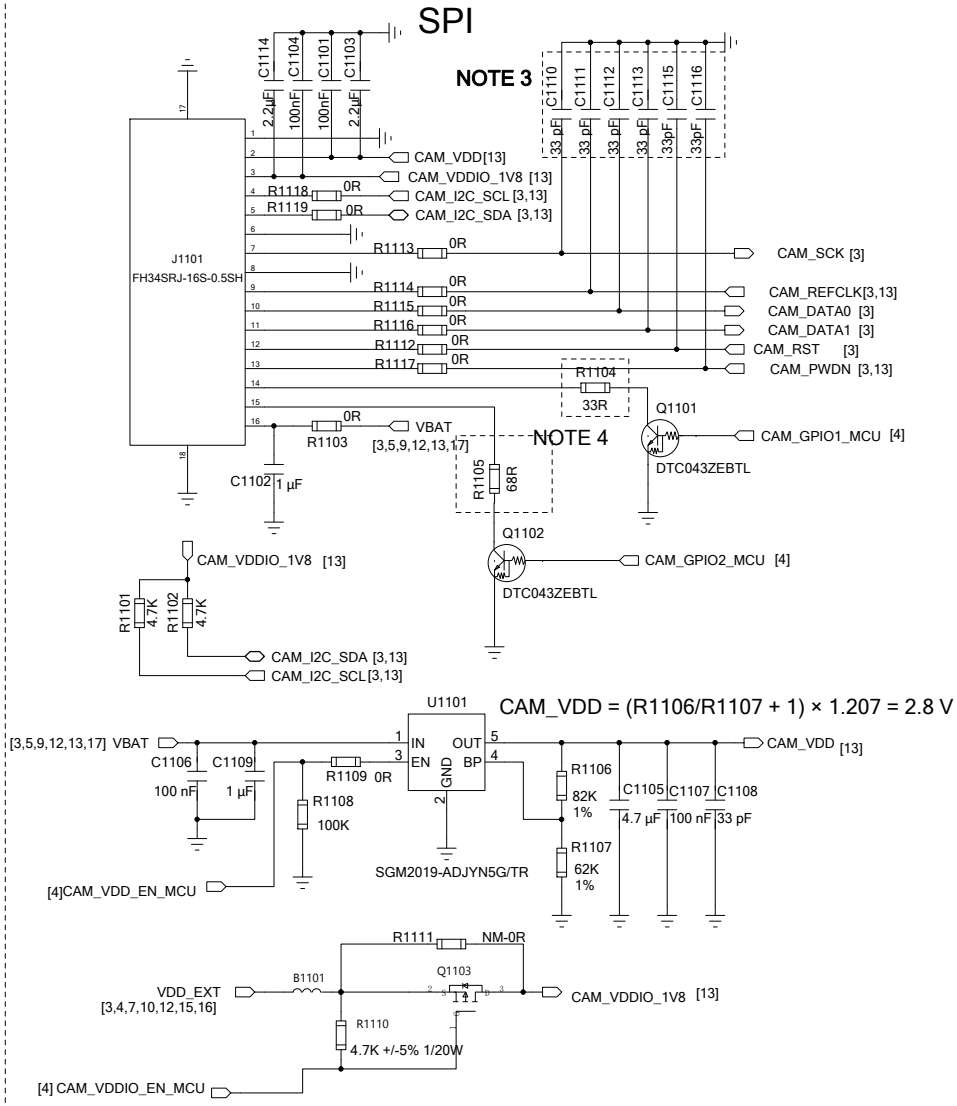
Camera Interface Design

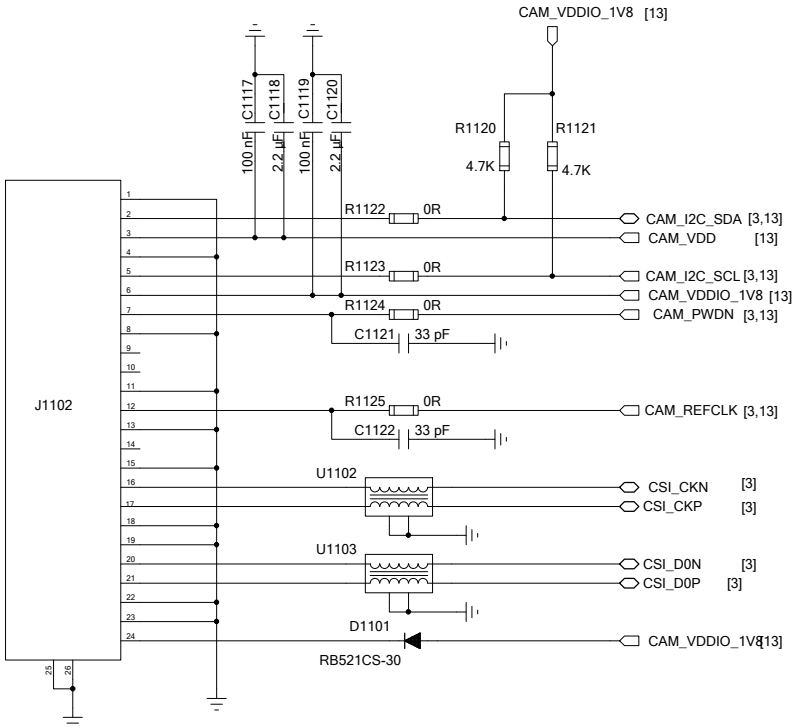
SPI



NOTE:

1. CAM_VDD_EN_MCU is used to control the CAM_VDD analog power supply of the camera.
   CAM_VDDIO_EN_MCU is used to control the CAM_VDDIO_1V8 power supply of the camera.
   The CAM_VDD and CAM_VDDIO_1V8 power supply need to be designed by yourself.
2. CAM_GPIO1_MCU controsl the cathode of the position lamp of the camera by controlling the transistor switch circuit;
   CAM_GPIO2_MCU controls the cathode of the fill light of the camera by controlling the transistor switch circuit;
   You can design and select the GPIO pins with default pull-down status for CAM_GPIO1_MCU and CAM_GPIO2_MCU.
3. The 33 pF capacitors of the signal pins are reserved and can be mounted or not mounted according to the actual debugging situation.
4. The value of the current-limiting resistors R1104 and R1105 of the position lamp and fill light can be selected according to actual brightness requirements.

MIPI



NOTE:

1. CAM_RST is multiplexed as the CSI_CKN function of MIPI camera.
   CAM_DATA0 is multiplexed as the CSI_CKP function of MIPI camera.
   CAM_DATA1 is multiplexed as the CSI_D0N function of MIPI camera.
   CAM_SCK is multiplexed as the CSI_D0P function of MIPI camera.
2. The position lamp and fill light can be designed by yourselves.

NOTE:

You can use either SPI or MIPI in the camera interface design, and it's recommended to choose the former.

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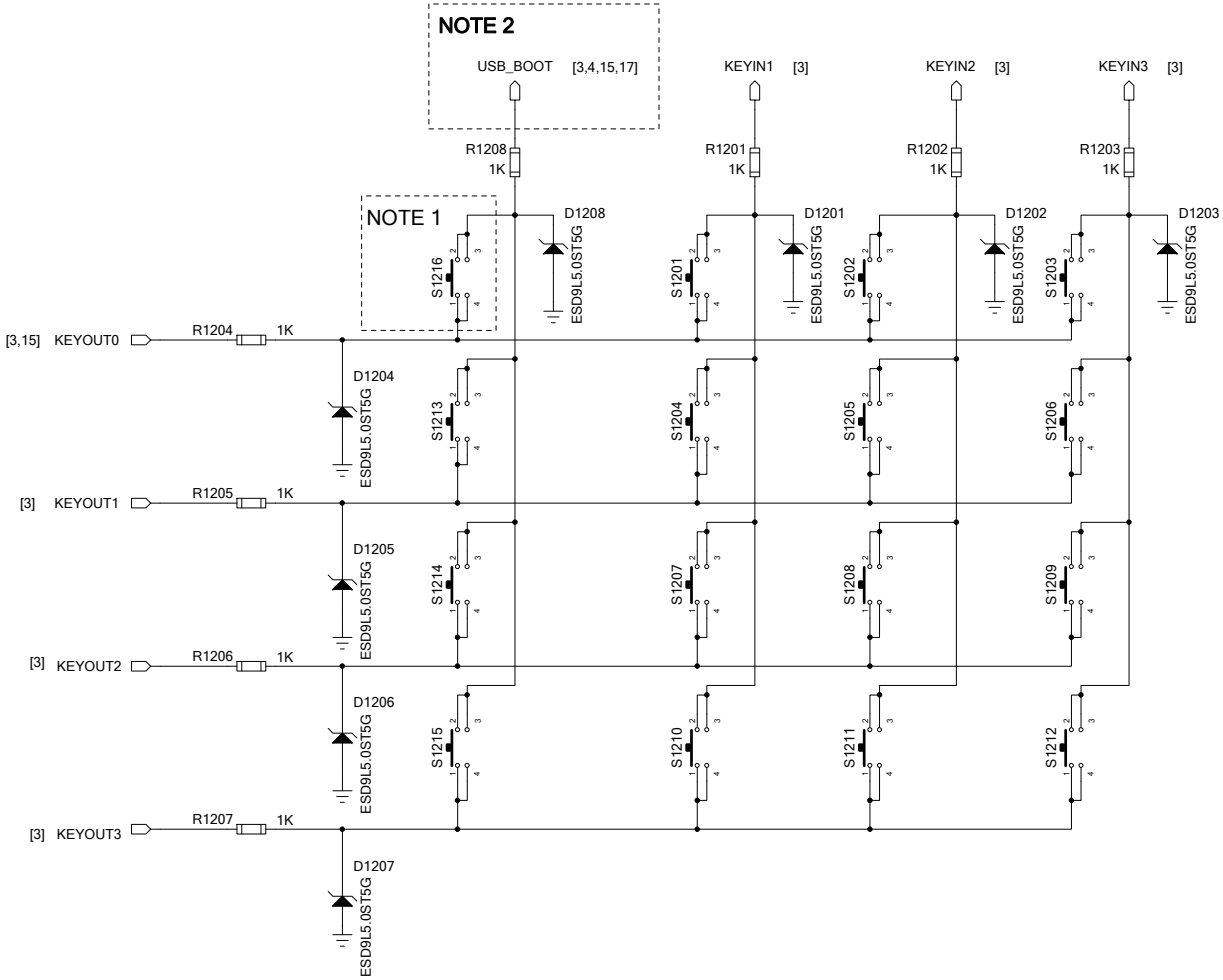
Matrix Keyboard Design



NOTE:

1. Press the scan keys composed of "USB_BOOT+KEYOUT0" before the module is powered on, and the module will enter the download mode after being powered on.
2. After the module is turned on normally, the USB_BOOT pin can be used as KEYIN0, which can be combined with other key pins to form the matrix keyboard.

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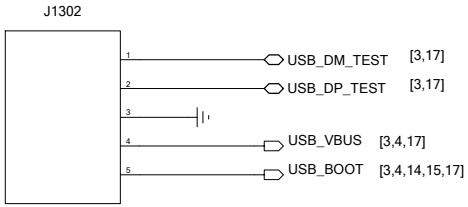
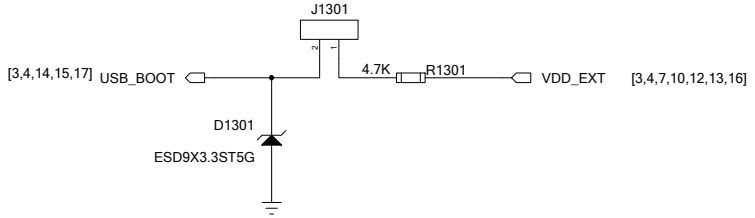
Download Method

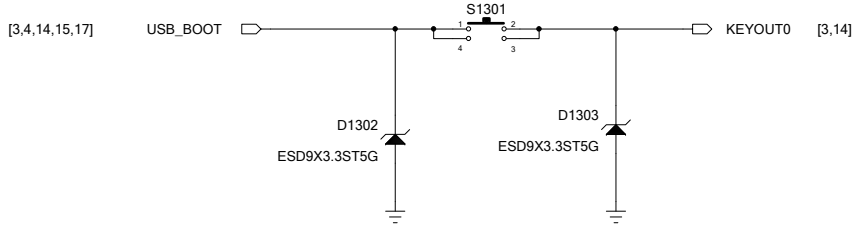
USB Download Interface Design



USB_BOOT Interface Design Method I



USB_BOOT Interface Design Method II



NOTE:

1. When the module needs to upgrade the firmware, it must first enter the download mode. There are two ways for making the module enter the download mode:
   Method I: Short-circuit USB_BOOT and VDD_EXT before the module is powered on, and the module will enter the download mode after being powered on;
   Method II: Press the keys composed of "USB_BOOT+KEYOUT0" before the module is powered on, and the module will enter the download mode after being powered on.
2. Be sure to reserve the USB_BOOT interface circuit (choose one of the two methods) to upgrade the firmware.
   If your application has a scan key design, it is recommended to adopt the download circuit design of method II, that is, enter the download mode through the keys, which is convenient for the module to upgrade the firmware.

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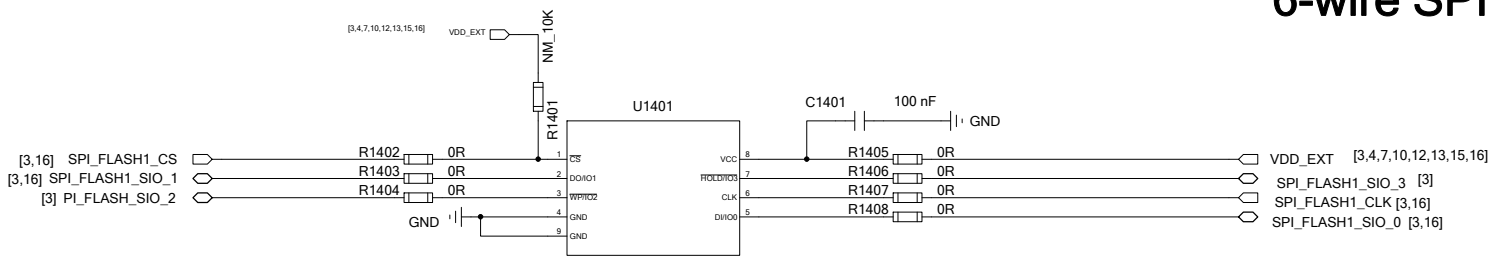
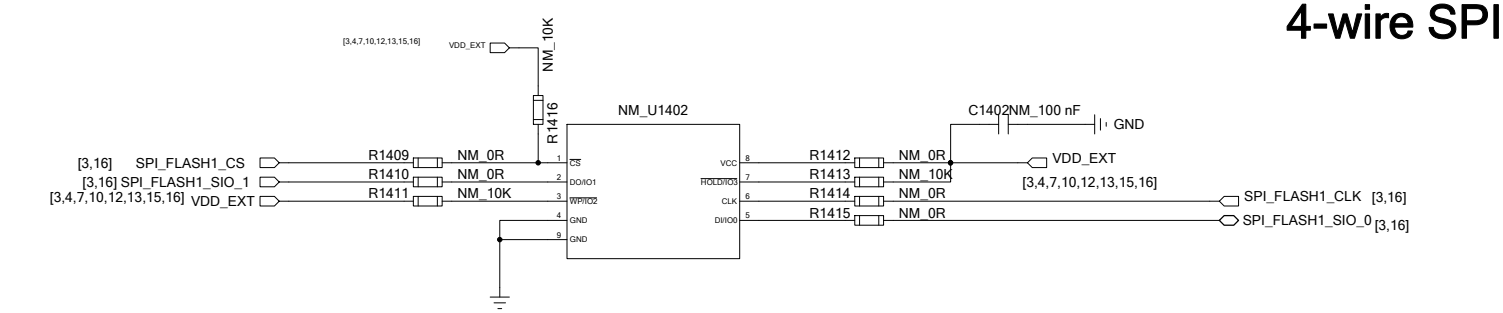
Flash Interface Design

6-wire SPI



4-wire SPI



NOTE:

1. The SPI interface only supports master mode.
2. If you choose a module without GNSS function, you can take pins 37-40 as general 4-wire SPI signal pins.
3. The filter capacitors C1401 and C1402 need to be placed close to the power pins of the flash chip to achieve the expected filtering effect.
4. The signal cable of Flash must be of equal length, and the cable length error is less than 1 mm.

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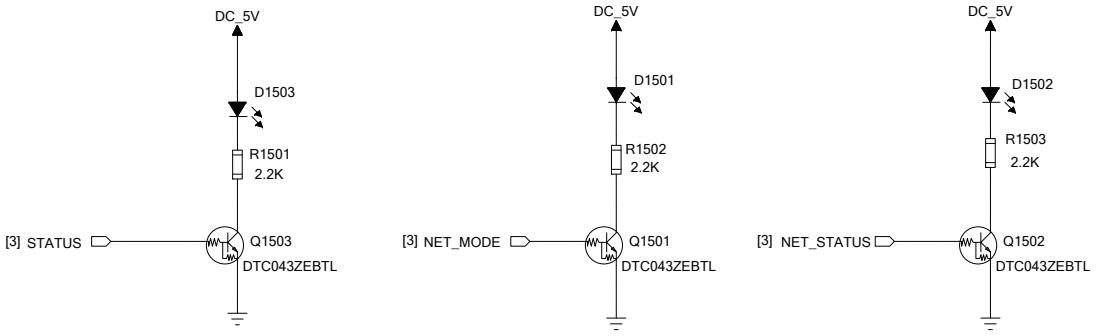
Other Designs

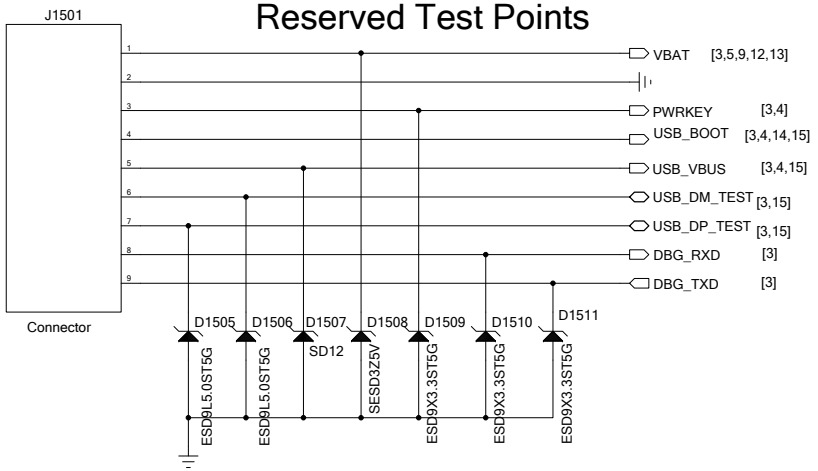
Indicator Light



NOTE:

1. For more details about NET_MODE and NET_STATUS, please refer to *Quectel_EC200U_Series_QuecOpen_Hardware_Design*.
1. If the low current consumption is required when the your application is in sleep status, replace the power supply (DC_5V) of the STATUS, NET_MODE, NET_STATUS indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

Reserved Test Points



NOTE:

1. Test points for both USB and debug UART interfaces are reserved for capturing logs.
2. Test points for USB interface also can be reserved for firmware upgrade.
3. The parasitic capacitance of the ESD protection components on USB data lines should be less than 2 pF.
4. Debug UART interface supports 1.8 V power domain, and a voltage-level translator should be used if the power domain of your application is 3.3 V. The debug UART only supports 921600 bps baud rate.
5. When the module needs to upgrade the firmware, it must firstly enter the download mode. Pull up USB_BOOT to VDD_EXT before the module is powered on, the module will enter download mode.

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