EC200U Series QuecOpen Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-02-21	King MA/ Nathan LIU	Creation of the document
1.0	2023-08-31	Denny QIN/ Chris LIANG/ Ryan YI	First official release

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines the EC200U series QuecOpen® module and describes its air interface and hardware interfaces which are connected with your applications.

It can help you quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use this module to design and to set up mobile applications easily.

This document is applicable to the following variants:

- EC200U-CN
- EC200U-EU
- EC200U-AU

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument and so on, it indicates that the function, feature, interface, pin, AT command, argument and so on, is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2 and SDIO_DATA3.

2 Product Overview

2.1. Frequency Bands and Functions

EC200U series is an LTE Cat 1 wireless communication module, which supports LTE-FDD, LTE-TDD and GSM/GPRS network data connections. The module provides voice function for your special applications and supports GNSS [1], Bluetooth and Wi-Fi Scan [2] functions. The following table shows the frequency bands and functions of the module.

Table 2: Frequency Bands and Functions of the Module

Network Mode and Functions	EC200U-CN	EC200U-EU	EC200U-AU
LTE-FDD	B1/B3/B5/B8	B1/B3/B5/B7/B8/B20/B28	B1/B2/B3/B4/B5/B7/B8/B28/B66
LTE-TDD	B34/B38/B39/B40/B41	B38/B40/B41	B38/B40/B41
GSM [3]	B3/B8	B2/B3/B5/B8	B2/B3/B5/B8
GNSS [1]	GPS, GLONASS, BDS, Galileo, QZSS		
Bluetooth and Wi-Fi Scan [2]	Supported	Supported	Supported

With a compact profile of 28.0 mm × 31.0 mm × 2.4 mm, the module can meet most of requirements for M2M applications such as automation, metering, tracking system, smart safety, router, wireless POS, mobile computing device, PDA phone and tablet PC.

EC200U series is an SMD module which can be embedded into applications through 144 pins, including 80 LCC pins and 64 LGA pins.

[1] GNSS function is optional.
[2] The module supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used at the same time; Bluetooth and Wi-Fi Scan functions are optional. Please contact Quectel Technical Support for details.
[3] GSM network of EC200U-CN is optional.

2.2. Key Features

Table 3: Key Features of the Module

Feature	Details
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 4 (33 dBm ±2 dB) for GSM850 ● Class 4 (33 dBm ±2 dB) for EGSM900 ● Class 1 (30 dBm ±2 dB) for DCS1800 ● Class 1 (30 dBm ±2 dB) for PCS1900 ● Class 3 (23 dBm ±2 dB) for LTE-FDD bands ● Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	● Supports Cat 1 FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Max. transmission data rates: LTE-FDD: 10 Mbps (DL)/5 Mbps (UL) LTE-TDD: 8.96 Mbps (DL)/3.1 Mbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1–4 ● Max. transmission data rates: 85.6 kbps (DL)/85.6 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/FTPS/SSL/FILE/MQTT/MMS protocols ● Supports PAP and CHAP for PPP connections
SMS	● Text and PDU mode ● Point to point MO and MT ● SMS cell broadcast ● SMS storage: (U) SIM card and ME, ME by default
(U)SIM Interfaces	● Supports (U)SIM/SIM card: 1.8/3.0 V ● Supports dual-SIM dual standby
USB Interface	● Compliant with USB 2.0 specification (slave mode only); the data transmission rate can reach up to 480 Mbps ● Used for data transmission, software debugging and firmware upgrade ● Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–6.5, Android 4.x–13.x, etc.
UART Interfaces [4]	**Main UART:** ● Used for data transmission ● Support RTS and CTS hardware flow control

[4] If the module you choose does not support the GNSS function, the UART3 function can be supported. For details, please consult Quectel Technical Support.

	Debug UART: ● Used for AP log output ● Can only be used as a debug UART, not a general-purpose UART **Auxiliary UART**
SPI Interface	Supports master mode only
I2C Interfaces	Supports two I2C interfaces
PCM Interface	● Supports one PCM interface ● Only supports slave mode
External Flash Interface	Supports external flash chip
Audio Features	● Supports one analog audio input and one analog audio output ● HR/FR/EFR/AMR/AMR-WB ● Supports echo cancellation and noise suppression
LCM Interface	Supports LCM interface in SPI and MIPI modes
Camera Interface	● Provides one camera interface supporting cameras up to 0.3 megapixel; I/O pins only support 1.8 V ● Supports the two-data-line transmission of SPI ● Supports MIPI data transmission
Matrix Keypad Interface	Supports 4 × 6 matrix keypad [5]
SD Card Interface	Compliant with SD 2.0 protocol
WLAN Application Interface*	Supports SDIO 1.1 interface for WLAN function
ADC Interfaces	Provides three ADC interfaces
Network Status Indication	Two pins NET_MODE and NET_STATUS indicate network connectivity status
USB_BOOT Interface	Supports one USB_BOOT interface
Antenna Interfaces	● Main antenna interface (ANT_MAIN), Wi-Fi Scan/Bluetooth [2] antenna interface (ANT_BT/WIFI_SCAN) and GNSS [1] antenna interface (ANT_GNSS) ● 50 Ω characteristic impedance
Location	Supports Wi-Fi Scan/GNSS
Physical Characteristics	● Size: (28.0 ±0.15) mm × (31.0 ±0.15) mm × (2.4 ±0.2) mm

[5] GNSS function is optional, and you can use 4 × 6 matrix keypad for the module without GNSS, and 4 × 4 keypad for the module with GNSS.

	• Weight: approx. 4.1 g
Temperature Ranges	• Operating temperature range: -35 °C to +75 °C [6] • Extended temperature range: -40 °C to +85 °C [7] • Storage temperature range: -40 °C to +90 ℃
Firmware Upgrade	Via USB interface or FOTA
RoHS	All hardware components are fully compliant with *EU RoHS Directive*

[6] Within the operating temperature range, the module meets 3GPP specifications.
[7] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- Flash
- Radio frequency
- Peripheral interfaces

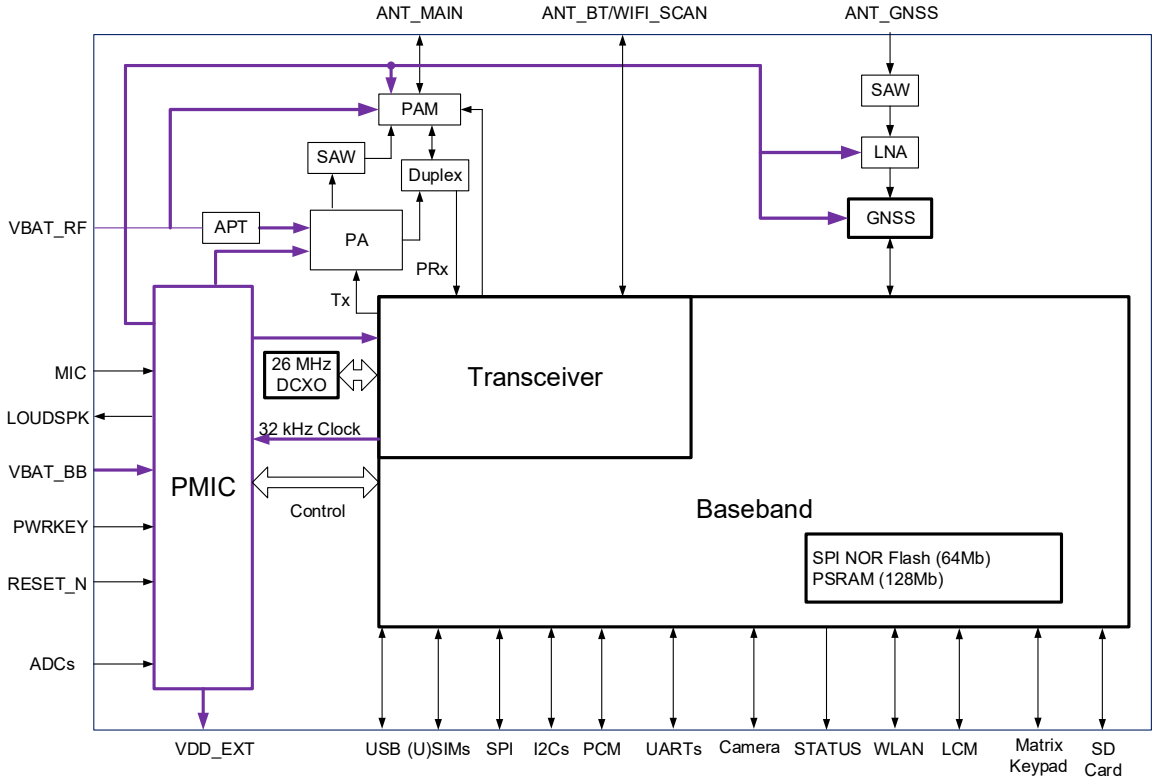


Figure 1: Functional Diagram

2.4. EVB Kit

Quectel supplies an evaluation board (LTE OPEN EVB) with accessories to develop or test the module. For more details, see ***document [1]***.

3 Application Interfaces

3.1. General Description

The module is equipped with 80 LCC pins plus 64 LGA pins that can be connected to cellular application platform. The subsequent chapters will provide detailed descriptions of the following interfaces.

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- SPI interface
- I2C interfaces
- PCM interface
- External flash interface
- Analog audio interfaces
- LCM interface
- Camera interface
- Matrix keypad interface
- SD card interface
- WLAN application interface*
- ADC interfaces
- Network indications
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of the module.

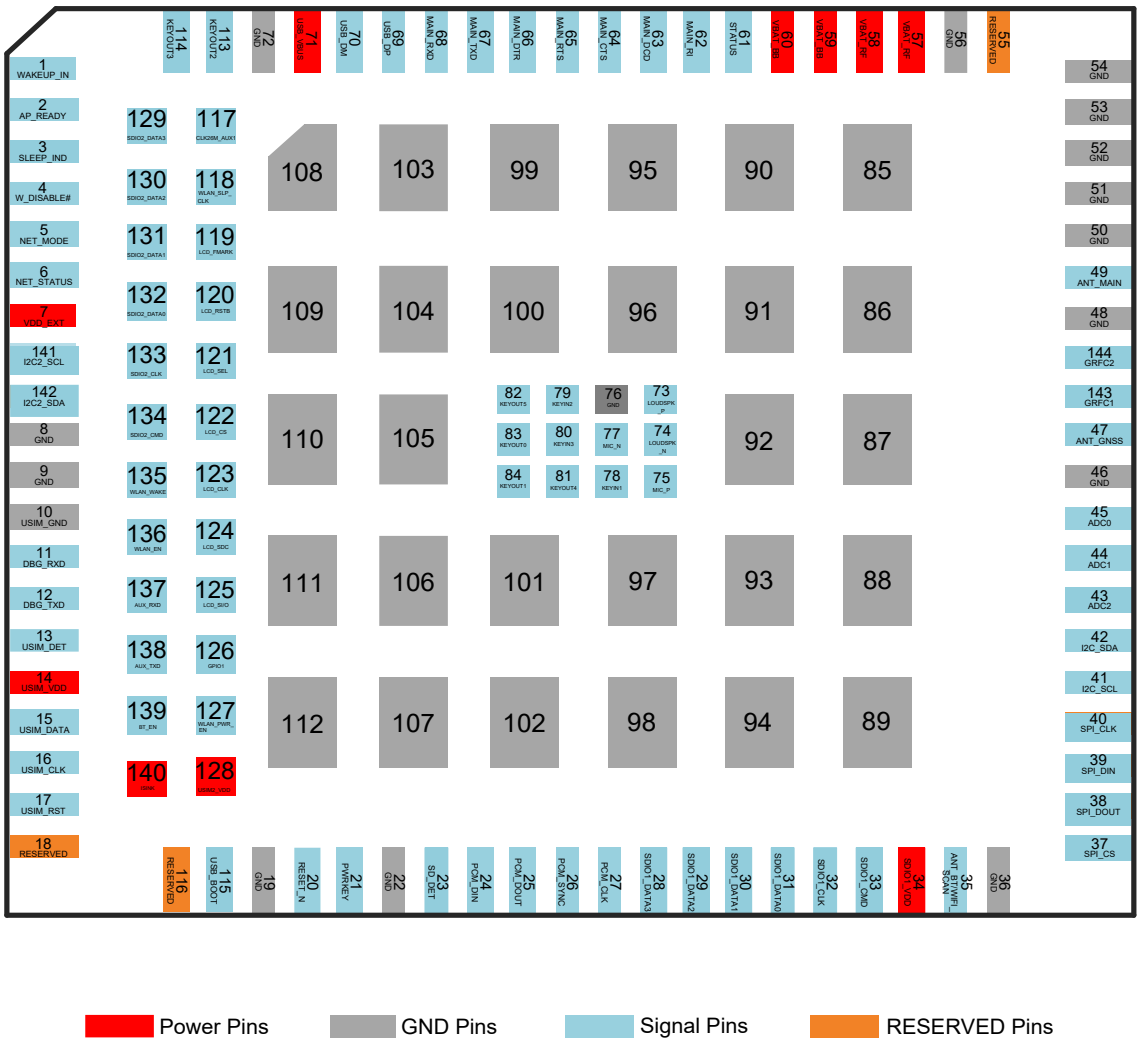


Figure 2: Pin Assignment (Top View)

NOTE

1. If the download function is not used, do not pull USB_BOOT up before the module's successful startup.
2. KEYIN1 cannot be pulled up before the module's successful startup.
3. Please keep all RESERVED and unused pins unconnected; all GND pins should be connected to the ground.

3.3. Pin Description

The following tables show the pin definition of the module.

Table 4: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rate current.

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for module's baseband part and RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current of at least 1.5 A.
VBAT_RF	57, 58	PI	Power supply for module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current of at least 2.0 A.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 76, 85–112				
Power Supply Output					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. Add 2.2 μF capacitor and TVS components if used. A test point is recommended to be reserved.
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module	V_{IL}max = 0.5 V	VBAT power domain.
RESET_N	20	DI	Reset the module	V_{IL}max = 0.5 V	VBAT power domain. Active low. A test point is recommended to be reserved.
Network Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	DO	Indicate module's operation status		1.8 V power domain. If unused, keep them open.
NET_MODE	5	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	
NET_STATUS	6	DO	Indicate the module's network registration mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	71	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.5 V Vnom = 5.0 V	Typical: 5.0 V. A test point must be reserved.
USB_DP	69	AIO	USB 2.0 differential data (+)		Require differential impedance of 90 Ω. USB 2.0 compliant. Test points must be
USB_DM	70	AIO	USB 2.0 differential data (-)		

					reserved.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	10		(U)SIM1 card GND		Connect to the GND of (U)SIM card connector.
USIM_VDD	14	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported and can be identified by the module automatically.
USIM_DATA	15	DIO	(U)SIM1 card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max =1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_CLK	16	DO	(U)SIM1 card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_RST	17	DO	(U)SIM1 card reset	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_DET	13	DI	(U)SIM1 card	V_{IL}min = -0.3 V	1.8 V power domain.

			hot-plug detect	V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	If unused, keep it open.
USIM2_VDD	128	PO	(U)SIM2 card power supply	$I_O$max = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V (U)SIM is supported and can be identified by the module automatically.
AP_READY	2	DIO	(U)SIM2 card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	The relevant functions of the (U)SIM2 card can be realized by multiplexing AP_READY, WAKEUP_IN, SLEEP_IND and W_DISABLE#. For details, please consult Quectel Technical Support.
WAKEUP_IN	1	DO	(U)SIM2 card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
SLEEP_IND	3	DI	(U)SIM2 card hot-plug detect	V_{IL}min = -0.3 V	
W_DISABLE#	4	DO	(U)SIM2 card reset	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

MAIN_CTS	64	DO	Clear to send signal from the module	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	Connect to the MCU's CTS. 1.8 V power domain. If unused, keep it open.
MAIN_RTS	65	DI	Request to send signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	Connect to the MCU's RTS. 1.8 V power domain. If unused, keep it open.
MAIN_TXD	67	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
MAIN_RXD	68	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	12	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Test points must be reserved to capture AP log.
DBG_RXD	11	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
Auxiliary UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_RXD	137	DI	Auxiliary UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
AUX_TXD	138	DO	Auxiliary UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC2	43	AI	General-purpose ADC interface	Voltage range: 0 V–VBAT_BB	It is recommended to reserve a divider circuit. If unused, keep them open.
ADC1	44	AI			
ADC0	45	AI			

Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LOUDSPK_P	73	AO	Loudspeaker differential output (+)		If unused, keep them open.
LOUDSPK_N	74	AO	Loudspeaker differential output (-)		
MIC_P	75	AI	Microphone analog input (+)		
MIC_N	77	AI	Microphone analog input (-)		
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock		Require external pull-up to 1.8 V if used. If unused, keep them open.
I2C_SDA	42	OD	I2C serial data		
I2C2_SCL	141	OD	I2C serial clock		
I2C2_SDA	142	OD	I2C serial data		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_DIN	24	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
PCM_DOUT	25	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCM_SYNC	26	DI	PCM data frame sync	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open. The PCM function only supports slave mode.
PCM_CLK	27	DI	PCM clock		
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CS	37	DO	SPI chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	If the module model you choose supports

SPI_DOUT	38	DO	SPI data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	GNSS function, the SPI function cannot be used and pins 37–40 need to be left unconnected.
SPI_DIN	39	DI	SPI data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
SPI_CLK	40	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_FMARK	119	DI	LCD frame synchronization	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
LCD_RSTB	120	DO	LCD reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_SEL	121		Reserved		
LCD_CS	122	DO	LCD chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
LCD_CLK	123	DO	LCD clock		
LCD_SDC	124	DO	LCD register selection		
LCD_SI/O	125	DIO	LCD data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
ISINK	140	PI	Sink current input. Backlight adjustment	Imax = 200 mA. Configurable current	It is driven by the current sink, and connected to the backlight cathode. The brightness can be adjusted with current control.
Matrix Keypad Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Matrix key input 0		It can be multiplexed as KEYIN0 after the module's startup.
KEYIN1	78	DI	Matrix key input 1		1.8 V power domain. If unused, keep it open. The KEYIN1 cannot be pulled up

					before startup.
KEYIN2	79	DI	Matrix key input 2		1.8 V power domain. If unused, keep them open.
KEYIN3	80	DI	Matrix key input 3		
KEYOUT0	83	DO	Matrix key output 0		
KEYOUT1	84	DO	Matrix key output 1		
KEYOUT2	113	DO	Matrix key output 2		
KEYOUT3	114	DO	Matrix key output 3		
KEYOUT4 [8]	81	DO	Matrix key output 4		
KEYOUT5 [8]	82	DO	Matrix key output 5		
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_DET	23	DI	SD card detect		1.8 V power domain. If unused, keep it open.
SDIO1_DATA3	28	DIO	SDIO data bit 3		3.2 V power domain. If unused, keep them open.
SDIO1_DATA2	29	DIO	SDIO data bit 2		
SDIO1_DATA1	30	DIO	SDIO data bit 1		
SDIO1_DATA0	31	DIO	SDIO data bit 0		
SDIO1_CLK	32	DO	SDIO clock		
SDIO1_CMD	33	DIO	SDIO command		
SDIO1_VDD	34	PO	SDIO power supply		
WLAN Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SLP_CLK	118	DO	WLAN sleep clock		If unused, keep it open.
WLAN_PWR_EN	127	DO	WLAN power supply enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them

[8] GNSS function is optional, and you can use 4 × 6 matrix keypad with pins 81 and 82 for the module without GNSS, and 4 × 4 matrix keypad for the module with GNSS function (pins 81 and 82 are kept open).

SDIO2_DATA3	129	DIO	WLAN SDIO data bit 3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	open.
SDIO2_DATA2	130	DIO	WLAN SDIO data bit 2		
SDIO2_DATA1	131	DIO	WLAN SDIO data bit 1		
SDIO2_DATA0	132	DIO	WLAN SDIO data bit 0		
SDIO2_CLK	133	DO	WLAN SDIO clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SDIO2_CMD	134	DIO	WLAN SDIO command	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
WLAN_WAKE	135	DI	Wake up the host (the module) by an external Wi-Fi module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
WLAN_EN	136	DO	WLAN function enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_BT/WIFI_SCAN	35	AIO	The shared antenna interface of Bluetooth and Wi-Fi Scan		Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan antenna can only receive but not transmit. 50 Ω characteristic impedance. If unused, keep it open.
ANT_GNSS	47	AI	GNSS antenna interface		50 Ω characteristic impedance. If unused, keep it open.
ANT_MAIN	49	AIO	Main antenna interface		50 Ω characteristic impedance.
USB_BOOT					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_BOOT	115	DI	Control the module to enter download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Active high. A circuit that enables the module to enter the download mode must be reserved. A test point is recommended to be reserved.
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	1	DIO	General-purpose input/output	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	GPIO function by default. 1.8 V power domain. If unused, keep them open.
AP_READY	2	DIO			
SLEEP_IND	3	DIO			
W_DISABLE#	4	DIO			
MAIN_RI	62	DIO			
MAIN_DCD	63	DIO			
MAIN_DTR	66	DIO			
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	126	DO	CP log		It can output CP log, and only 8 Mbps baud rate is supported. A test points must be reserved.
BT_EN	139		Reserved		
GRFC1	143	DIO	Generic RF controller		
GRFC2	144	DIO	Generic RF controller		
CLK26M_AUX1	117		Reserved		

Reserved Pins		
Pin Name	**Pin No.**	**Comment**
RESERVED	18, 55, 116	Keep these pins open.

NOTE

For GPIO configurations, see ***document [2]***.

3.4. Operating Modes

Table 6: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	Use *ql_dev_set_modem_fun()* to set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM are invalid.	
Airplane Mode	Use *ql_dev_set_modem_fun()* to set the module to airplane mode. In this case, RF function is invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. In this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, PMIC shuts down the power supply. Software is inactive, while operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

NOTE

For details about the above API, see ***document [3]***.

3.5. Power Saving

3.5.1. Sleep Mode

The module can reduce its current consumption to a minimal level in sleep mode. The following sections describe power saving procedures of the module.

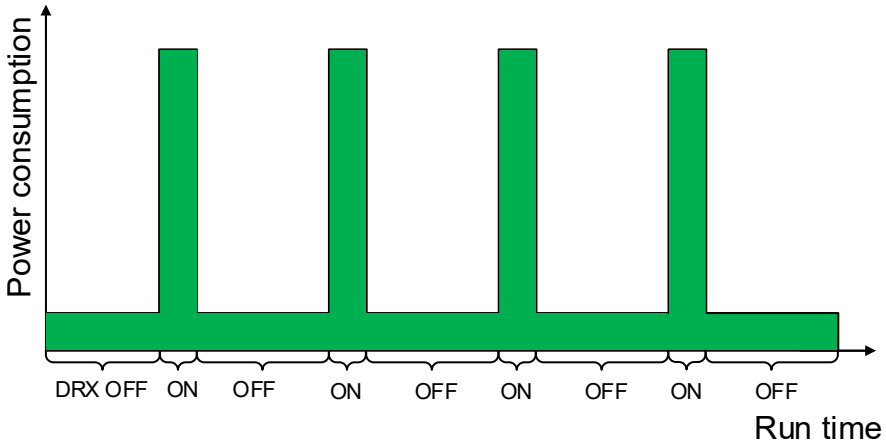


Figure 3: Power Consumption During Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.5.1.1. USB Application with USB Suspend/Resume Function

For the following two scenarios:

- The host supports USB suspend/resume and remote wakeup functions
- The host supports USB suspend/resume, but does not support remote wake-up function

The following three preconditions must be met to make the module enter sleep mode:

- Enable sleep function through *ql_autosleep_enable()*. See ***document [4]*** for details on the API.
- Ensure that all wakelocks have been released.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

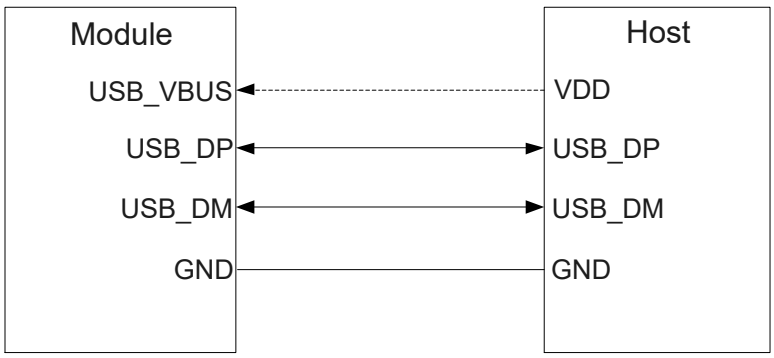


Figure 4: Sleep Mode Application with USB Suspend/Resume Function

Sending data to the module through USB can wake up the module.

3.5.1.2. USB Application Without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be disconnected via an external control circuit of USB_VBUS to let the module enter sleep mode.

- Enable sleep function through *ql_autosleep_enable()*.
- Ensure that all wakelocks have been released.
- Disconnect USB_VBUS power supply.

The following figure shows the connection between the module and the host.

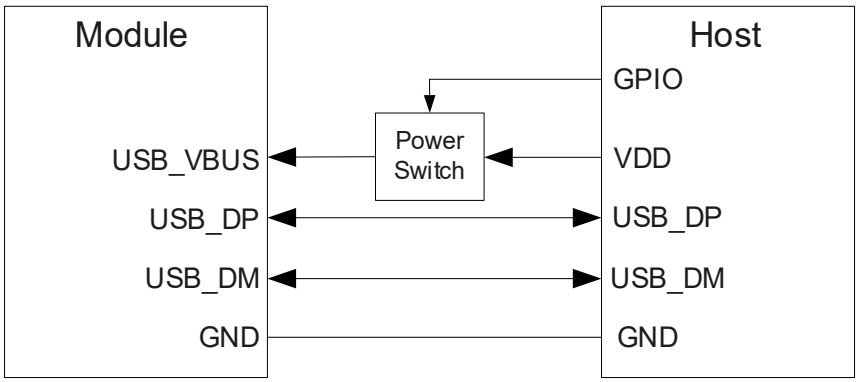


Figure 5: Sleep Mode Application Without Suspend Function

The module will be woken up when USB_VBUS power supply is restored.

NOTE

1. USB suspend is supported on Linux system but not supported on Windows system.
2. Please pay attention to the level match shown in dotted line between the module and the host in ***Chapter 3.5.1***.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function does not work, and API related to RF function will be not accessible.

ql_dev_set_modem_fun() provides the choice of the functionality level through setting *at_dst_cfun* into 0, 1 or 4.

- *at_dst_cfun* is *0*: Minimum functionality mode (Both RF and (U)SIM functions are disabled).
- *at_dst_cfun* is *1*: Full functionality mode (by default).
- *at_dst_cfun* is *4*: Airplane mode (RF function is disabled).

3.6. Power Supply

3.6.1. Power Supply Pins

The module provides four VBAT pins for connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's baseband part and RF part.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	59, 60	Power supply for module's baseband part and RF part	3.3	3.8	4.3	V
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 76, 85–112					

3.6.2. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure that the input voltage will never drop below 3.3 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 4G networks.

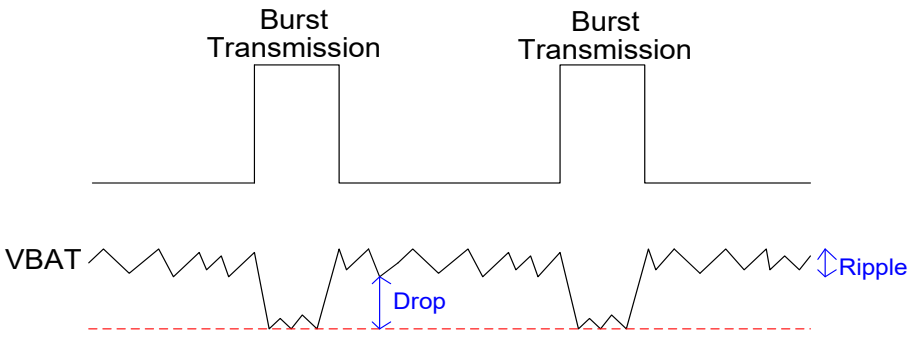


Figure 6: Power Supply Limits during Burst Transmission

To decrease voltage drop, a filter capacitor of about 100 μF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT_BB and VBAT_RF. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star configuration routing. The width of VBAT_BB trace should be not less than 2 mm; and the width of VBAT_RF trace should be not less than 2.5 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used.

The following figure shows the star configuration routing of the power supply.

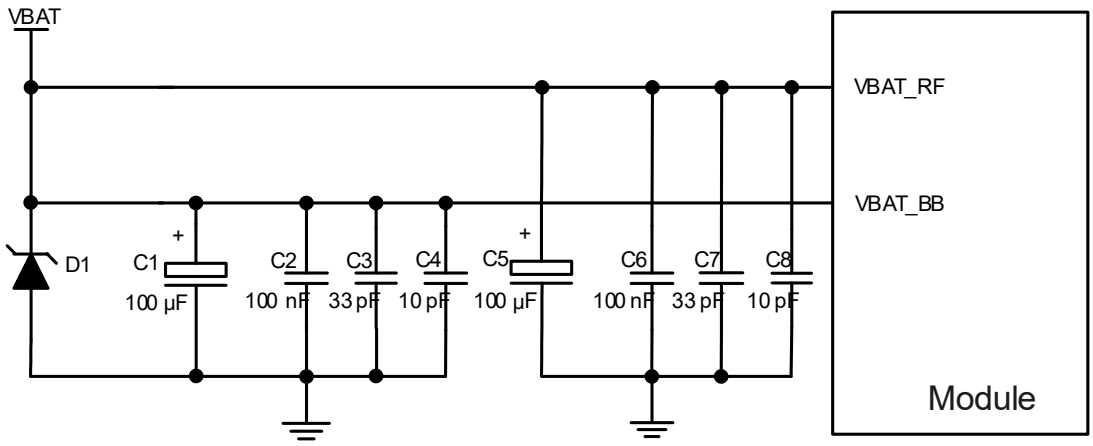


Figure 7: Star Configuration Routing of Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current of at least 2.0 A to the module that only supports LTE network, while at least 3.0 A should be provided when GSM network is available. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used. If there is a big voltage difference between the input source and the desired output (VBAT), use a buck converter as the power supply.

The following figure shows a reference design for 5 V input power source.

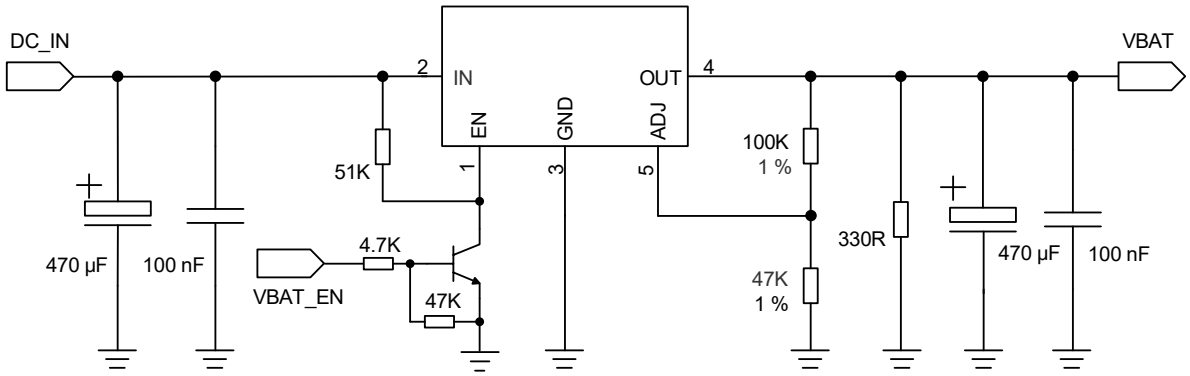


Figure 8: Reference Circuit of Power Supply

3.7. Turn On/Turn Off/Reset

3.7.1. Turn On Module with PWRKEY

Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	VBAT power domain.

When the module is in power-down mode, it can be turned on to normal mode by driving PWRKEY to a low level for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

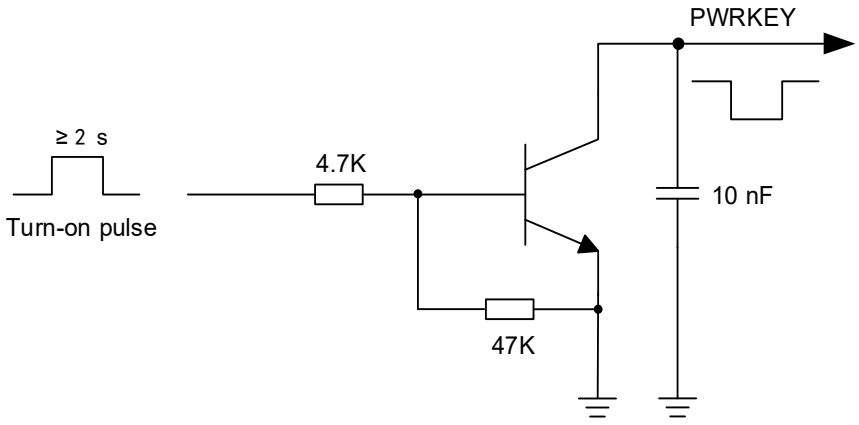


Figure 9: Turn On Module by Using Driving Circuit

Another way to control the PWRKEY is to use a button directly. When pressing the button, electrostatic strike may generate from finger. Therefore, it is indispensable to place a TVS nearby the button for ESD protection.

A reference circuit is shown in the following figure.

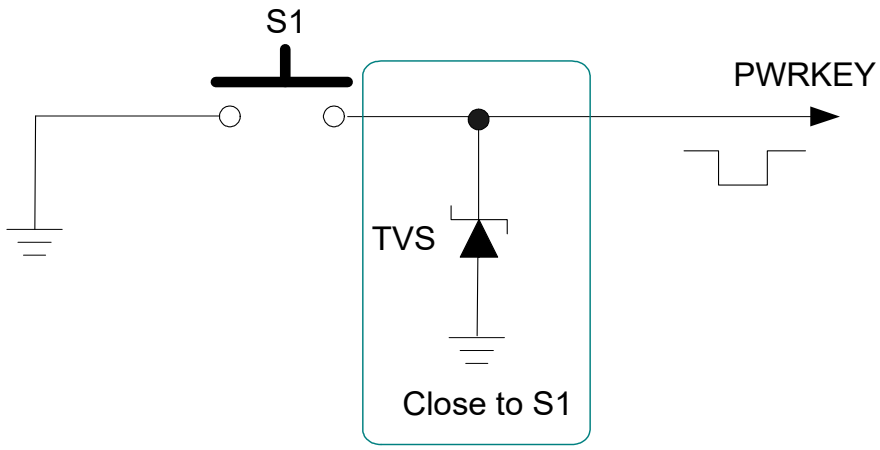


Figure 10: Turn On Module by Using Button

The turn-on timing is illustrated in the following figure.

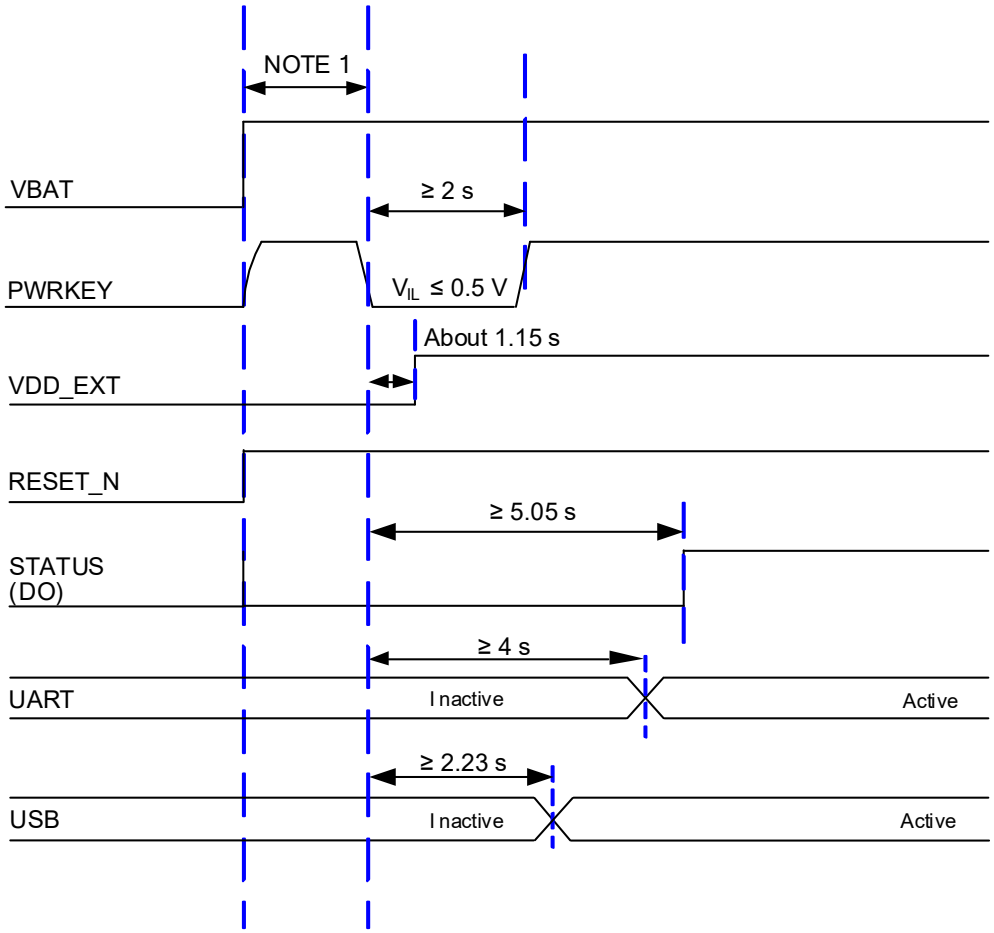


Figure 11: Turn-on Timing

NOTE

1. Please make sure that VBAT is stable before PWRKEY is pulled down. It is recommended that the time interval between powering up VBAT and pulling down PWRKEY is not less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a resistor of less than 1 kΩ if the module needs being powered on automatically and shutdown is not needed.
3. Pay special attention to the following two power-on scenarios:
   - In the scenario where USB_VBUS is connected first (or always connected), VBAT is powered on later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that VBAT is powered on stably for at least 2 s before PWRKEY is pulled down;
   - In the scenario where VBAT is powered on first (or always powered on), USB_VBUS is connected later, and then PWRKEY is pulled down to start up the module, it is necessary to ensure that USB_VBUS is connected for at least 2 s before PWRKEY is pulled down.

3.7.2. Turn Off Module

The following ways can be used to turn off the module:

- Turn off the module with PWRKEY.
- Turn off the module by using *ql_power_down()*. See ***document [5]*** for details on the API.

3.7.2.1. Turn Off Module with PWRKEY

Drive PWRKEY low for at least 3 s and release it, and the module will execute power-down procedure.

The turn-off timing is illustrated in the following figure.

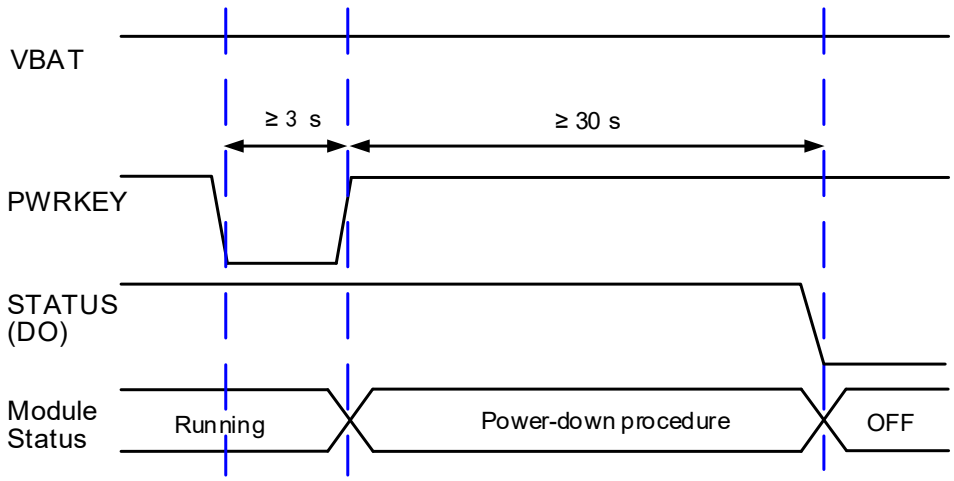


Figure 12: turn-off Timing

3.7.2.2. Turn Off Module with ql_power_down()

It is also a safe way to use *ql_power_down()* to turn off the module, which is similar to the procedure of turning off the module via PWRKEY.

NOTE

1. To avoid corrupting the data in the internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or *ql_power_down()* can the power supply be cut off.
2. When keeping the PWRKEY to the ground, the module will not boot automatically after being turned off with the AT command. In this case, it is necessary to forcibly disconnect the VBAT power supply and turn on the module again. Therefore, it is recommended that you can turn on or turn off the module by controlling the PWEKEY instead of keeping the PWRKEY to the ground.
3. When being turned off, the module will log out of the network. The time for logging out relates to its network status. Thus, please pay attention to the shutdown time in your design because the actual shutdown time varies with the network status.
4. If you disconnect the VBAT power supply, ensure that the VBAT pins' voltage is less than 0.5 V before powering it on again.

3.7.3. Reset Module

The RESET_N can be used to reset the module. The module can be reset by driving RESET_N low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, and so it is recommended to route the trace as short as possible and surround the trace with ground.

Table 9: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	VBAT power domain. Active low. A test point is recommended to be reserved.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

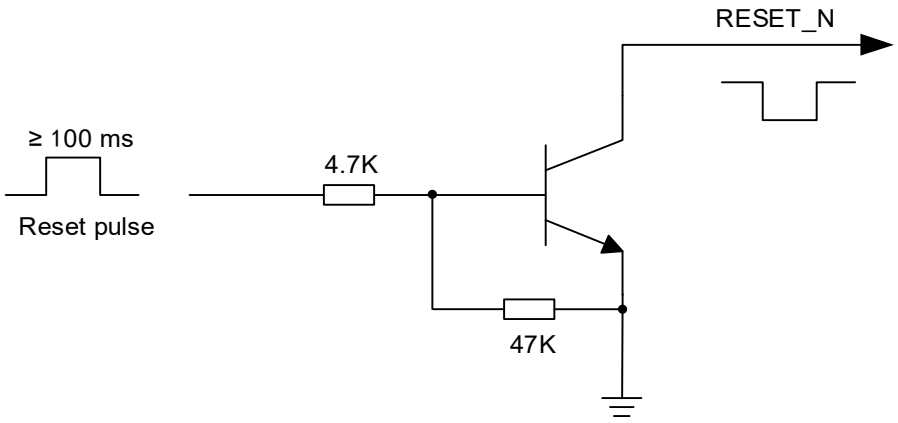


Figure 13: Reference Circuit of RESET_N by Using Driving Circuit

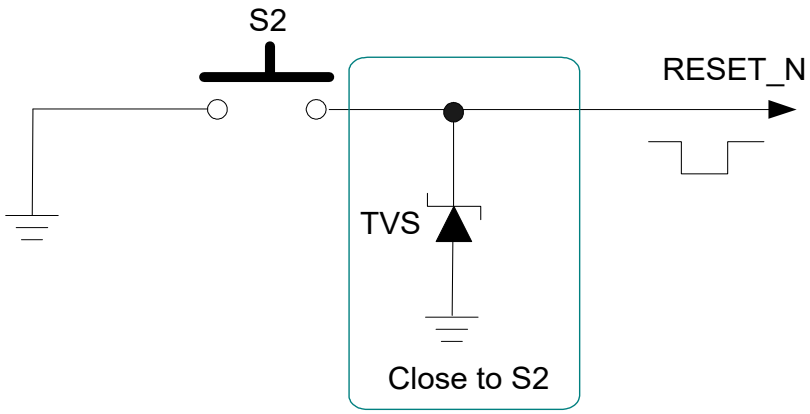


Figure 14: Reference Circuit of RESET_N by Using Button

The timing of resetting module is illustrated in the following figure.

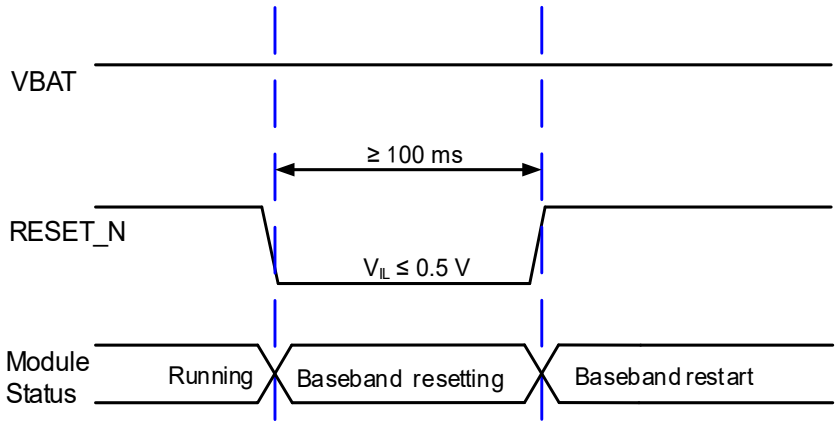


Figure 15: Timing of Resetting Module

NOTE

1. Ensure the load capacitance on PWRKEY and RESET_N does not exceed 10 nF.
2. It is recommended to use RESET_N only when the module cannot be turned off by *ql_power_down()* or PWRKEY.

3.8. (U)SIM Interfaces

The module provides two (U)SIM interfaces, and it supports DSDS function. The (U)SIM interfaces meet ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 10: Pin Definition of (U)SIM1 Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM_DATA	15	DIO	(U)SIM1 card data	
USIM_CLK	16	DO	(U)SIM1 card clock	
USIM_RST	17	DO	(U)SIM1 card reset	
USIM_DET	13	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM_GND	10		(U)SIM1 card GND	Connect to the GND of (U)SIM card connector.

Table 11: Pin Definition of Multiplexed (U)SIM2 Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM2_VDD	128	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM is supported and can be identified by the module automatically.
AP_READY	2	DIO	(U)SIM2 card data	The relevant functions of the (U)SIM2 card can be realized by multiplexing AP_READY, WAKEUP_IN, SLEEP_IND, and W_DISABLE#.
WAKEUP_IN	1	DO	(U)SIM2 card clock	
W_DISABLE#	4	DO	(U)SIM2 card reset	

SLEEP_IND	3	DI	(U)SIM2 card hot-plug detect	For details, please consult Quectel Technical Support.

The module supports (U)SIM card hot-plug via the USIM_DET. For details about how to configure the hot-plug function, see the *ql_sim_demo.c* in the CSDK. For details about pin multiplexing of the module, see ***document [2]***.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

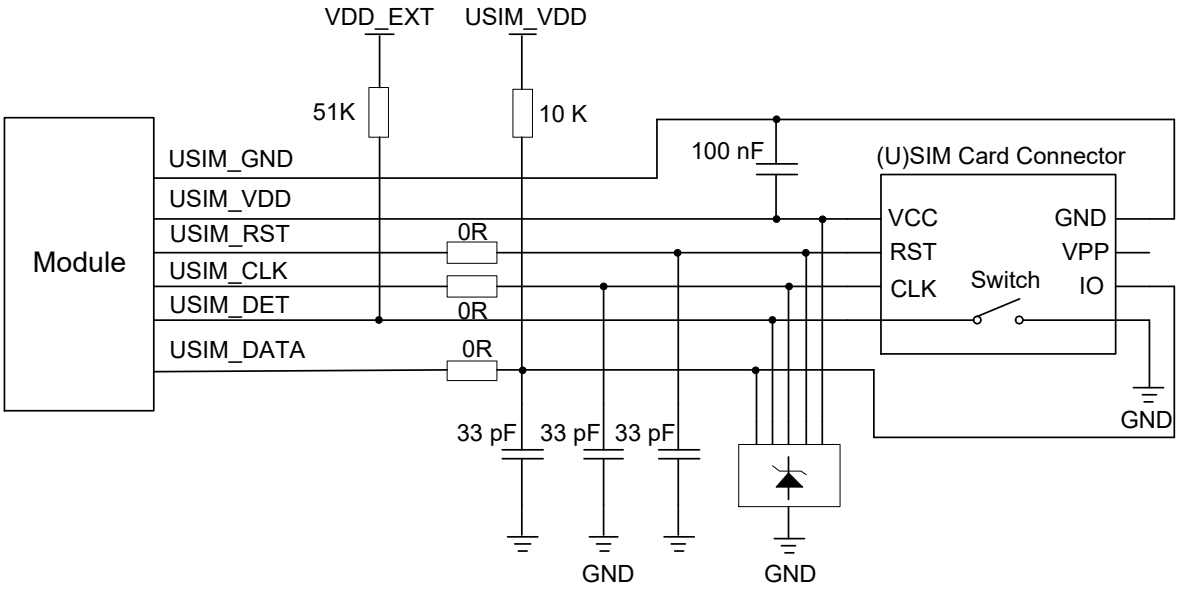


Figure 16: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

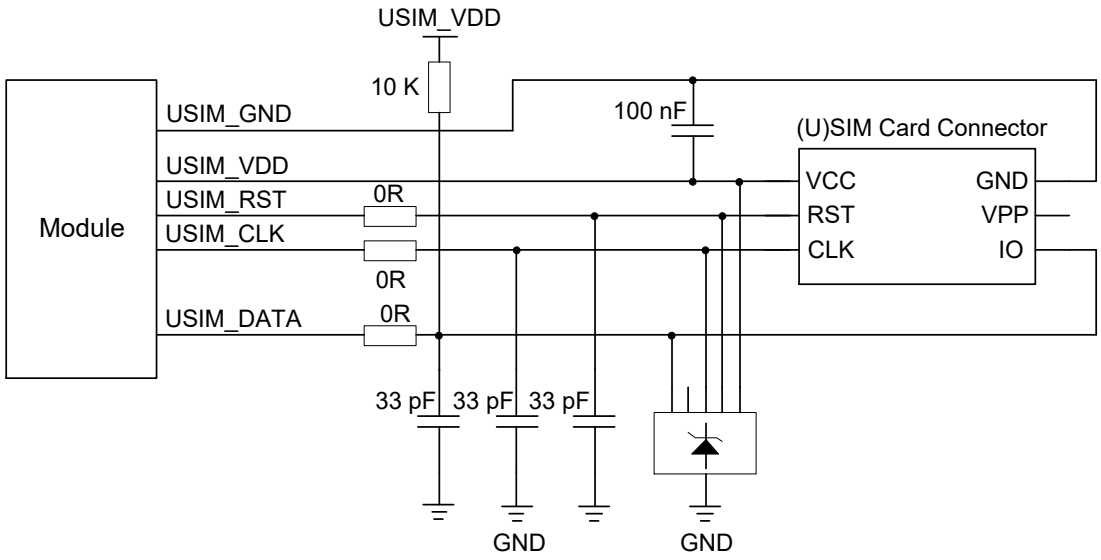


Figure 17: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in your applications, please follow the criteria below in (U)SIM circuit design:

- Place (U)SIM card connector as close to the module as possible. Keep the trace length at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Keep the trace between the ground of (U)SIM card connector and USIM_GND short and wide. Keep the trace width of USIM_GND and USIM_VDD not less than 0.5 mm to maintain the same electric potential. If the ground is complete on your PCB, USIM_GND can be connected to PCB ground directly.
- Ensure that the capacitance of the bypass capacitor between USIM_VDD and GND is not greater than 1 μF, and the capacitor should be close to the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS array whose parasitic capacitance should not exceed 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors on USIM_DATA, USIM_CLK and USIM_RST are used for filtering RF interference. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

3.9. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. The USB interface only supports USB slave mode and it can be used for data transmission, software debugging and firmware upgrade.

Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	AIO	USB 2.0 differential data (+)	Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	70	AIO	USB 2.0 differential data (-)	
USB_VBUS	71	AI	USB connection detect	Typical 5.0 V. Minimum 3.5 V. A test point must be reserved.
GND	72		Ground	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

Reserve test points for debugging and firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

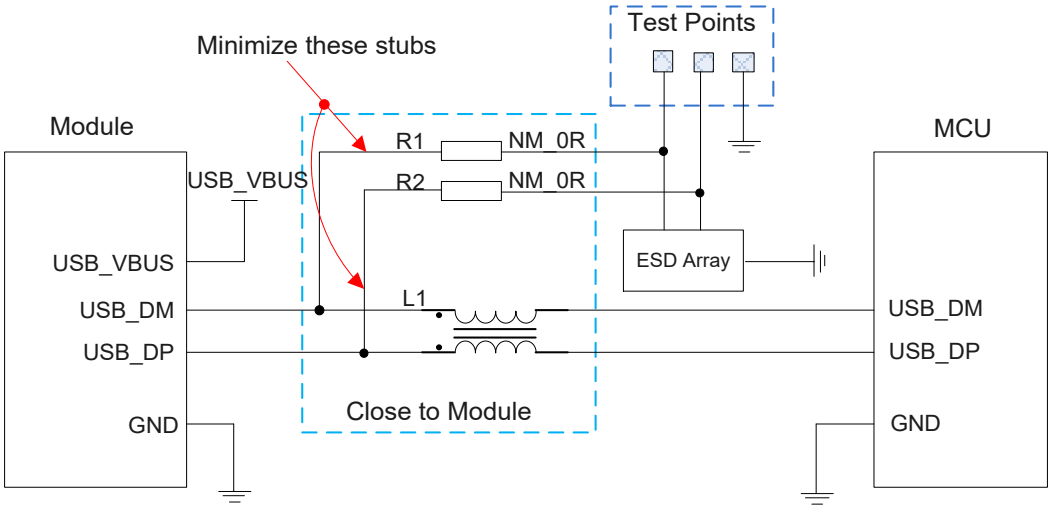


Figure 18: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU in order to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not

mounted by default. In order to ensure the integrity of USB data line signal, L1, R1 and R2 components must be placed close to the module, and these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when designing the USB interface, so as to meet USB 2.0 specification.

- Route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is recommended to route the USB differential traces in inner-layer of the PCB and to surround the traces with ground on that layer and with ground planes above and below.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance should be at most 2.0 pF, and keep the ESD protection components to the USB connector as close as possible.

3.10. UART Interfaces

The module provides three UART interfaces: the main UART interface, the debug UART interface and auxiliary UART Interface. The following shows their features.

- Main UART interface: This interface is used for data transmission and supports RTS and CTS hardware flow control.
- Debug UART interface: It is used for AP log output and can only be used as a debug UART.
- Auxiliary UART Interface

Table 13: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	64	DO	Clear to send signal from the module (Connect to the MCU's CTS)	1.8 V power domain. If unused, keep them open.
MAIN_RTS	65	DI	Request to send signal to the module (Connect to the MCU's RTS)	
MAIN_TXD	67	DO	Main UART transmit	
MAIN_RXD	68	DI	Main UART receive	

Table 14: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	12	DO	Debug UART transmit	1.8 V power domain. Test points must be reserved to capture AP log.
DBG_RXD	11	DI	Debug UART receive	

Table 15: Pin Definition of Auxiliary UART Interface

Pin Name	Pin No.	I/O	Description	Comment
AUX_TXD	138	DO	Auxiliary UART transmit	1.8 V power domain. If unused, keep them open.
AUX_RXD	137	DI	Auxiliary UART receive	

The module provides 1.8 V UART interface. A voltage-level translator should be used if the application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0104EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

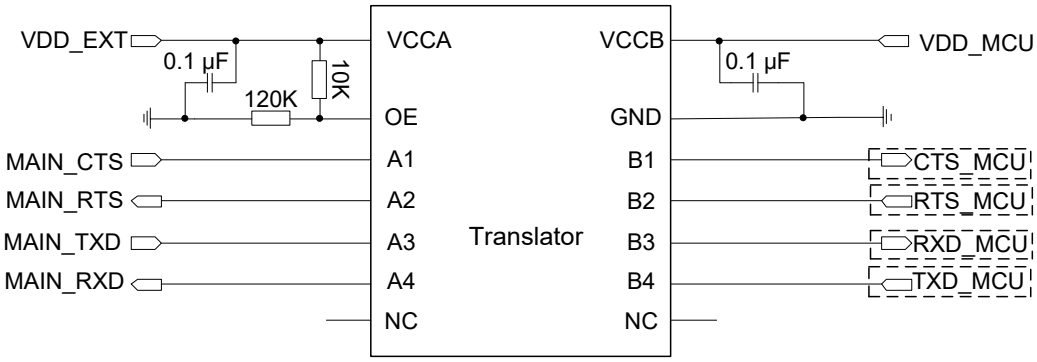


Figure 19: Reference Circuit with Voltage-level Translator

Please visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, please refer to that shown in solid lines, but pay attention to the direction of connection.

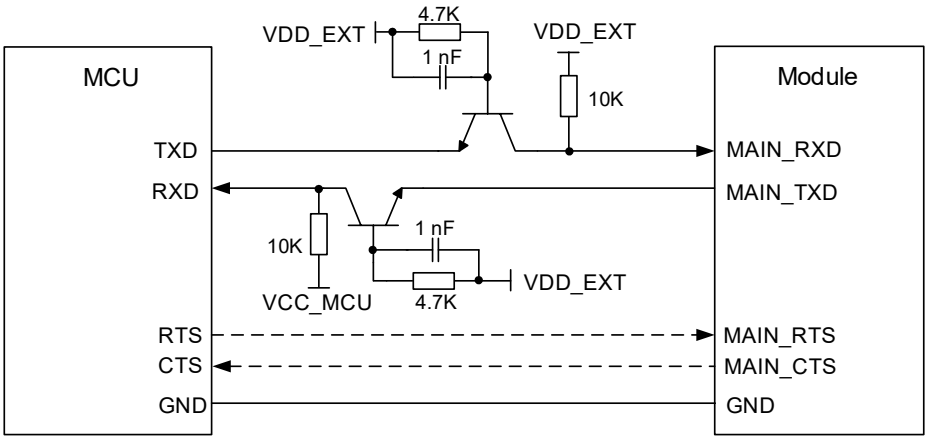


Figure 20: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the MCU CTS, and the module RTS is connected to the MCU RTS.
3. If the selected module does not support GNSS function, it can support UART3 function. For details, please consult Quectel Technical Support.

3.11. SPI Interface

The SPI interface of the module only supports master mode. It allows the full-duplex synchronous communication between module and peripherals. Its working voltage is 1.8 V, and the maximum clock frequency is 25 MHz.

Table 16: Pin Definition of SPI interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CS	37	DO	SPI chip select	If the module model you choose supports GNSS function, the SPI function cannot be used and pins 37–40 need to be left unconnected.
SPI_DOUT	38	DO	SPI data output	
SPI_DIN	39	DI	SPI data input	
SPI_CLK	40	DO	SPI clock	

NOTE

1. When the general 4-wire SPI interface is used for connecting external NOR flash, it supports basic flash operations such as read, write and erase, file systems, wear leveling, FOTA upgrade and preset files. It can be used only for storage purpose and cannot be used to run code.
2. When the general 4-wire SPI interface is used for connecting external NAND flash, it supports basic flash operations such as read, write and erase, file systems and wear leveling. It does not support FOTA upgrade and preset files. it can be used only for storage purpose and cannot be used to run code.

3.12. I2C Interfaces

The module provides two I2C interfaces.

Table 17: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	41	OD	I2C serial clock	Require external pull-up to 1.8 V if used. If unused, keep them open.
I2C_SDA	42	OD	I2C serial data	
I2C2_SCL	141	OD	I2C serial clock	
I2C2_SDA	142	OD	I2C serial data	

NOTE

The I2C bus supports simultaneous connection of multiple peripherals except for codec IC. In other words, if a codec IC has been mounted on the I2C bus, no other peripherals can be mounted. If there is no codec IC on the bus, multiple peripherals can be mounted.

3.13. PCM Interface

The module provides one pulse code modulation (PCM) interface for connecting an external codec IC. The PCM interface only supports slave mode; therefore, the clock signal of the codec IC needs to be provided externally. It is recommended to use the module's MAIN_DCD to provide the clock signal.

Table 18: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	24	DI	PCM data input	1.8 V power domain. If unused, keep them open.
PCM_DOUT	25	DO	PCM data output	
PCM_SYNC	26	DI	PCM data frame sync	1.8 V power domain. If unused, keep them open. The PCM function only supports slave mode.
PCM_CLK	27	DI	PCM clock	

The following figure shows a reference design of I2C and PCM interfaces with an external codec IC.

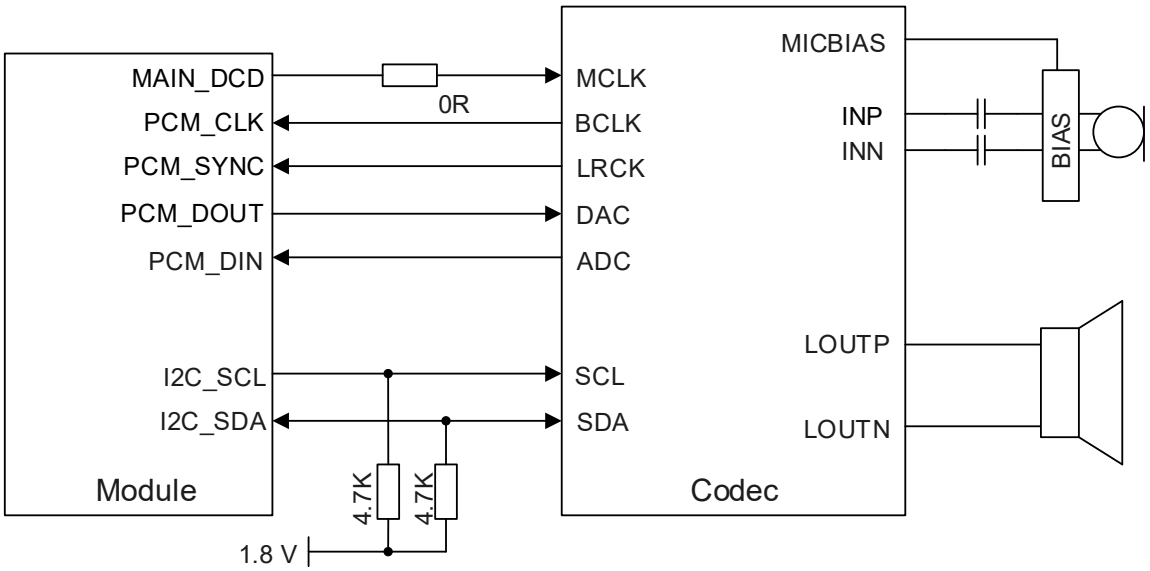


Figure 21: Reference Circuit of I2C and PCM Application with Audio Codec

NOTE

1. It is recommended to reserve an RC (R = 0 Ω, C = 33 pF) circuit on the PCM traces, especially for PCM_CLK.
2. If the module's MAIN_DCD pin is used for providing clock signal, it cannot be used for other purpose.

3.14. External Flash Interface

The module supports an external flash chip, and the external flash interface is multiplexed with other pins of the module. For details, see the following table:

Table 19: Pin Definition of Multiplexed External Flash Interface

Pin Name	Pin No.	Alternate Function	I/O	Comment
PCM_DIN	24	SPI_FLASH1_SIO_0	DIO	Connect to IO0 of the external flash chip
PCM_DOUT	25	SPI_FLASH1_SIO_1	DIO	Connect to IO1 of the external flash chip
PCM_SYNC	26	SPI_FLASH1_CS	DO	Connect to CS of the external flash chip
PCM_CLK	27	SPI_FLASH1_CLK	DO	Connect to CLK of the external flash chip
USIM_DET	13	SPI_FLASH1_SIO_2	DIO	Connect to IO2 of the external flash chip
WLAN_WAKE	135	SPI_FLASH1_SIO_3	DIO	Connect to IO3 of the external flash chip

Pins 24–27, 13, 135 can be multiplexed into a set of dedicated SPI for connecting external 6-wire NOR flash or NAND flash. The difference between them is as follows:

- When the dedicated SPI interface is used for connecting external NOR flash, it supports file system, wear leveling, FOTA upgrade and preset files. It can be used only for storage purpose and cannot be used to run code.
- When the dedicated SPI interface is used for connecting external NAND flash, it supports basic flash operations such as read, write and erase, file systems and wear leveling. It does not support FOTA upgrade and preset files. it can be used only for storage purpose and cannot be used to run code.

See ***document [6]*** for the detailed circuit design of the above interfaces.

NOTE

1. Pins 24–27 can also be multiplexed into a general SPI for connecting external 4-wire flash and other peripherals.
2. For GPIO configuration, see ***document [2]***.

3.15. Analog Audio Interfaces

The module provides one analog audio input channel and one analog audio output channel. The pin definition is shown in the table below.

Table 20: Pin Definition of Analog Audio Interfaces

Interface	Pin Name	Pin No.	I/O	Description
AOUT	LOUDSPK_P	73	AO	Loudspeaker differential output (+)
	LOUDSPK_N	74	AO	Loudspeaker differential output (-)
AIN	MIC_P	75	AI	Microphone analog input (+)
	MIC_N	77	AI	Microphone analog input (-)

- AIN channel is a differential input channel, which can be applied for input of microphone (usually an electret microphone).
- The AOUT channel is a differential output channel built with a power amplifier. The default configuration of power amplifier is Class AB and the maximum driving power is 500 mW for 8 Ω load. When PA is configured as Class D, the maximum driving power is 800 mW for 8 Ω load.

3.15.1. Notes on Audio Interface Design

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. Without placing this capacitor, TDD noise could be heard during the call. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you would have to discuss with your capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

For models that support GSM, the severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required. The filter capacitor on the PCB should be placed near the audio devices or audio interfaces as close as possible, and the traces should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To decrease signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

3.15.2. Microphone Interface Circuit

The reference circuit of the microphone interface is shown in the figure below:

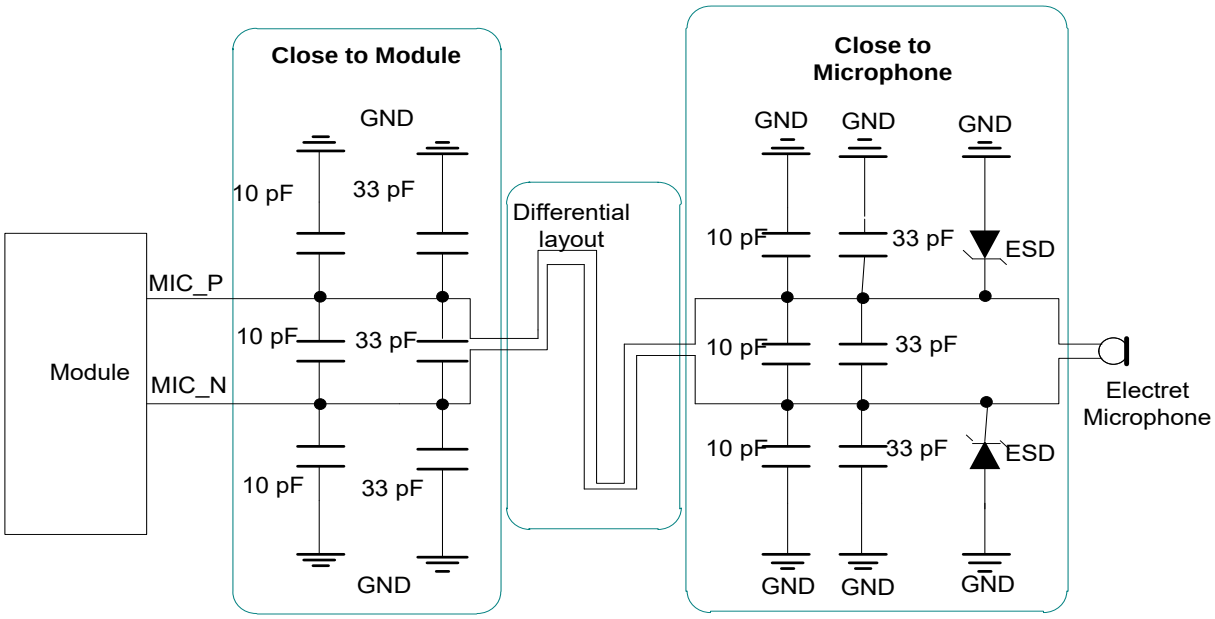


Figure 22: Reference Circuit of Microphone Interface

NOTE

Microphone channel is sensitive to ESD, so it is not recommended to remove the ESD components used for protecting the microphone.

3.15.3. Loudspeaker Interface Circuit

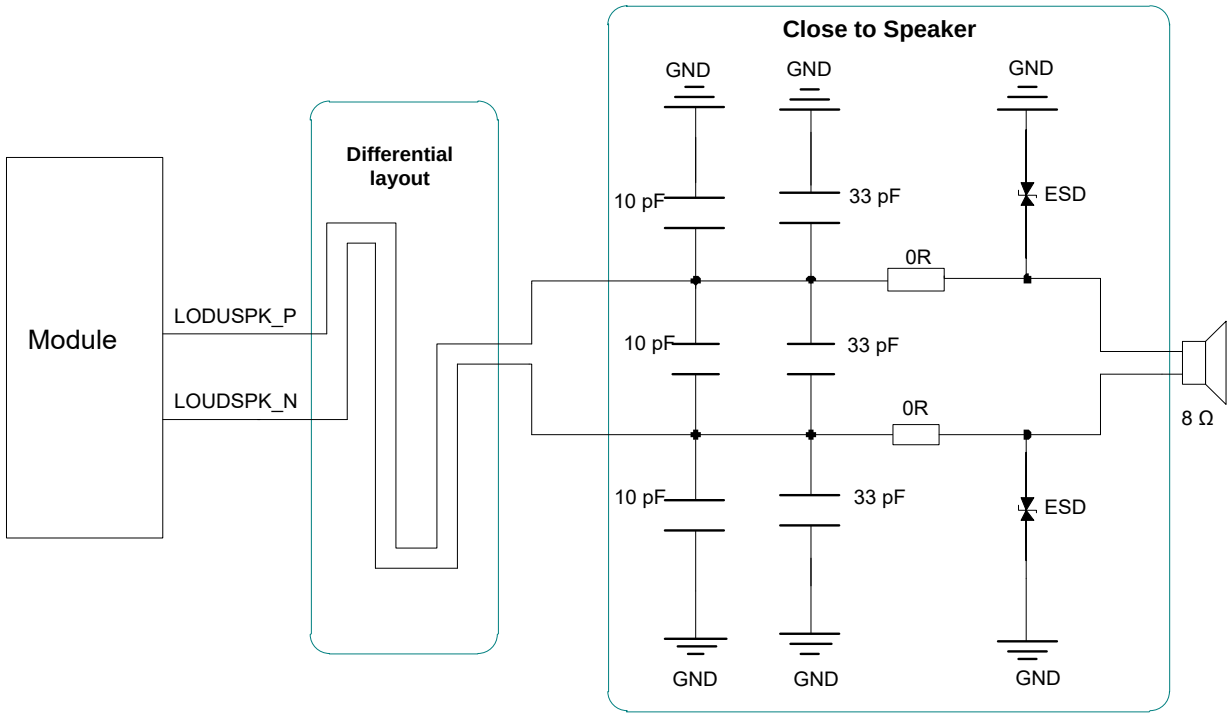


Figure 23: Reference Circuit of Loudspeaker Interface

3.16. LCM Interface

The LCM interface supports both SPI and MIPI modes. SPI LCM interface supports a liquid crystal display with a maximum resolution of 320 × 240 and supports DMA transmission, 16-bit RGB565 and YUV formats. The MIPI LCM interface supports the liquid crystal display with a maximum resolution of 800 × 1280. See ***document [6]*** for the circuit design of SPI LCM and MIPI LCM.

For GPIO configurations, see ***document [2]***.

Table 21: Pin Definition of SPI LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_FMARK	119	DI	LCD frame synchronization	1.8 V power domain. If unused, keep them open.
LCD_RSTB	120	DO	LCD reset	

LCD_SEL	121		Reserved	
LCD_CS	122	DO	LCD chip select	
LCD_CLK	123	DO	LCD clock	
LCD_SDC	124	DO	LCD register selection	
LCD_SI/O	125	DIO	LCD data	
ISINK	140	PI	Sink current input. Backlight adjustment	Imax = 200 mA. The current is configurable. It is driven by the current sink, and connected to the backlight cathode. The brightness can be adjusted with current control.

Table 22: Pin Definition of Multiplexed MIPI LCM Interface

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
LCD_RSTB	120		DO	LCD reset	1.8 V power domain. If unused, keep them open.
LCD_FMARK	119		DI	LCD frame synchronization	
PCM_DOUT	25	DSI_D1P	DIO	MIPI differential data (+)	
PCM_DIN	24	DSI_D1N	DIO	MIPI differential data (-)	
WLAN_WAKE	135	DSI_D0P	DIO	MIPI differential data (+)	
USIM_DET	13	DSI_D0N	DIO	MIPI differential data (-)	
PCM_SYNC	26	DSI_CKP	DIO	MIPI differential clock (+)	
PCM_CLK	27	DSI_CKN	DIO	MIPI differential clock (-)	

3.17. Camera

The module supports the camera interface with only 1.8 V I/O interface is supported. The camera interface is multiplexed with other pins and can support up to 0.3 megapixel cameras. It supports the two-data-line transmission of SPI and MIPI data transmission. For GPIO configurations, see ***document [2]***.

Table 23: Pin Definition of Multiplexed SPI Camera Interface

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
SD_DET	23	CAM_SCK	DI	Camera SPI clock	1.8 V power domain.
STATUS	61	CAM_RST	DO	Camera reset	
MAIN_RI	62	CAM_PWDN	DO	Camera power down	
MAIN_DCD	63	CAM_REFCLK	DO	Camera main clock	
MAIN_DTR	66	CAM_DATA0	DIO	Camera SPI data 0	
NET_STATUS	6	CAM_DATA1	DIO	Camera SPI data 1	

Table 24: Pin Definition of Multiplexed MIPI Camera Interface

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
I2C_SDA	42		OD	Camera I2C data	Pull each of them up to 1.8 V power domain with an external resistor. If unused, keep them open.
I2C_SCL	41		OD	Camera I2C clock	
MAIN_RI	62	CAM_PWDN	DO	Camera power down	1.8 V power domain. If unused, keep them open.
MAIN_DCD	63	CAM_REFCLK	DO	Camera master clock	
STATUS	61	CSI_CKN	DIO	MIPI differential clock (-)	
MAIN_DTR	66	CSI_CKP	DIO	MIPI differential clock (+)	
NET_STATUS	6	CSI_D0N	DIO	MIPI differential data (-)	
SD_DET	23	CSI_D0P	DIO	MIPI differential data (+)	

3.18. Matrix Keypad Interface

The module provides one matrix keypad interface. Since GNSS function is optional, you can use 4 × 6 matrix keypad with pins 81 and 82 connected for the module without GNSS, and 4 × 4 matrix keypad for the module with GNSS (pins 81 and 82 are kept open).

Table 25: Pin Definition of Matrix Keypad Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Matrix keypad input 0	USB_BOOT can be used as KEYIN0 after startup. It cannot be pulled up before startup, otherwise the module will enter download mode.
KEYIN1	78	DI	Matrix keypad input 1	1.8 V power domain. If unused, keep it open. KEYIN1 cannot be pulled up before startup.
KEYIN2	79	DI	Matrix keypad input 2	1.8 V power domain. If unused, keep them open.
KEYIN3	80	DI	Matrix keypad input 3	
KEYOUT0	83	DO	Matrix keypad output 0	
KEYOUT1	84	DO	Matrix keypad output 1	
KEYOUT2	113	DO	Matrix keypad output 2	
KEYOUT3	114	DO	Matrix keypad output 3	
KEYOUT4	81	DO	Matrix keypad output 4	
KEYOUT5	82	DO	Matrix keypad output 5	

3.19. SD Card Interface

The module supports one SD card interface compliant with SD 2.0 protocol.

Table 26: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_DET	23	DI	SD card detect	1.8 V power domain. If unused, keep it open.
SDIO1_DATA3	28	DIO	SDIO data bit 3	3.2 V power domain. If unused, keep them open.
SDIO1_DATA2	29	DIO	SDIO data bit 2	
SDIO1_DATA1	30	DIO	SDIO data bit 1	

SDIO1_DATA0	31	DIO	SDIO data bit 0
SDIO1_CLK	32	DO	SDIO clock
SDIO1_CMD	33	DIO	SDIO command
SDIO1_VDD	34	PO	SDIO power supply

The following figure shows a reference design of SD card interface.

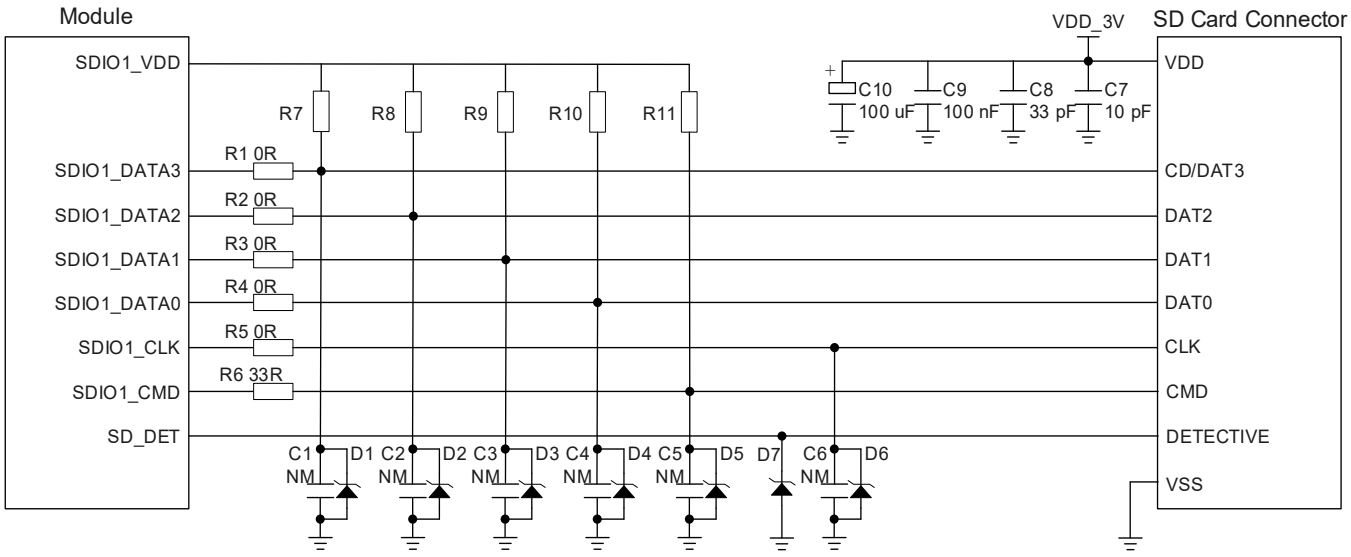


Figure 24: Reference Circuit of SD Card Interface

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- The voltage range of SD card power supply VDD_3 V provided externally is 2.7–3.6 V and a sufficient current of at least 0.8 A should be provided. The maximum output current of module's output power supply SDIO1_VDD is 150 mA and it can only be used for SDIO pull-up resistors.
- To avoid the jitter of bus, it is necessary to reserve pull-up resistors R7–R11 on the SDIO signal traces. The recommended value is 4.7 kΩ. The pull-up power supply should be the SDIO1_VDD of the module.
- To adjust signal quality, it is necessary to add resistors R1–R6 in series between the module and the SD card connector. The recommended value for R1–R5 is 0 Ω and for R6 is 33 Ω. The bypass capacitors C1–C6 are reserved and not mounted by default. The resistors and capacitors should be placed close to the module when placing the PCB.
- In order to offer good ESD protection, it is recommended to add TVS diodes with junction capacitance less than 15 pF on SD card pins near the SD card connector.

- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- It is important to route the SDIO signal surrounded with ground on the layer and ground planes above and below. The impedance of SDIO data trace is 50 Ω ±10 %.
- Make sure the adjacent trace spacing is more than twice the trace width and the load capacitance of SDIO bus should be less than 15 pF.
- It is recommended to keep the trace length difference between SDIO1_CLK and SDIO1_DATA [0:3]/ SDIO1_CMD less than 1 mm and the total routing length less than 50 mm.

3.20. WLAN Application Interface*

The module provides an SDIO 1.1 standard WLAN application interface.

Table 27: Pin Definition of WLAN Application Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SLP_CLK	118	DO	WLAN sleep clock	If unused, keep it open.
WLAN_PWR_EN	127	DO	WLAN power supply enable control	1.8 V power domain. If unused, keep them open.
SDIO2_DATA3	129	DIO	WLAN SDIO data bit 3	
SDIO2_DATA2	130	DIO	WLAN SDIO data bit 2	
SDIO2_DATA1	131	DIO	WLAN SDIO data bit 1	
SDIO2_DATA0	132	DIO	WLAN SDIO data bit 0	
SDIO2_CLK	133	DO	WLAN SDIO CLK	
SDIO2_CMD	134	DIO	WLAN SDIO command	
WLAN_WAKE	135	DI	Wake up the host (the module) by an external Wi-Fi module	1.8 V power domain. If unused, keep them open.
WLAN_EN	136	DO	WLAN function enable control	

The data rate of SDIO interface is very high. To ensure that the interface design complies with the SDIO 1.1 specification, the following principles should be complied with.

- It is important to route the SDIO signal surrounded with ground on the layer and ground planes above and below. The impedance of SDIO data trace is 50 Ω ±10 %.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- It is recommended to keep the trace length difference between WLAN_SLP_CLK, SDIO2_DATA [0:3] and SDIO2_CMD less than 1 mm and the total routing length less than 50 mm.
- Make sure the adjacent trace spacing is more than twice the trace width and the load capacitance of SDIO bus should be less than 15 pF.

NOTE

WLAN application interface conflicts with other functions, and please consult Quectel Technical Support for details.

3.21. ADC Interfaces

The module provides three ADC interfaces. In order to improve the measurement accuracy of ADC, the traces of ADC should be surrounded with ground.

Table 28: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description	Comment
ADC0	45	General-purpose ADC interface	It is recommended to reserve a divider circuit. If unused, keep them open.
ADC1	44	General-purpose ADC interface	
ADC2	43	General-purpose ADC interface	

Table 29: Characteristic of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC[0:2] Voltage Range	0	-	VBAT_BB	V
ADC Resolution	-	12	-	bits

You can use the *ql_adc_get_volt()* to read the voltage of an ADC interface. The mapping between *ql_adc_channel_id* and ADC channel is as follows:

Table 30: Mapping Between *q_adc_channel_id* and ADC Channel

ql_adc_channel_id	ADC Channel
QL_ADC0_CHANNEL	ADC0
QL_ADC1_CHANNEL	ADC1
QL_ADC2_CHANNEL	ADC2

NOTE

1. For details about the above API, please see ***document [7]***.
2. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins, it is strongly recommended to reserve the voltage divider circuit for better compatibility with other modules. The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADCs will be significantly reduced. When the divider circuit is not used, the ADC pins require 1 kΩ resistance in series.

3.22. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module has NET_MODE and NET_STATUS for network status indication. The following tables describe pin definition and logic level changes in different network status. See *led_cfg_demo.c* in the CSDK for details.

Table 31: Pin Definition of Network Status Indication

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network activity status	1.8 V power domain. If unused, keep them open.
NET_STATUS	6	DO	Indicate the module's network registration mode	

Table 32: Working State of Network Indication Pins

Pin Name	Logic Level Changes	Network Status
NET_STATUS	Always high	Registered on LTE network
	Always low	Others

NET_MODE	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker quickly (234 ms high/266 ms low)	Idle
	Flicker rapidly (63 ms high/62 ms low)	Data transfer is ongoing
	Always high	Voice calling

A reference circuit is shown in the following figure:

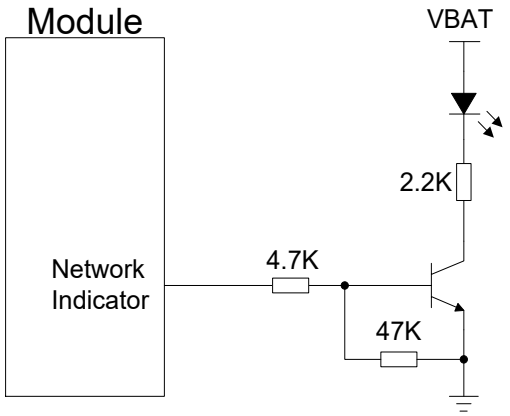


Figure 25: Reference Circuit of Network Status Indication

3.23. STATUS

The STATUS pin indicates the module's operation status. When the module is turned on normally, the STATUS outputs high level.

Table 33: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	DO	Indicate the module's operation status	1.8 V power domain. If unused, keep it open.

A reference circuit is shown in the following figure.

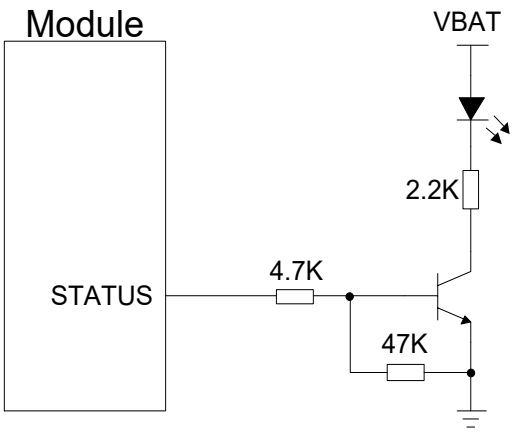


Figure 26: Reference Circuit of STATUS

NOTE

The STATUS cannot be used as the indication of power-down state when VBAT doesn't supply power to the module.

3.24. USB_BOOT Interface

The module provides a USB_BOOT pin. Pull up USB_BOOT to 1.8 V before VDD_EXT is powered up, and the module will enter download mode when it is powered on. In this mode, the module can upgrade firmware over USB interface.

If your application has a scan key, you can also press the "USB_BOOT + KEYOUT0" scan key before powering on the module, and the module will enter the download mode when it is turned on.

Table 34: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Control the module to enter download mode	1.8 V power domain. Active high. A test point is recommended to be reserved. A circuit that enables the module to enter the download mode must be reserved.

The following figure shows a reference circuit of USB_BOOT interface.

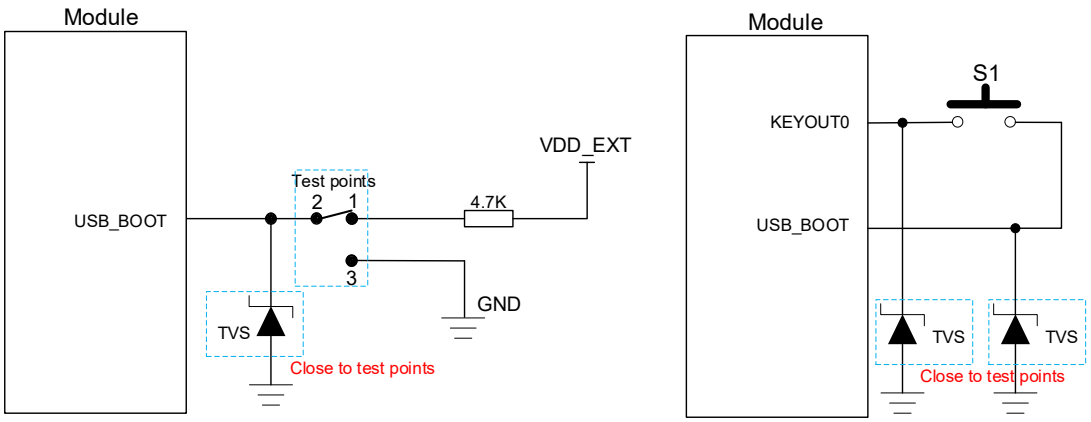


Figure 27: Reference Circuit of USB_BOOT Interface

4 Antenna Interfaces

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module provides a main antenna interface, a Wi-Fi Scan/Bluetooth antenna interface and a GNSS antenna interface. The antenna ports have an impedance of 50 Ω.

4.1. Main Antenna and Wi-Fi Scan/Bluetooth Antenna Interfaces

4.1.1. Pin Definition

The pin definition of main antenna and Wi-Fi Scan/Bluetooth antenna interfaces is shown below.

Table 35: Pin Definition of Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	AIO	Main antenna interface	50 Ω characteristic impedance.
ANT_BT/WIFI_SCAN [9]	35	AIO	The shared interface for Bluetooth and Wi-Fi Scan	Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan antenna can only receive but not transmit. 50 Ω characteristic impedance. If unused, keep it open.

[9] The module supports Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used at the same time; Bluetooth and Wi-Fi Scan functions are optional. Please contact Quectel Technical Support for details.

4.1.2. Operating Frequency

Table 36: EC200U-CN Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-TDD B34	2010–2025	2010–2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2535–2675	2535–2675	MHz

NOTE

The GSM network access technology of EC200U-CN is optional. If the module that you select doesn't support GSM network access technology, there is no corresponding frequency band.

Table 37: EC200U-EU Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz

LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

Table 38: EC200U-AU Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930-1990	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B28	703–748	758–803	MHz

LTE-FDD B66	1710–1780	2110–2180	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

4.1.3. Reference Design of RF Antenna Interfaces

A reference design of ANT_MAIN and ANT_BT/WIFI_SCAN is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

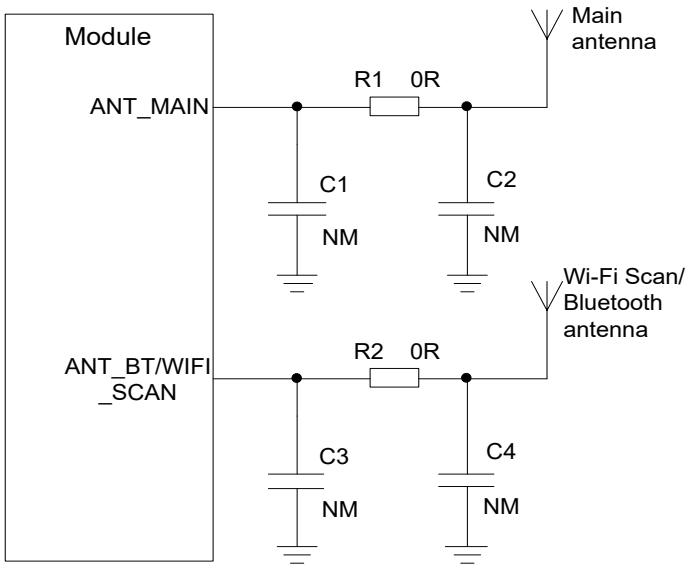


Figure 28: Reference Circuit of RF Antenna Interfaces

NOTE

1. In order to improve the receiving sensitivity, it is necessary to ensure the proper distance between the main antenna and Wi-Fi Scan/Bluetooth antenna.
2. Place the π-type matching components (R1 & C1 & C2 and R2 & C3 & C4) as close to the antenna as possible.

4.2. GNSS Antenna Interface

Table 39: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna interface	50 Ω characteristic impedance. If unused, keep it open.

Table 40: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz
QZSS	1575.42	MHz

A reference design of GNSS antenna is shown as below:

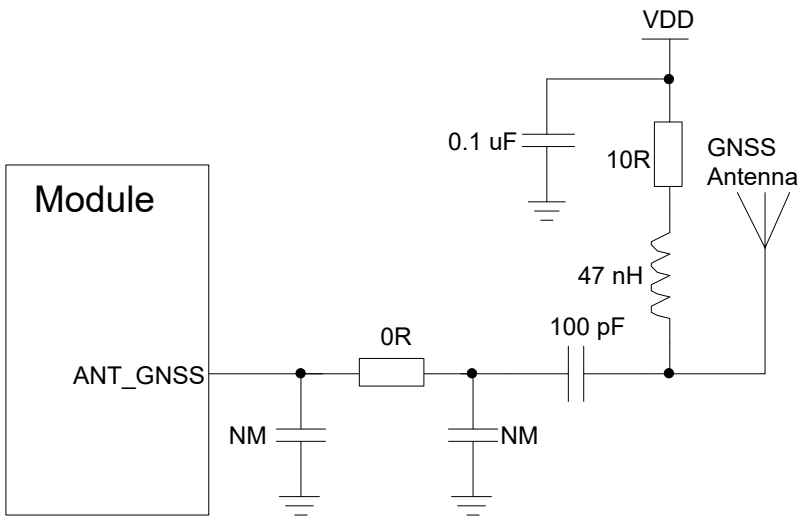


Figure 29: Reference Circuit of GNSS Antenna

NOTE

1. The VDD circuit is not needed if you use the passive antenna.
2. If an active antenna is needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design.

4.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

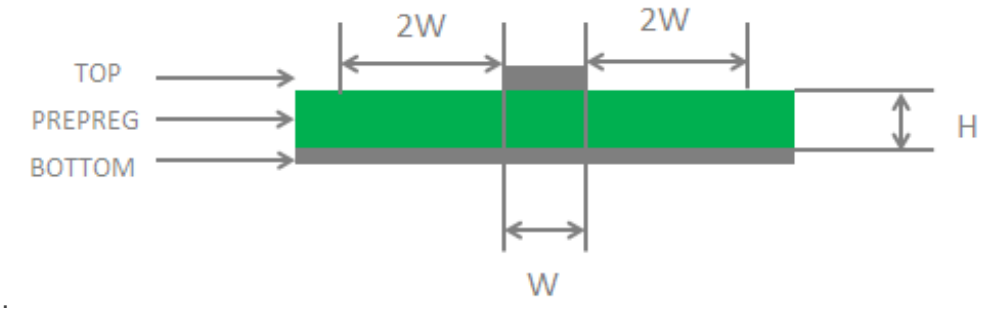


Figure 30: Microstrip Design on a 2-layer PCB

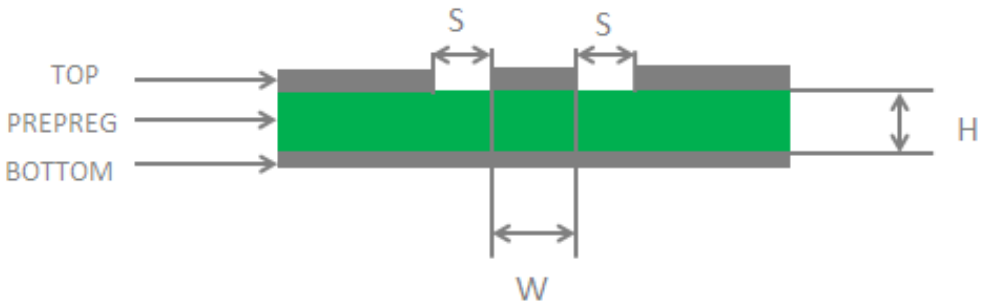


Figure 31: Coplanar Waveguide Design on a 2-layer PCB

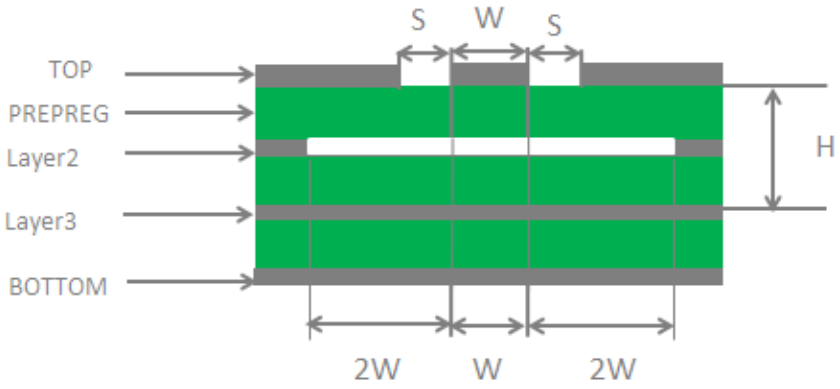


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

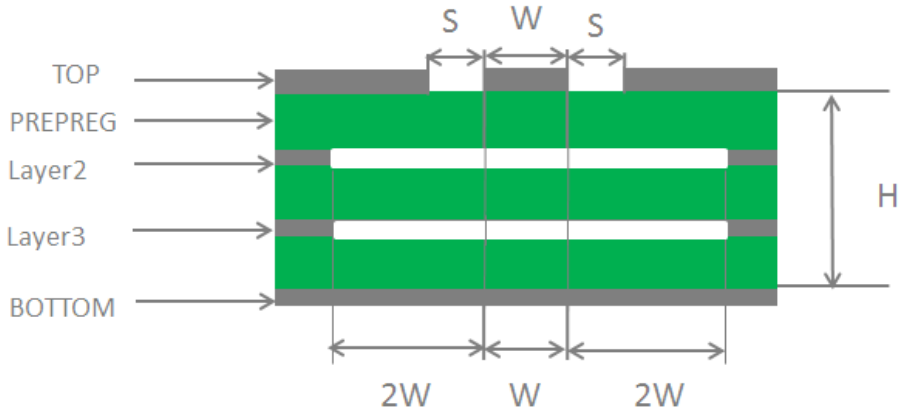


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [8]***.

4.4. Antenna Installation

4.4.1. Antenna Requirement

Table 41: Antenna Requirements

Type	Requirement
GNSS	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (typ.) Isolation from main antenna: > 40 dB
	For passive antenna usage: Passive antenna gain: > 0 dBi
	For active antenna usage: Active antenna noise factor: < 1.5 dB Active antenna gain: > 0 dBi Active antenna internal LNA gain: < 17 dB
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max. input power: 50 W Input impedance: 50 Ω < 1 dB: LB (< 1 GHz) < 1.5 dB: MB (1–2.3 GHz) < 2 dB: HB (> 2.3 GHz)

4.4.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

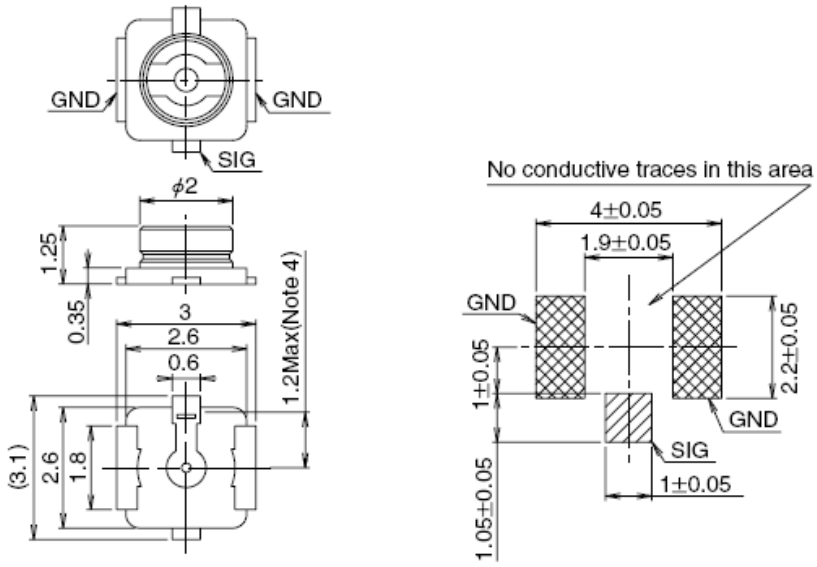


Figure 34: Dimensions of Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

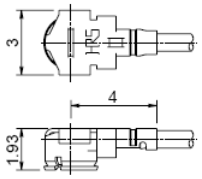
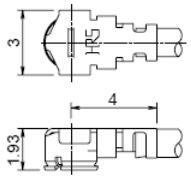
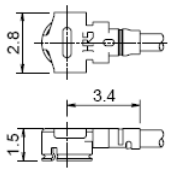
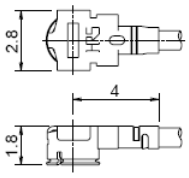
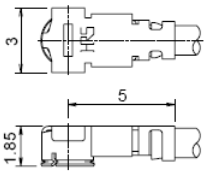
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 35: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors:

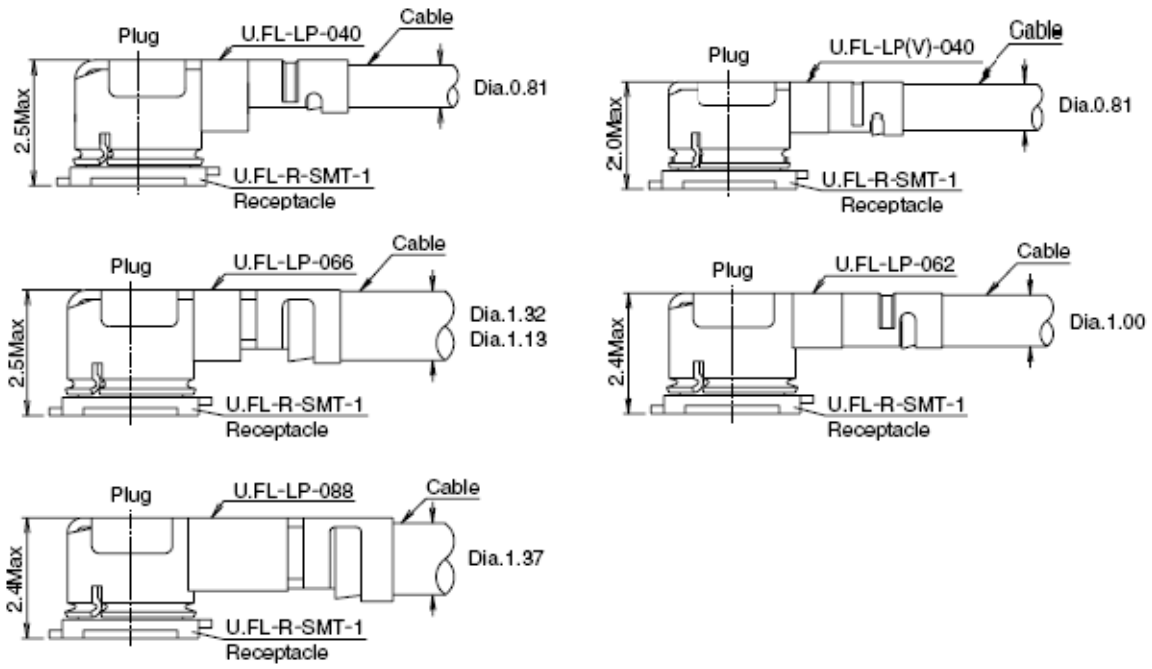


Figure 36: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://hirose.com.

5 Electrical Characteristics and Reliability

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 42: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	1.5	A
Peak Current of VBAT_RF	-	2.0	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC[0:2]	0	VBAT_BB	V

5.2. Power Supply Ratings

Table 43: Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum	3.3	3.8	4.3	V

		and maximum value.				
	Voltage drop during burst transmission	Maximum power control level	-	-	400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level	-	1.8	2.0/3.0	A
USB_VBUS	USB connection detection	-	3.5	5.0	5.25	V

NOTE

The power supply should be able to provide sufficient current of at least 2.0 A to the module that only supports LTE network, while at least 3.0 A should be provided for the module supporting GSM network.

5.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 44: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [10]	-35	+25	+75	℃
Extended Temperature Range [11]	-40	-	+85	℃
Storage Temperature Range	-40	-	+90	℃

[10] Within the operating temperature range, the module meets 3GPP specifications.
[11] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

5.4. Power Consumption

Table 45: EC200U-CN Current Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	32	μA
Sleep state	Minimum functionality mode (USB disconnected)	0.972	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.02	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.46	mA
	EGSM900 @ DRX = 5 (USB suspended)	2.90	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.30	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.00	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.46	mA
	DCS1800 @ DRX = 5 (USB suspended)	2.89	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.30	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.64	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.85	mA
	LTE-FDD @ PF = 64 (USB suspended)	3.41	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.46	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.26	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.70	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.97	mA
	LTE-TDD @ PF = 64 (USB suspended)	3.47	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.56	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.24	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	13.26	mA

	EGSM900 @ DRX = 5 (USB connected)	28.41	mA
	LTE-FDD @ PF = 64 (USB disconnected)	13.20	mA
	LTE-FDD @ PF = 64 (USB connected)	28.42	mA
	LTE-TDD @ PF = 64 (USB disconnected)	13.38	mA
	LTE-TDD @ PF = 64 (USB connected)	28.58	mA
GPRS data transfer (GNSS Off)	EGSM900 4DL/1UL @ 32.49 dBm	217	mA
	EGSM900 3DL/2UL @ 30.87 dBm	339	mA
	EGSM900 2DL/3UL @ 28.8 dBm	391	mA
	EGSM900 1DL/4UL @ 26.74 dBm	411	mA
	DCS1800 4DL/1UL @ 29.44 dBm	146	mA
	DCS1800 3DL/2UL @ 27.91 dBm	220	mA
	DCS1800 2DL/3UL @ 25.93 dBm	249	mA
	DCS1800 1DL/4UL @ 23.89 dBm	260	mA
LTE data transfer (GNSS Off)	LTE-FDD B1 @ 22.63 dBm	652	mA
	LTE-FDD B3 @ 22.73 dBm	630	mA
	LTE-FDD B5 @ 22.61 dBm	547	mA
	LTE-FDD B8 @ 22.21 dBm	545	mA
	LTE-TDD B34 @ 22.68 dBm	272	mA
	LTE-TDD B38 @ 22.94 dBm	352	mA
	LTE-TDD B39 @ 22.79 dBm	285	mA
	LTE-TDD B40 @ 23.37 dBm	461	mA
	LTE-TDD B41 @ 22.88 dBm	357	mA
GSM voice call	EGSM900 PCL = 5 @ 32.41 dBm	237	mA
	EGSM900 PCL = 12 @ 19.04 dBm	91	mA
	EGSM900 PCL = 19 @ 5.73 dBm	62	mA

	DCS1800 PCL = 0 @ 29.45 dBm	161	mA
	DCS1800 PCL = 7 @ 15.87 dBm	75	mA
	DCS1800 PCL = 15 @ 0.51 dBm	58	mA

NOTE

The GSM network access technology of EC200U-CN is optional. If the module that you select doesn't support GSM network access technology, there is no corresponding current consumption.

Table 46: EC200U-EU Current Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	40	μA
Sleep state	Minimum functionality mode (USB disconnected)	1.68	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.70	mA
	EGSM900 @ DRX = 5 (USB disconnected)	2.15	mA
	EGSM900 @ DRX = 5 (USB suspended)	3.56	mA
	EGSM900 @ DRX = 9 (USB disconnected)	2.02	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.66	mA
	DCS1800 @ DRX = 5 (USB disconnected)	2.16	mA
	DCS1800 @ DRX = 5 (USB suspended)	3.55	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.90	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.49	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.85	mA
	LTE-FDD @ PF = 64 (USB suspended)	3.24	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.52	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.35	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.55	mA

	LTE-TDD @ PF = 64 (USB disconnected)	1.87	mA
	LTE-TDD @ PF = 64 (USB suspended)	3.29	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.54	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.37	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	13.01	mA
	EGSM900 @ DRX = 5 (USB connected)	28.94	mA
	LTE-FDD @ PF = 64 (USB disconnected)	12.68	mA
	LTE-FDD @ PF = 64 (USB connected)	27.92	mA
	LTE-TDD @ PF = 64 (USB disconnected)	12.70	mA
	LTE-TDD @ PF = 64 (USB connected)	27.95	mA
GPRS data transfer (GNSS Off)	GSM850 4DL/1UL @ 32.30 dBm	243	mA
	GSM850 3DL/2UL @ 30.74 dBm	377	mA
	GSM850 2DL/3UL @ 28.69 dBm	438	mA
	GSM850 1DL/4UL @ 26.44 dBm	452	mA
	EGSM900 4DL/1UL @ 32.34 dBm	210	mA
	EGSM900 3DL/2UL @ 30.91 dBm	335	mA
	EGSM900 2DL/3UL @ 28.80 dBm	380	mA
	EGSM900 1DL/4UL @ 26.73 dBm	402	mA
	DCS1800 4DL/1UL @ 29.32 dBm	138	mA
	DCS1800 3DL/2UL @ 27.88 dBm	207	mA
	DCS1800 2DL/3UL @ 25.74 dBm	229	mA
	DCS1800 1DL/4UL @ 23.75 dBm	239	mA
	PCS1900 4DL/1UL @ 28.82 dBm	136	mA
	PCS1900 3DL/2UL @ 27.80 dBm	215	mA
	PCS1900 2DL/3UL @ 25.79 dBm	247	mA

	PCS1900 1DL/4UL @ 23.79 dBm	260	mA
LTE data transfer (GNSS Off)	LTE-FDD B1 @ 23.37 dBm	591	mA
	LTE-FDD B3 @ 22.76 dBm	578	mA
	LTE-FDD B5 @ 22.73 dBm	575	mA
	LTE-FDD B7 @ 22.24 dBm	735	mA
	LTE-FDD B8 @ 22.60 dBm	559	mA
	LTE-FDD B20 @ 24.05 dBm	581	mA
	LTE-FDD B28 @ 23.96 dBm	591	mA
	LTE-TDD B38 @ 22.32 dBm	303	mA
	LTE-TDD B40 @ 22.97 dBm	287	mA
	LTE-TDD B41 @ 22.60 dBm	330	mA
GSM voice call	GSM850 PCL = 5 @ 32.21 dBm	259	mA
	GSM850 PCL = 12 @ 19.21 dBm	97	mA
	GSM850 PCL = 19 @ 5.74 dBm	62	mA
	EGSM900 PCL = 5 @ 32.26 dBm	231	mA
	EGSM900 PCL = 12 @ 18.90 dBm	89	mA
	EGSM900 PCL = 19 @ 5.97 dBm	61	mA
	DCS1800 PCL = 0 @ 29.36 dBm	153	mA
	DCS1800 PCL = 7 @ 15.89 dBm	72	mA
	DCS1800 PCL = 15 @ 0.35 dBm	55	mA
	PCS1900 PCL = 0 @ 28.78 dBm	152	mA
	PCS1900 PCL = 7 @ 16.01 dBm	75	mA
	PCS1900 PCL = 15 @ 0.48 dBm	56	mA

Table 47: EC200U-AU Current Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	31	μA
Sleep state	Minimum functionality mode (USB disconnected)	1.034	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.06	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.52	mA
	EGSM900 @ DRX = 5 (USB suspended)	2.97	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.36	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.04	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.51	mA
	DCS1800 @ DRX = 5 (USB suspended)	2.93	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.36	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.63	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.87	mA
	LTE-FDD @ PF = 64 (USB suspended)	3.41	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.50	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.31	mA
	LTE-TDD @ PF = 32 (USB disconnected)	2.69	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.91	mA
	LTE-TDD @ PF = 64 (USB suspended)	3.37	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.52	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.32	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	12.71	mA
	EGSM900 @ DRX = 5 (USB connected)	27.90	mA
	LTE-FDD @ PF = 64 (USB disconnected)	13.05	mA

	LTE-FDD @ PF = 64 (USB connected)	28.33	mA
	LTE-TDD @ PF = 64 (USB disconnected)	13.10	mA
	LTE-TDD @ PF = 64 (USB connected)	28.34	mA
GPRS data transfer (GNSS Off)	GSM850 4DL/1UL @ 32.43 dBm	242	mA
	GSM850 3DL/2UL @ 31.00 dBm	385	mA
	GSM850 2DL/3UL @ 28.74 dBm	435	mA
	GSM850 1DL/4UL @ 26.50 dBm	447	mA
	EGSM900 4DL/1UL @ 32.39 dBm	208	mA
	EGSM900 3DL/2UL @ 30.81 dBm	325	mA
	EGSM900 2DL/3UL @ 28.76 dBm	376	mA
	EGSM900 1DL/4UL @ 26.68 dBm	392	mA
	DCS1800 4DL/1UL @ 29.97 dBm	153	mA
	DCS1800 3DL/2UL @ 28.47 dBm	220	mA
	DCS1800 2DL/3UL @ 26.28 dBm	245	mA
	DCS1800 1DL/4UL @ 24.29 dBm	256	mA
	PCS1900 4DL/1UL @ 29.78 dBm	152	mA
	PCS1900 3DL/2UL @ 28.26 dBm	228	mA
	PCS1900 2DL/3UL @ 26.26 dBm	261	mA
	PCS1900 1DL/4UL @ 24.08 dBm	270	mA
LTE data transfer (GNSS Off)	LTE-FDD B1 @ 23.84 dBm	730	mA
	LTE-FDD B2 @ 23.31 dBm	606	mA
	LTE-FDD B3 @ 23.10 dBm	603	mA
	LTE-FDD B4 @ 23.53 dBm	606	mA
	LTE-FDD B5 @ 22.90 dBm	533	mA
	LTE-FDD B7 @ 23.40 dBm	692	mA

	LTE-FDD B8 @ 23.81 dBm	650	mA
	LTE-FDD B28 @ 23.47 dBm	632	mA
	LTE-FDD B66 @ 23.60 dBm	506	mA
	LTE-TDD B38 @ 23.85 dBm	346	mA
	LTE-TDD B40 @ 23.05 dBm	405	mA
	LTE-TDD B41 @ 23.61 dBm	347	mA
GSM voice call	GSM850 PCL = 5 @ 32.40 dBm	260	mA
	GSM850 PCL = 12 @ 19.46 dBm	96	mA
	GSM850 PCL = 19 @ 6.59 dBm	63	mA
	EGSM900 PCL = 5 @ 32.40 dBm	227	mA
	EGSM900 PCL = 12 @ 19.05 dBm	88	mA
	EGSM900 PCL = 19 @ 6.05 dBm	61	mA
	DCS1800 PCL = 0 @ 29.95 dBm	168	mA
	DCS1800 PCL = 7 @ 16.50 dBm	75	mA
	DCS1800 PCL = 15 @ 1.25 dBm	57	mA
	PCS1900 PCL = 0 @ 29.76 dBm	168	mA
	PCS1900 PCL = 7 @ 16.42 dBm	77	mA
	PCS1900 PCL = 15 @ 1.66 dBm	58	mA

5.5. Tx Power

The following table shows the RF output power of the module.

Table 48: EC200U-CN RF Output Power

Frequency Band	Max. RF Output Power	Min. RF Output Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 49: EC200U-EU RF Output Power

Frequency Band	Max. RF Output Power	Min. RF Output Power
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38/B40/B41	23 dBm ±2 dB	< -39 dBm

Table 50: EC200U-AU RF Output Power

Frequency Band	Max. RF Output Power	Min. RF Output Power
GSM850	33 dBm ±2 dB	5 dBm ±5 dB
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1/B2/B3/B4/B5/B7/B8/B28/B66	23 dBm ±2 dB	< -39 dBm
LTE-TDD B38/B40/B41	23 dBm ±2 dB	< -39 dBm

NOTE

1. For GPRS transmission on 4 uplink timeslots, the maximum output power reduction is 6.0 dB. The design conforms to *3GPP TS 51.010-1* ***subclause 13.16***.
2. The GSM network access technology of EC200U-CN is optional. If the module that you select doesn't support GSM network access technology, there is no corresponding RF output power.

5.6. Rx Sensitivity

The following tables show conducted RF receiving sensitivity of the module.

Table 51: EC200U-CN Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP
	Primary	
EGSM900	-109.5 dBm	-102.0 dBm
DCS1800	-109.5 dBm	-102.0 dBm
LTE-FDD B1 (10 MHz)	-98.5 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-99.6 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99.2 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.7 dBm	-93.3 dBm
LTE-TDD B34 (10 MHz)	-99.2 dBm	-96.3 dBm
LTE-TDD B38 (10 MHz)	-98.8 dBm	-96.3 dBm
LTE-TDD B39 (10 MHz)	-99.5 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-99.4 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-98.9 dBm	-94.3 dBm

NOTE

The GSM network access technology of EC200U-CN is optional. If the module that you select doesn't support GSM network access technology, there is no corresponding RF receiving sensitivity data.

Table 52: EC200U-EU Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP
	Primary	
GSM850	-109.5 dBm	-102.0 dBm
EGSM900	-109.5 dBm	-102.0 dBm
DCS1800	-109 dBm	-102.0 dBm
PCS1900	-109 dBm	-102.0 dBm
LTE-FDD B1 (10 MHz)	-97.8 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.5 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99.2 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-97 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-98.7 dBm	-93.3 dBm
LTE-FDD B20 (10 MHz)	-96.8 dBm	-93.3 dBm
LTE-FDD B28 (10 MHz)	-98.8 dBm	-94.8 dBm
LTE-TDD B38 (10 MHz)	-98.3 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-98.5 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-98 dBm	-94.3 dBm

Table 53: EC200U-AU Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)	3GPP
	Primary	
GSM850	-109.9 dBm	-102.0 dBm
EGSM900	-110 dBm	-102.0 dBm
DCS1800	-109.6 dBm	-102.0 dBm
PCS1900	-109.6 dBm	-102.0 dBm
LTE-FDD B1 (10 MHz)	-98.6 dBm	-96.3 dBm
LTE-FDD B2 (10 MHz)	-98.5 dBm	-94.3 dBm
LTE-FDD B3 (10 MHz)	-98.9 dBm	-93.3 dBm
LTE-FDD B4 (10 MHz)	-98.7 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-97.9 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-99.3 dBm	-93.3 dBm
LTE-FDD B28 (10 MHz)	-99.8 dBm	-94.8 dBm
LTE-FDD B66 (10 MHz)	-98.4 dBm	-96.3 dBm
LTE-TDD B38 (10 MHz)	-99 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-99.7 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-99.1 dBm	-94.3 dBm

5.7. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 54: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter. The tolerances for dimensions without tolerance values are ±0.2 mm.

6.1. Mechanical Dimensions

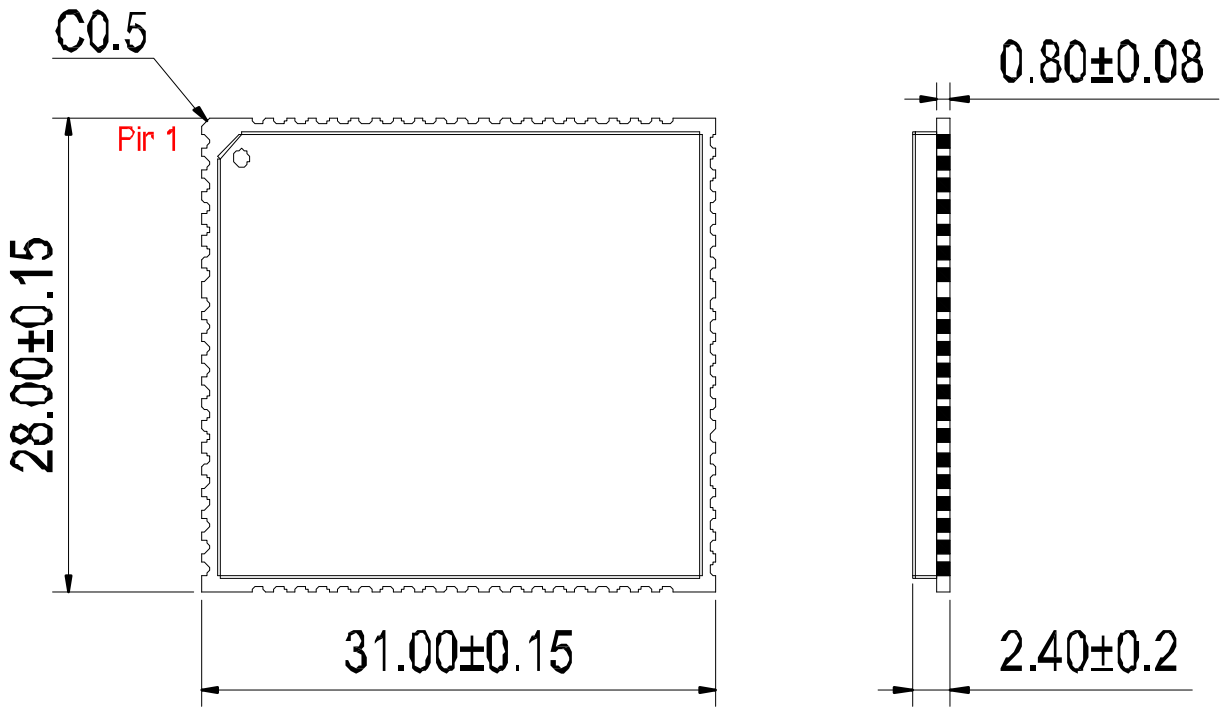


Figure 37: Module Top and Side Dimensions

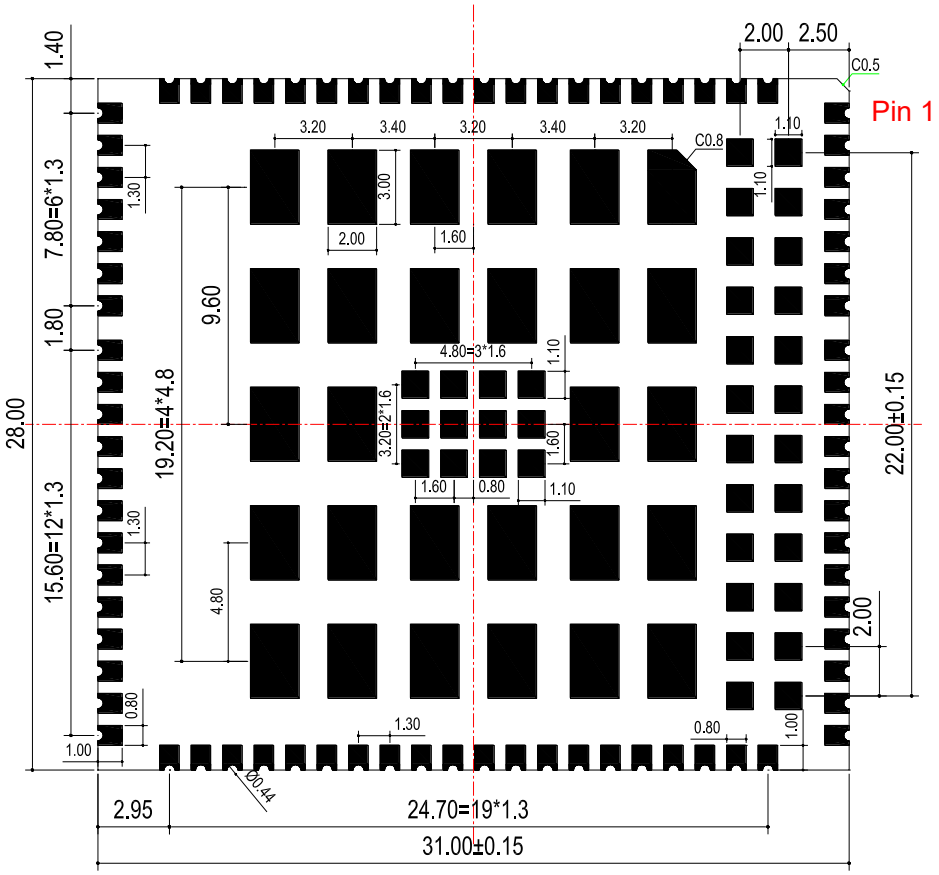


Figure 38: Module Bottom Dimensions

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

6.2. Recommended Footprint

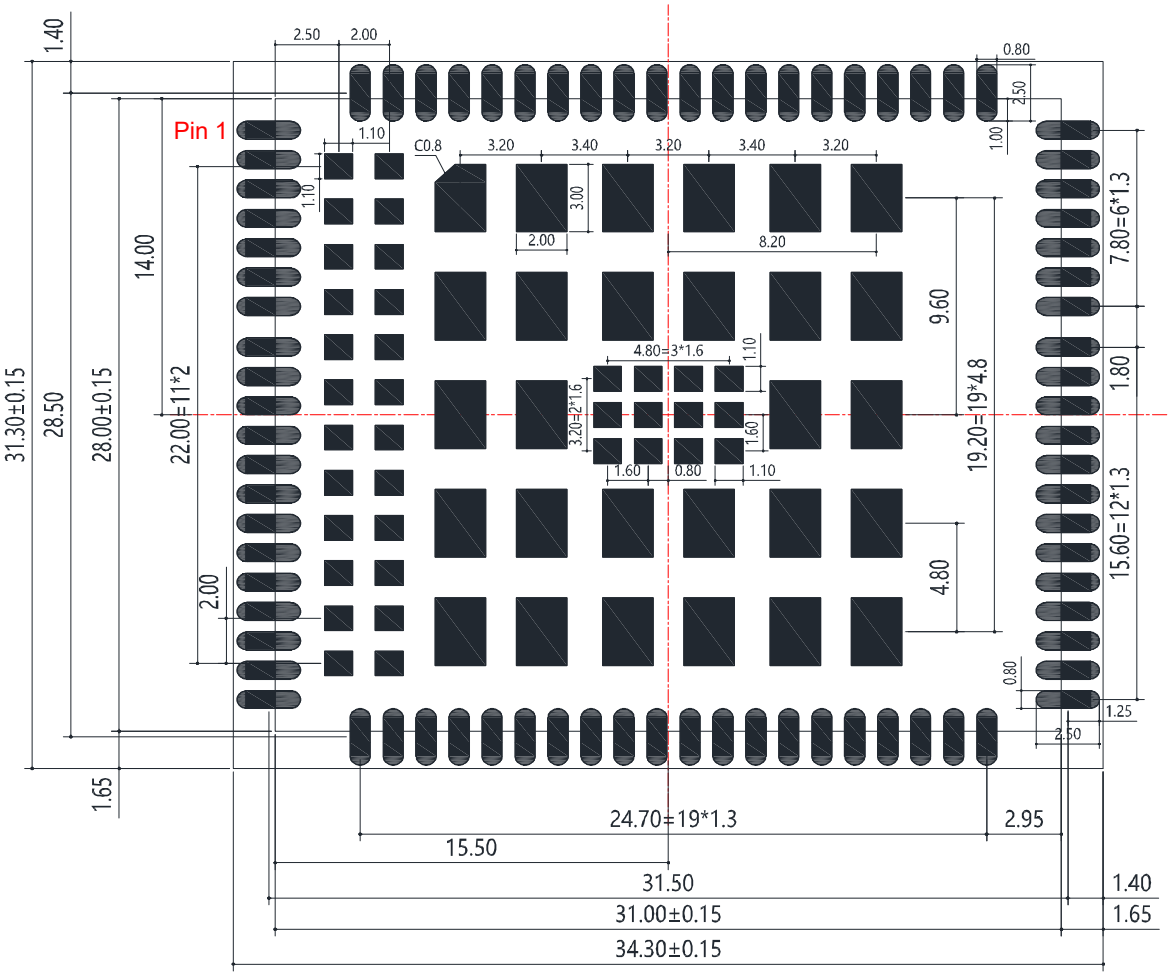


Figure 39: Recommended Footprint (Top View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3. Top and Bottom Views

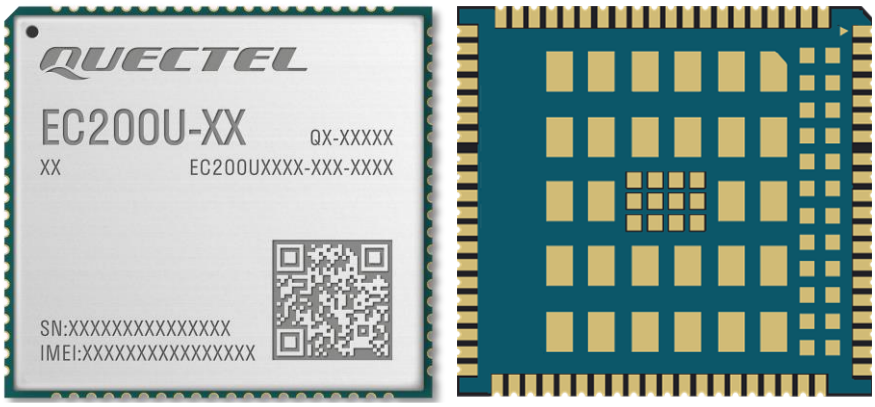


Figure 40: Top & Bottom View of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7 Storage, Manufacturing & Packaging

7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [12] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 ℃;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[12] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.20 mm. For more details, see ***document [9]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

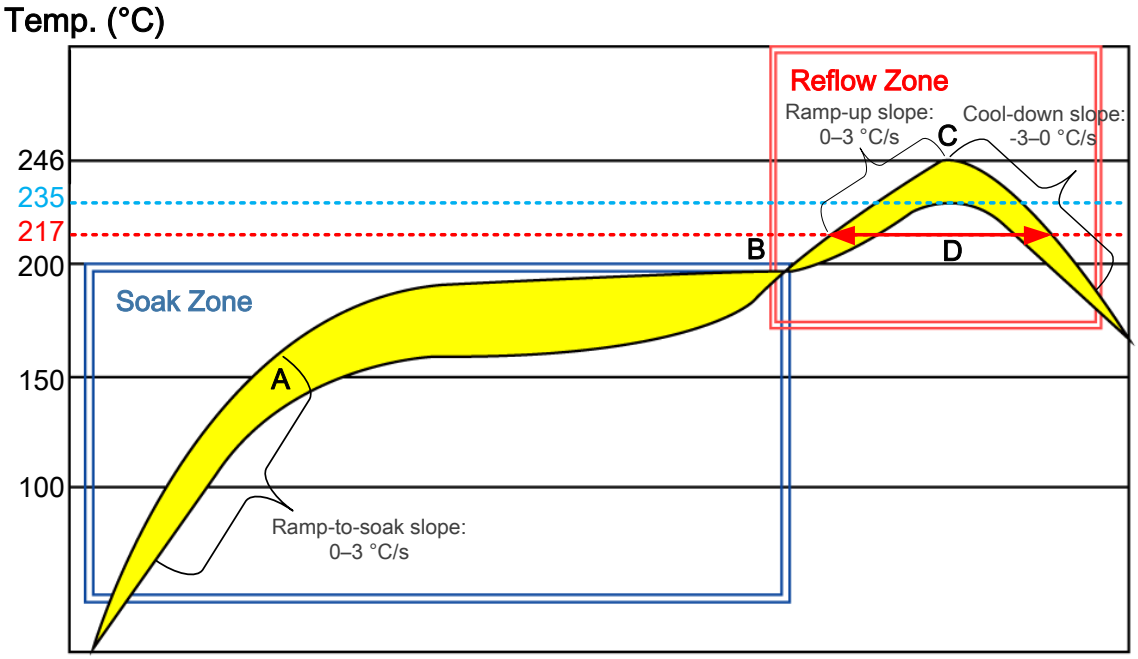


Figure 41: Reflow Soldering Thermal Profile

Table 55: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [9]***.

7.3. Packaging Specification

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

7.3.1. Carrier Tape

Dimension details are as follow:

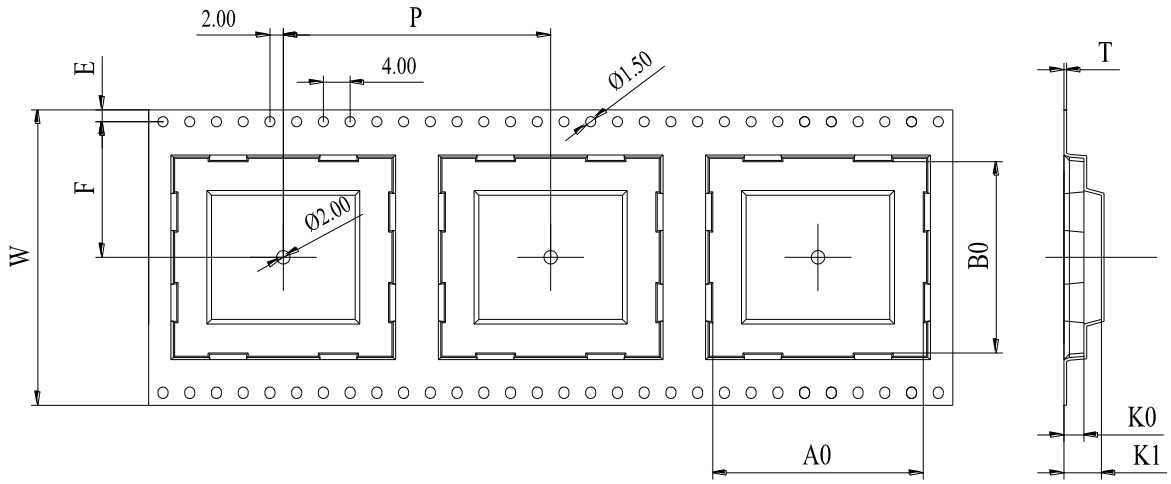


Figure 42: Carrier Tape Dimension Drawing

Table 56: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	40	0.4	31.5	28.5	3	5.6	20.2	1.75

7.3.2. Plastic Reel

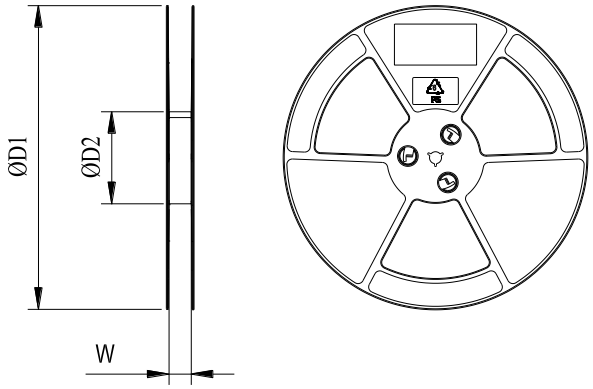


Figure 43: Plastic Reel Dimension Drawing

Table 57: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

7.3.3. Mounting Direction

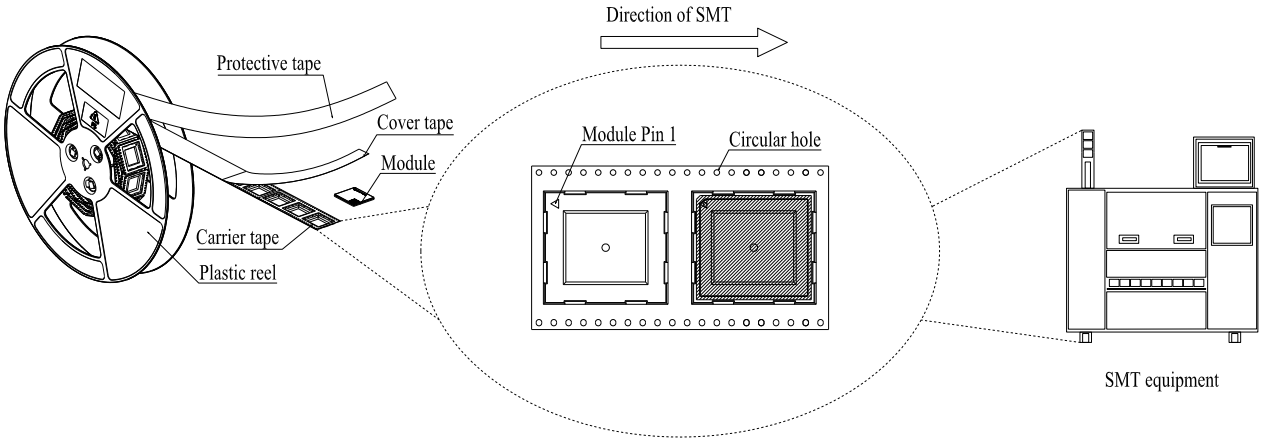
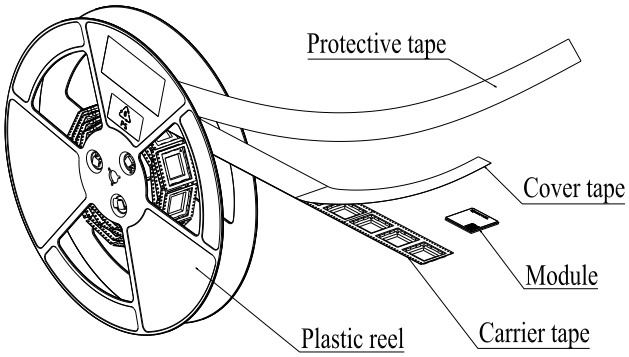


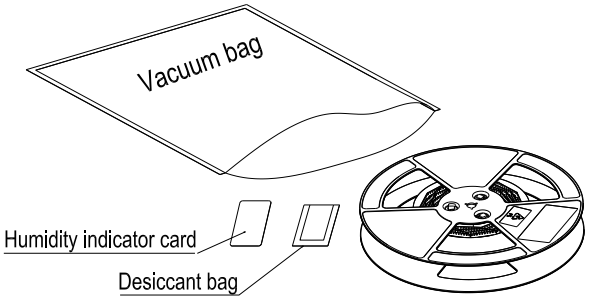
Figure 44: Mounting Direction

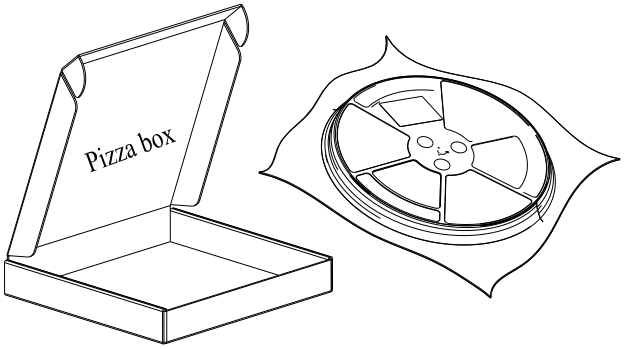
7.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

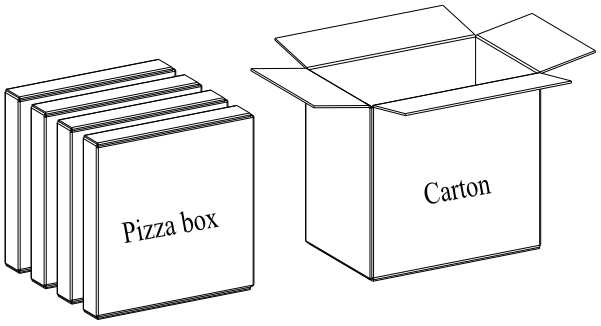


Figure 45: Packaging Process

8 Appendix References

Table 58: Related Documents

Document Name	
[1]	Quectel_LTE_OPEN_EVB_User_Guide
[2]	Quectel_EC200U_Series_QuecOpen_GPIO_Configuration
[3]	Quectel_EC200U&EG91xU_Series_QuecOpen_Device_Management_API_Reference_Manual
[4]	Quectel_EC200U&EG91xU_Series_QuecOpen_Low_Power_Consumption_API_Reference_Manual
[5]	Quectel_EC200U&EG91xU_Series_QuecOpen_Booting&Shutdown_Development_Guide
[6]	Quectel_EC200U_Series_QuecOpen_Reference_Design
[7]	Quectel_EC200U&EG91xU_Series_QuecOpen_ADC_Development_Guide
[8]	Quectel_RF_Layout_Application_Note
[9]	Quectel_Module_SMT_User_Guide

Table 59: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection Multiplexing
CS	Coding Scheme

CTS	Clear to Send
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DMA	Direct Memory Access
DSDS	Dual SIM Dual Standby
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
EVB	Evaluation Board
FDD	Frequency Division Duplex
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP-over-SSL
GND	Ground
GSM	Global System for Mobile Communications
HR	Half Rate
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
LED	Light Emitting Diode
LTE	Long Term Evolution
MCU	Microcontroller Unit/Microprogrammed Control Unit

ME	Mobile Equipment
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Level
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PF	Paging Frame
PING	Packet Internet Groper
PMIC	Power Management IC
POS	Point of Sale
PPP	Point-to-Point Protocol
RF	Radio Frequency
RGB	Red, Green, Blue
SM	Smart Media
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver &Transmitter
UDP	User Datagram Protocol

UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WLAN	Wireless Local Area Network