BG600L-M3

Reference Design

LPWA Module Series

Version: 1.2

Date: 2022-08-18

Status: Released

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About the Document

Revision History

Version	Date	Author	Description
1.0	2020-07-07	Lyndon LIU/ Newgate HUA	Initial
1.1	2021-06-21	Army RONG/ Lex LI	Modified PON_TRIG peripheral circuit in Sheet 8.
1.2	2022-08-18	Lex LI/ Pearl GUO	1. Updated the note about PON_TRIG in Sheet 3. 2. Updated VBAT reference design and related notes in standard and battery power supply solutions in Sheet 4 and Sheet 5.

Contents

1 Reference Design

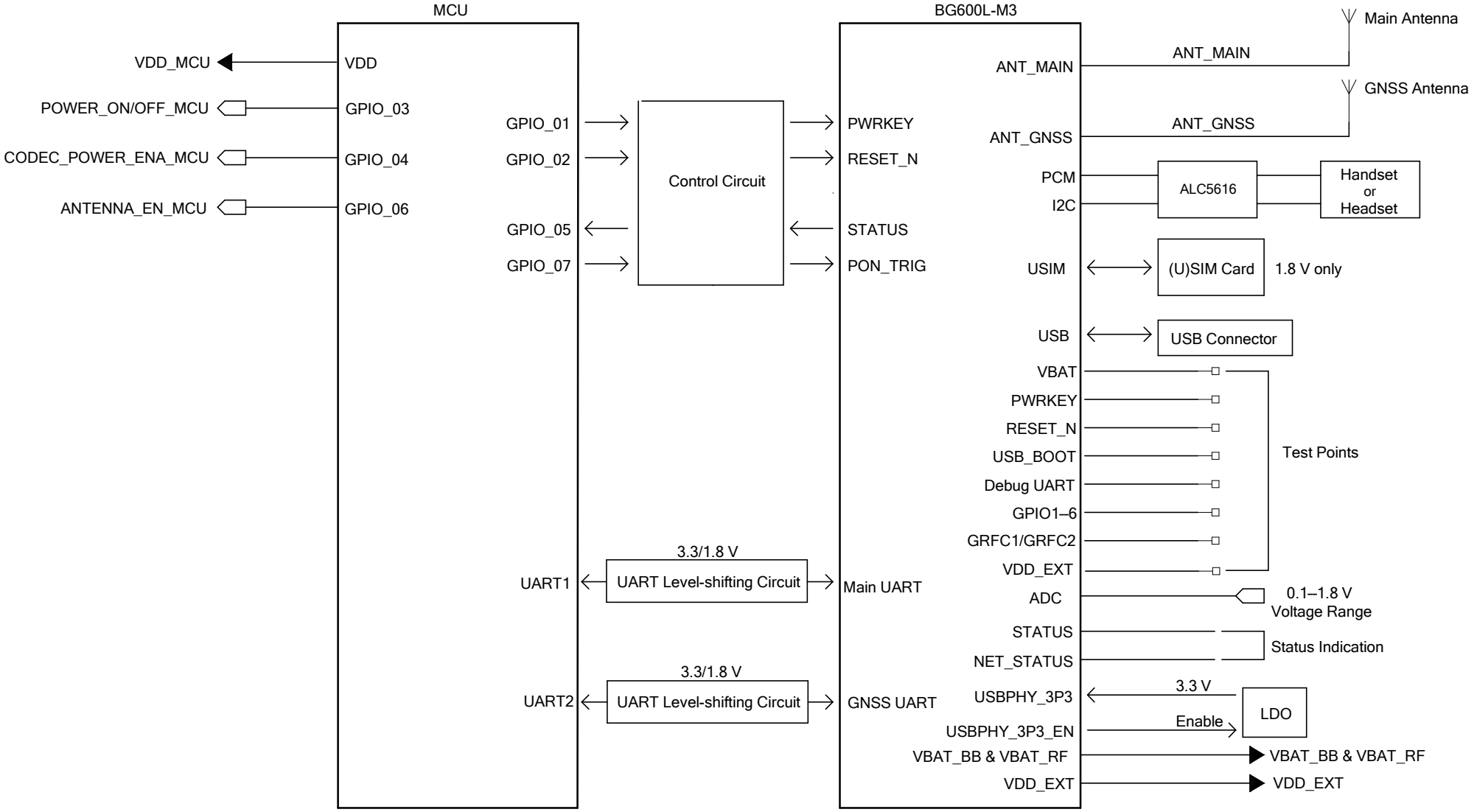
1.1. Introduction

This document provides reference designs of Quectel BG600L-M3 module, including power supply, (U)SIM, UART, USB, audio and more interface designs.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



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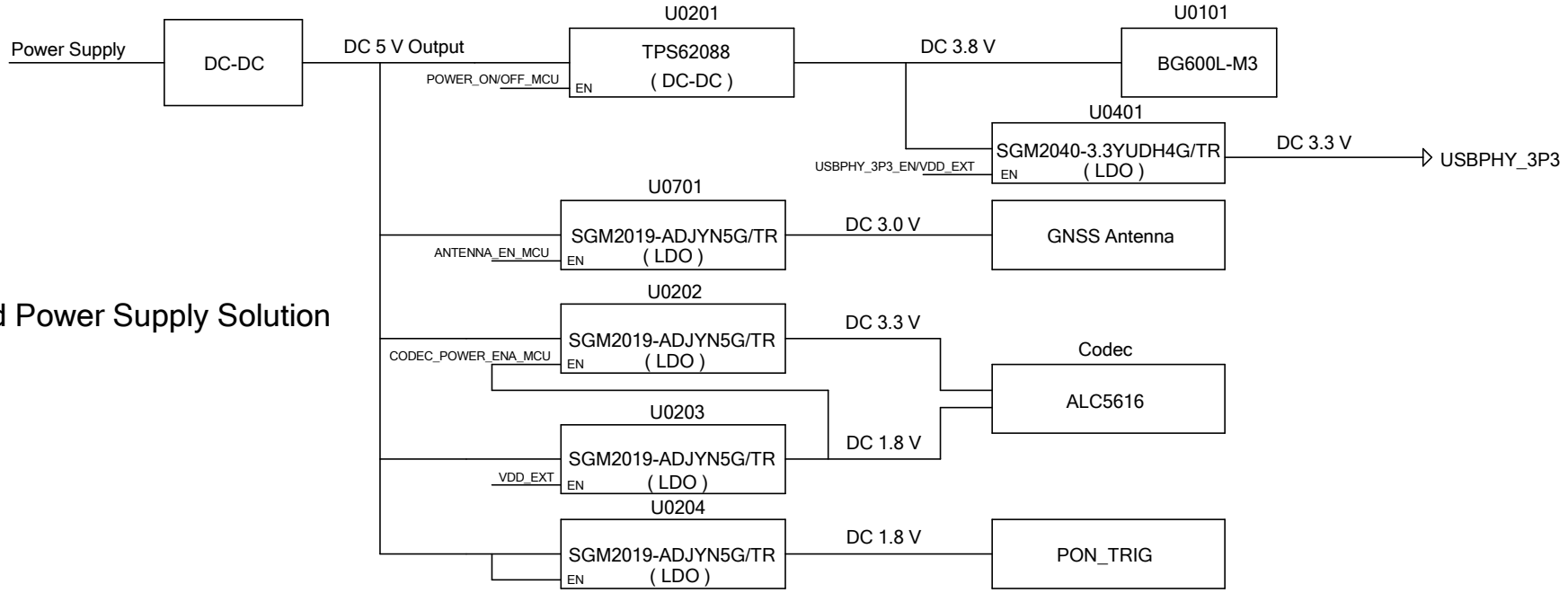
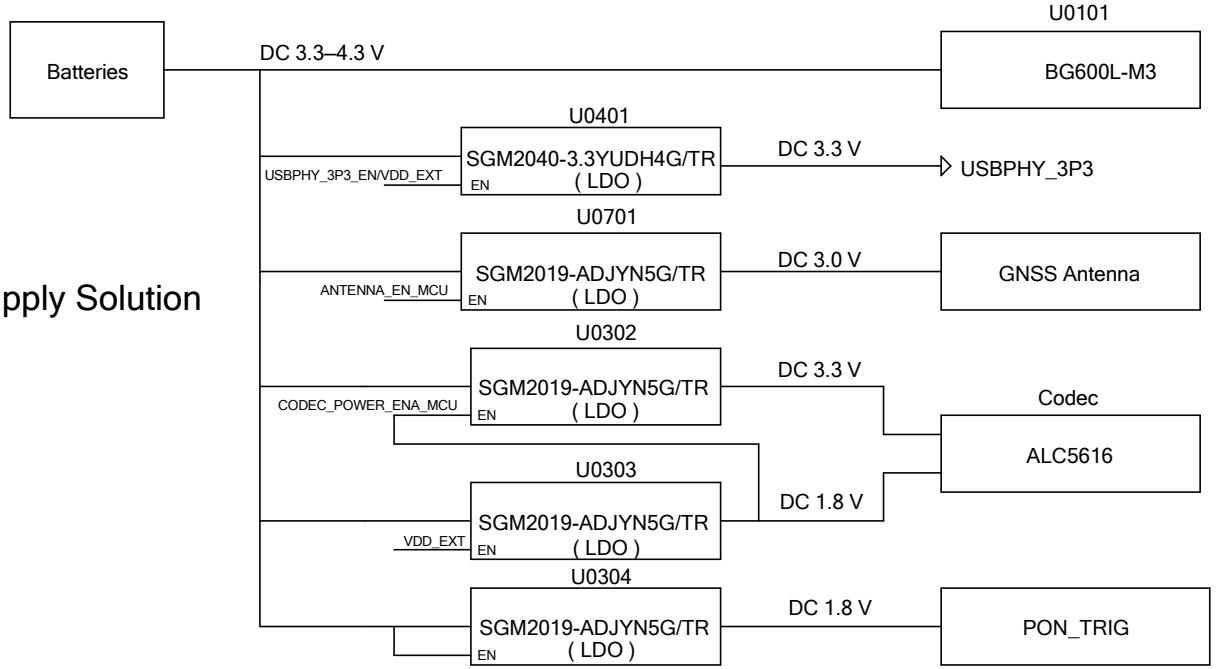
	SHEET 1 OF 14	DATE 2022/8/18

Power Supply Block Diagram

Standard Power Supply Solution



Battery Power Supply Solution



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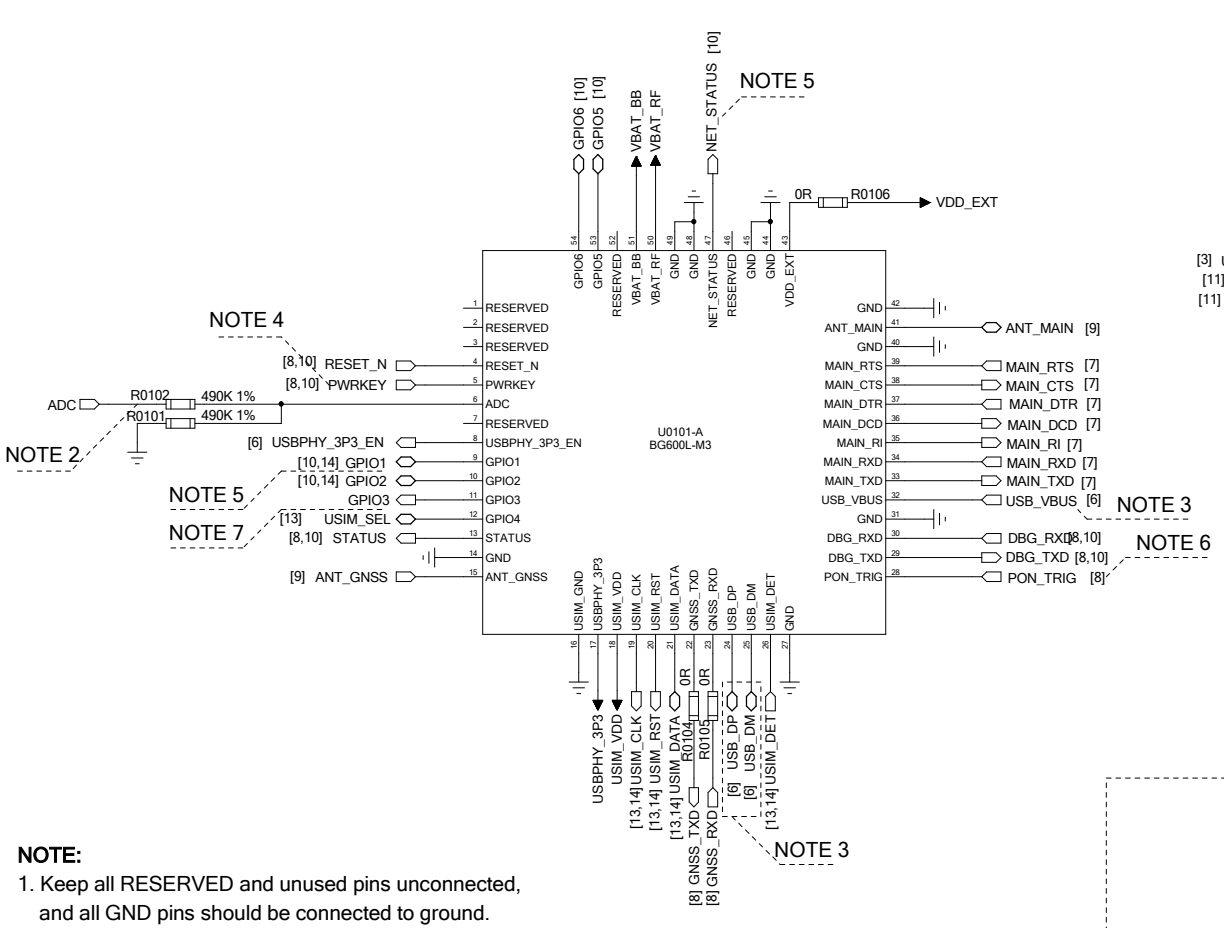
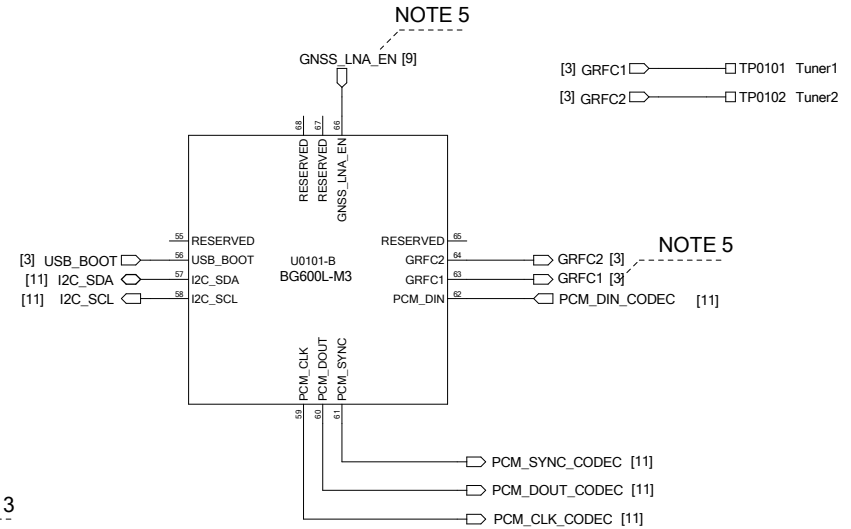
Module Interfaces Design

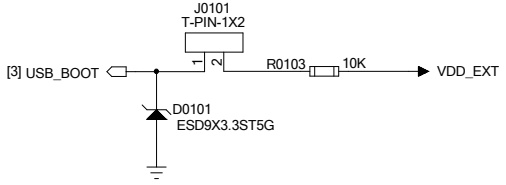




NOTE:

1. Keep all RESERVED and unused pins unconnected, and all GND pins should be connected to ground.
2. ADC pin can not be directly connected to the power supply and must not exceed 1.8 V. It is recommended to use resistor divider circuit for ADC application, and the divider resistor accuracy should be no less than 1 %.
3. The USB interface supports slave mode only and supports low-speed, full-speed and high-speed modes. The USB interface is primarily used for AT command communication, GNSS NEMA sentences output, software debugging and firmware upgrade. The input voltage range of USB_VBUS is 1.3–1.8 V.
4. Never pull down PWRKEY to GND permanently.
5. GPIO1, NET_STATUS, GRFC1 and GNSS_LNA_EN are BOOT_CONFIG pins, and do not pull them up before startup. Otherwise, the module cannot power on normally.
6. When PON_TRIG detects a rising edge and keeps at high level for at least 30 ms, the module will wake up from PSM (Power Saving Mode). PON_TRIG is pulled down by default.
7. To meet specific requirements for power-down protection, the module can support fast shutdown over GPIO3, through software configuration. When GPIO3 (pin 11, GPIO by default) is set to a fast shutdown pin, it is pulled up by default. When the pin detects a falling edge, the module powers off within 100 ms without damaging the file system, but the writing data may be lost.

USB_BOOT Design



NOTE:

Pulling up USB_BOOT to VDD_EXT before startup, the module will be forced into emergency download mode when it is powered on.

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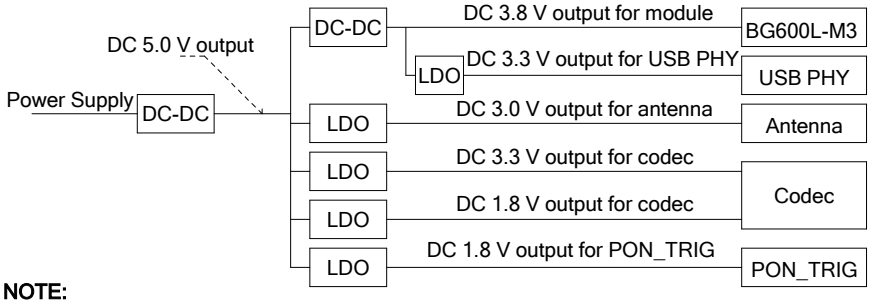
	SHEET 3 OF 14	DATE 2022/8/18

Power Supply Design (Standard)

DC-DC Application

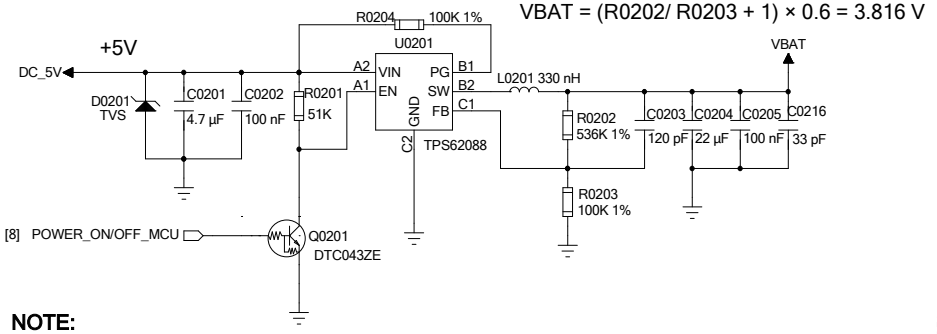


NOTE:

1. You can select either the standard power supply design or the battery power supply design according to your specific application demands.
2. The solution is used when the input voltage is above 7.0 V. First, use a DC-DC converter to convert the high input voltage into a 5.0 V output, and then use LDOs and a DC-DC converter to generate 3.8 V, 3.3 V, 3.0 V and 1.8 V typical voltages.

DC-DC Design

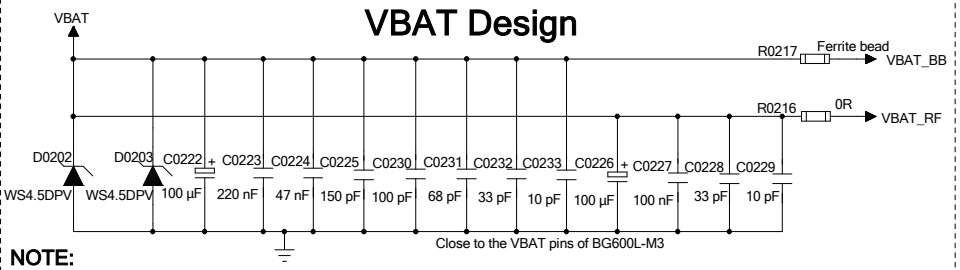
VBAT = (R0202/ R0203 + 1) × 0.6 = 3.816 V



NOTE:

The maximum input supply voltage of U0201 is 5.5 V.

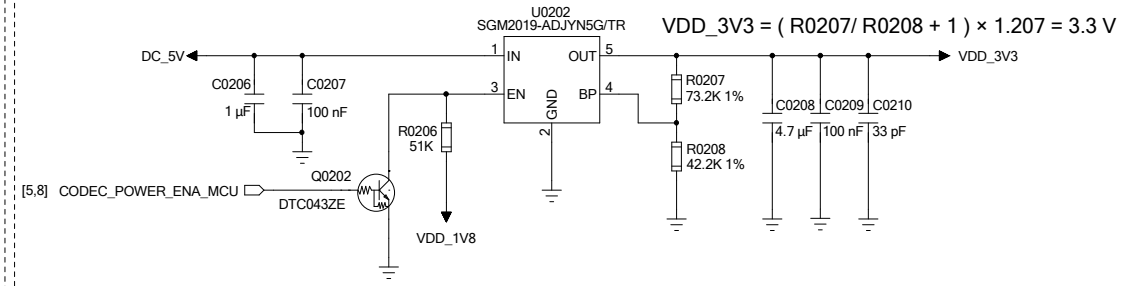
VBAT Design

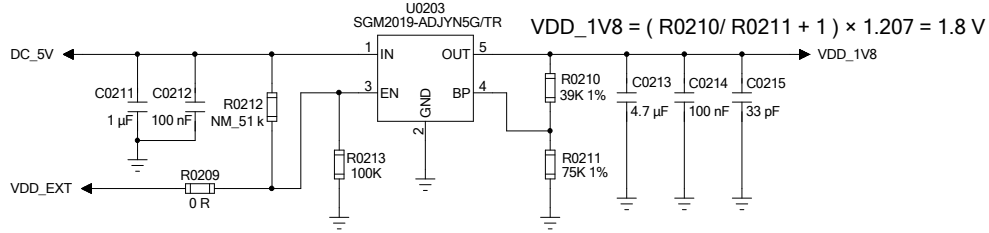


NOTE:

1. VBAT should be routed in star structure to VBAT_BB and VBAT_RF pins.
2. Select a ferrit bead for R0217, and place it as close to VBAT_BB as possible. R0217 requirements:
1) Current rating ≥ 600 mA and low DC resistance to avoid voltage drop during instantaneous high power consumption.
2) ≥ 800 Ω impedance @ 700-960 MHz.

Audio Codec Power Supply

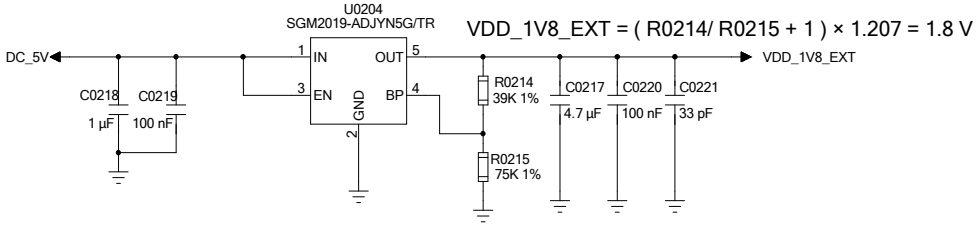




NOTE:

1. CODEC_POWER_ENA_MCU must be at low level to ensure the normal output voltage of VDD_3V3. If CODEC_POWER_ENA_MCU is at high level, VDD_3V3 power supply will be switched off.
2. The following power-on/off sequences should be followed to ensure the audio codec works normally.
Power-on sequence: power on VDD_1V8 first, and then VDD_3V3.
Power-off sequence: power off VDD_3V3 first, and then VDD_1V8.

PON_TRIG Power Supply



NOTE:

PON_TRIG is powered by an external LDO.

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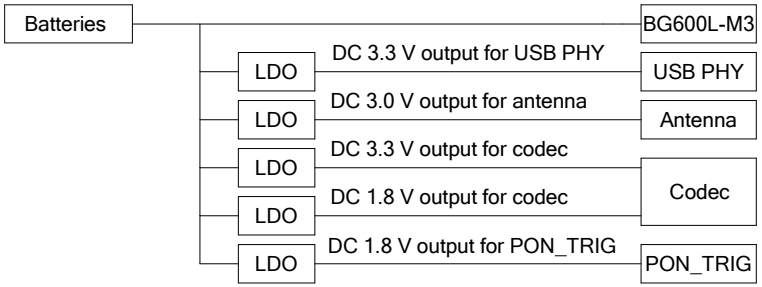
	SHEET 4 OF 14	DATE 2022/8/18

Power Supply Design (Battery)

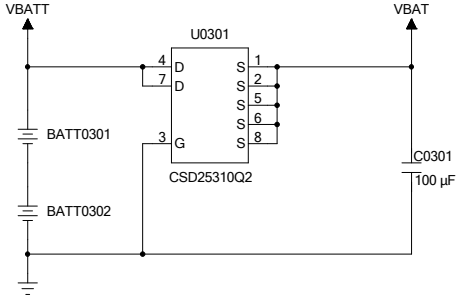
Battery Application



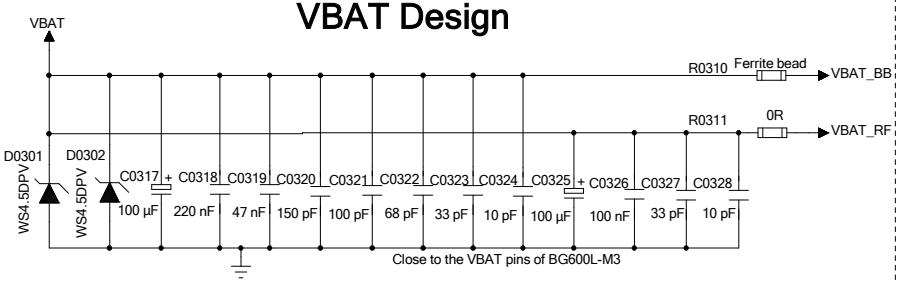
NOTE:

1. You can select either the standard power supply design or the battery power supply design according to your specific application demands.
2. The output voltage of batteries must be 3.3–4.3 V.

Battery Polarity Protection Design



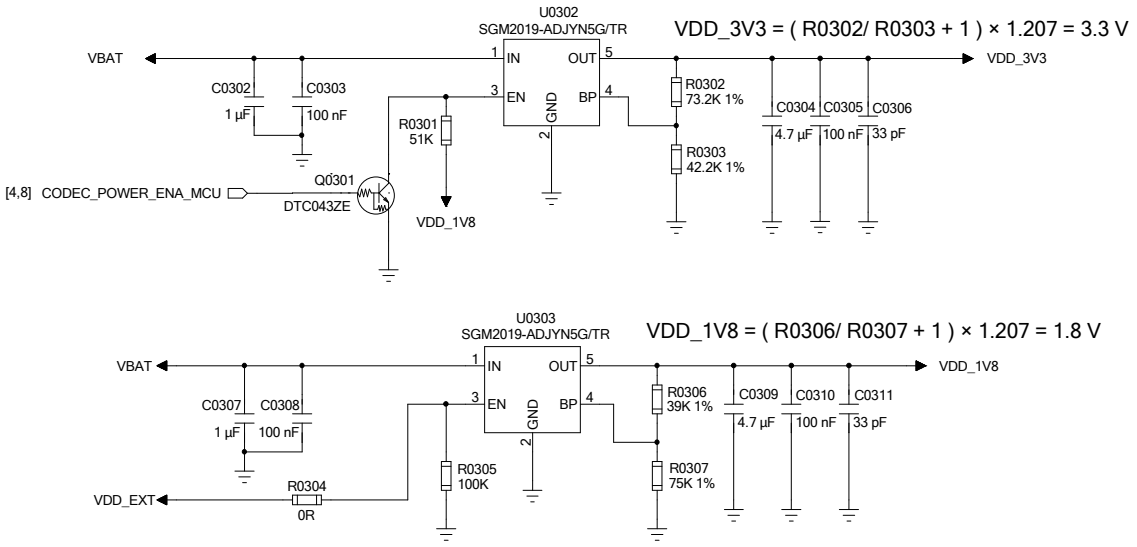
VBAT Design



NOTE:

1. VBAT should be routed in star structure to VBAT_BB and VBAT_RF pins.
2. Select a ferrit bead for R0310, and place it as close to VBAT_BB as possible. R0310 requirements:
   1) Current rating ≥ 600 mA and lower DC resistance to avoid voltage drop during instantaneous high power consumption.
   2) Impedance ≥ 800 Ω @ 700-960 MHz.

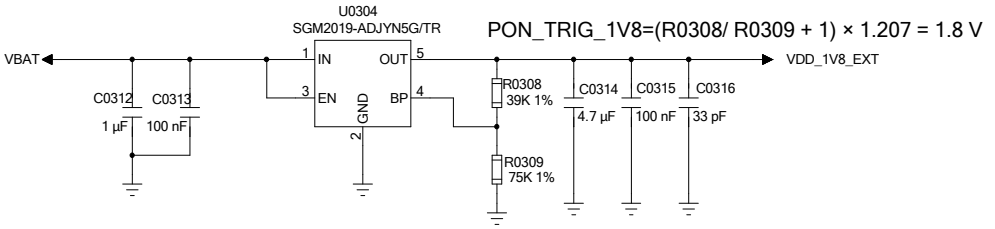
Audio Codec Power Supply



NOTE:

1. CODEC_POWER_ENA_MCU must be at low level to ensure the normal output voltage of VDD_3V3. If CODEC_POWER_ENA_MCU is at high level, VDD_3V3 power supply will be switched off.
2. The following power-on/off sequences should be followed to ensure the audio codec works normally.
   Power-on sequence: power on VDD_1V8 first, and then VDD_3V3.
   Power-off sequence: power off VDD_3V3 first, and then VDD_1V8.

PON_TRIG Power Supply



NOTE:

PON_TRIG is powered by an external LDO.

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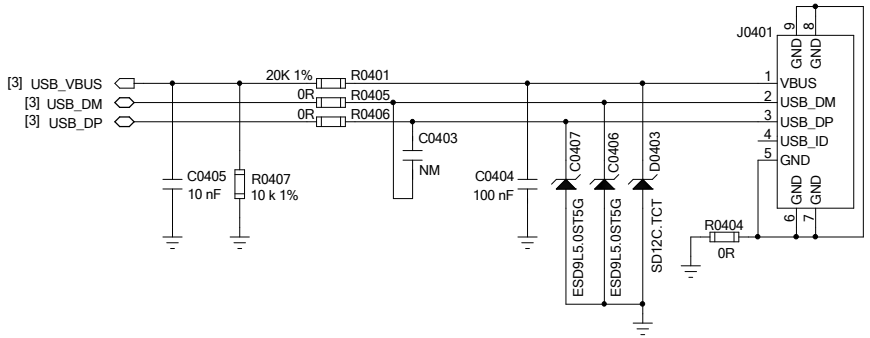
	SHEET 5 OF 14	DATE 2022/8/18

USB Interface Design

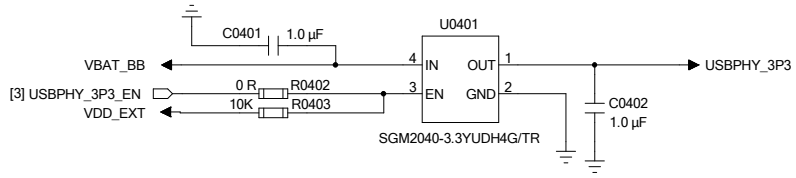
USB Connector Design



NOTE:

1. The junction capacitance of the ESD protection components should be less than 2 pF.
2. It is important to route the USB signal traces as differential pairs with surrounded ground.
   The impedance of USB differential trace is 90 Ω.

Power Supply for USB PHY Circuit



NOTE:

The typical voltage of USBPHY_3P3 is 3.3 V.

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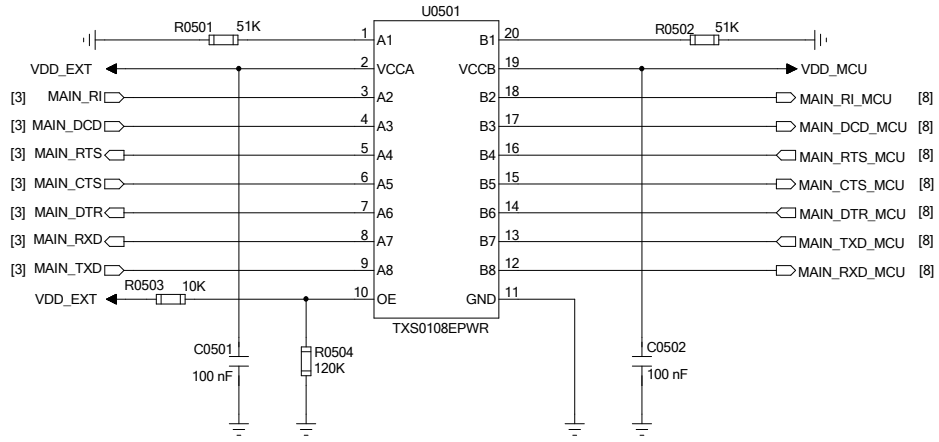
	SHEET 6 OF 14	DATE 2022/8/18

UART Interface Design

UART Interface with Voltage-level Translator



NOTE:

1. It is recommended to use a voltage-level translator TXS0108EPWR between BG600L-M3 and MCU.
2. VCCA should not exceed VCCB. For more information about TXS0108EPWR, see the datasheet from TI website.

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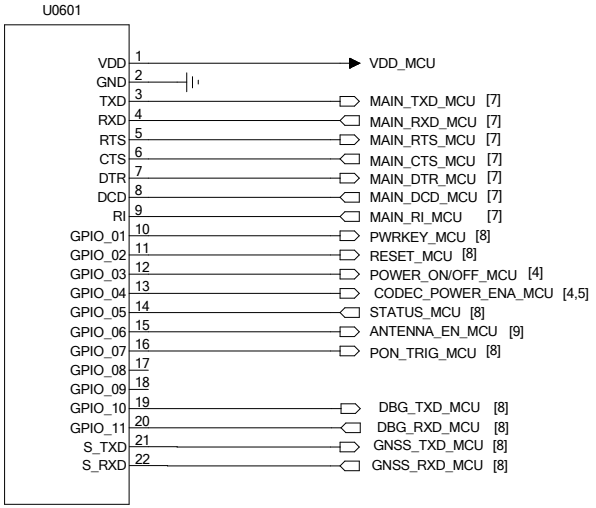
	SHEET 7 OF 14	DATE 2022/8/18

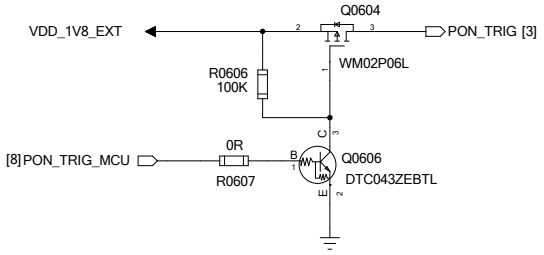
MCU Interfaces Design

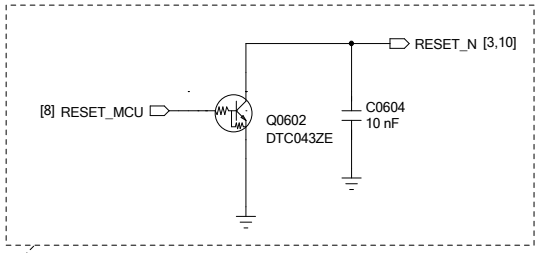


NOTE:

1. U0601 represents your MCU.
2. Pay attention to the UART interface connection of RTS/CTS.
3. When BG600L-M3 enters PSM, set the MCU's UART interface into the high-impedance mode.

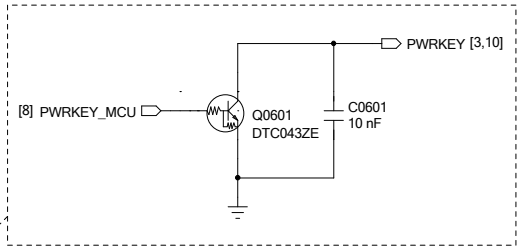
PON_TRIG Design

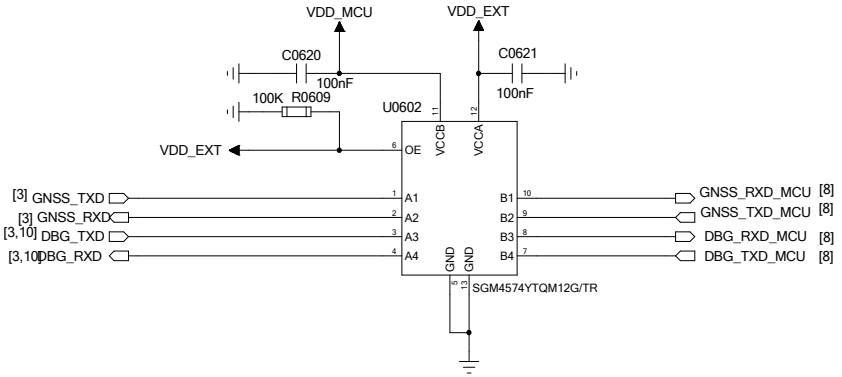


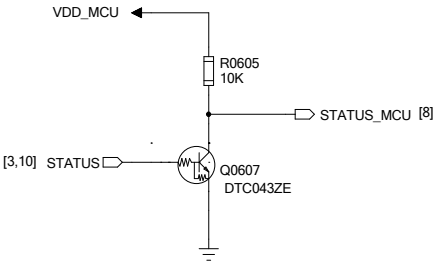


NOTE 1

NOTE 2







State	STATUS	STATUS_MCU
Power-off	0	1
Power-on	1	0

NOTE:

1. Reset the module by driving RESET_N low for 2–3.8 s.
2. When the module is in turn-off state, it can be turned on by driving PWRKEY low for 500–1000 ms. After the module is turned on, it can be turned off by driving PWRKEY low for 650–1500 ms. Never pull down PWRKEY to GND permanently.

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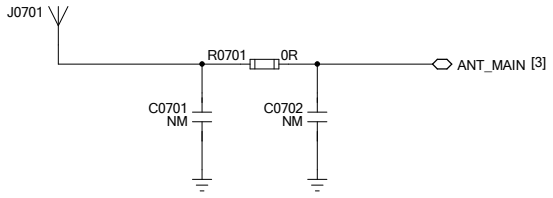
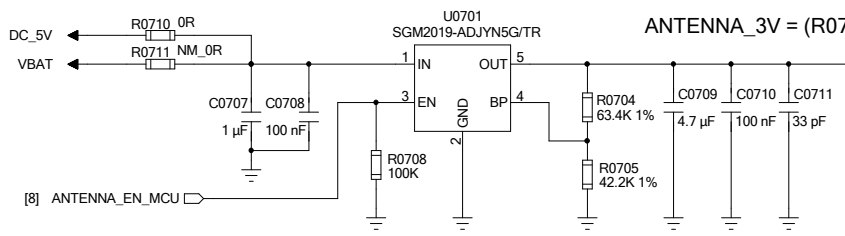
	SHEET 8 OF 14	DATE 2022/8/18

Antenna Interfaces Design

Main Antenna Interface



Power Supply for Antenna



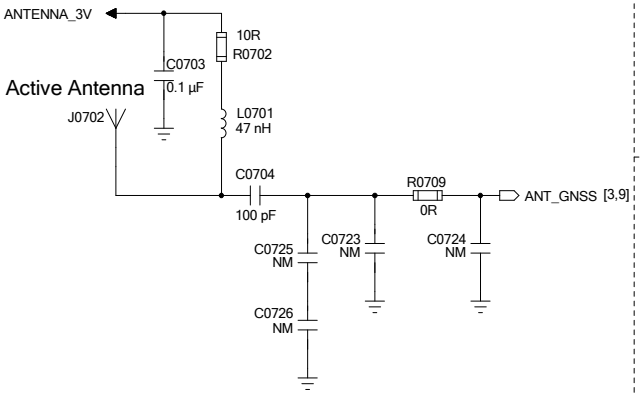
ANTENNA_3V = (R0704/ R0705 + 1) × 1.207 = 3.0 V

	R0710	R0711
Standard Solution	M	NM
Battery Solution	NM	M

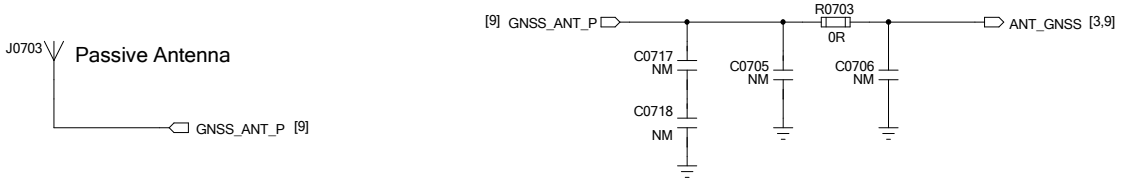
GNSS Antenna Interface

GPS_EXT
GNSS_ENABLE — TP0701

Active Antenna Design

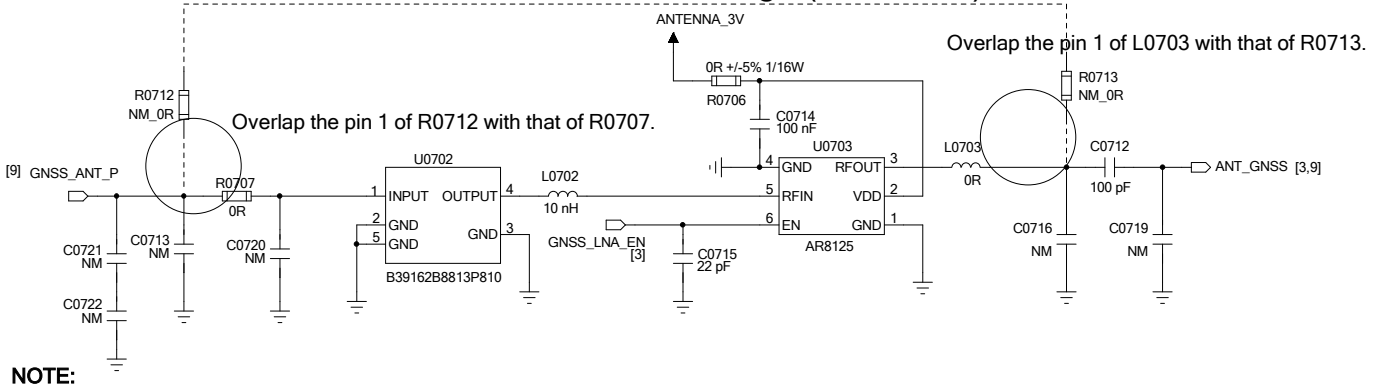


Passive Antenna Design (Solution 1)



NOTE:
This solution is ideal for compact-sized applications where the cable insertion loss from the module to the antenna is small.

Passive Antenna Design (Solution 2)



NOTE:
This solution is ideal for applications where the cable insertion loss from the module to the antenna is large and external LNA and SAW are needed.

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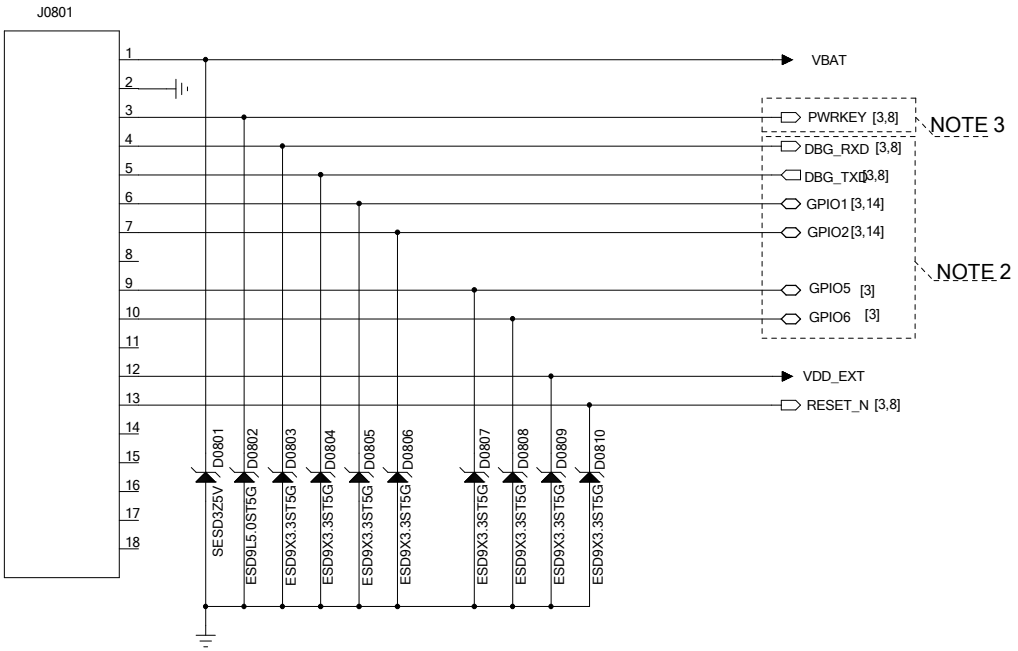
	SHEET 9 OF 14	DATE 2022/8/18

Test Points and Indicators

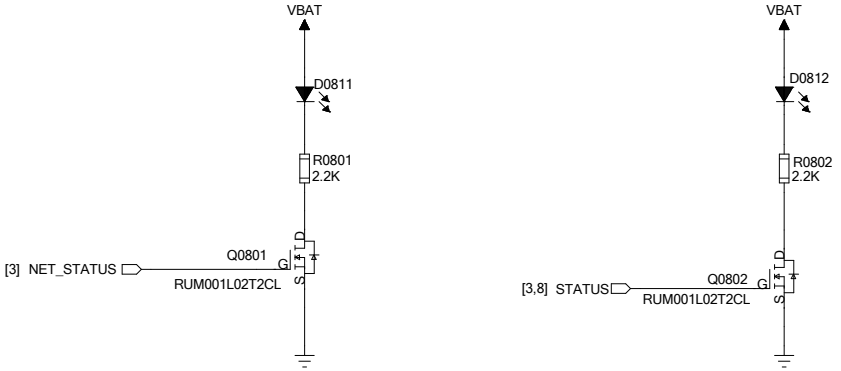
Reserved Test Points



NOTE:

1. It is recommended to reserve the test points for debug UART interface for future software debugging.
2. The voltage level of debug UART interface and GPIO interfaces is 1.8 V.
   Do not connect them directly to a 3.3 V level.
3. Never pull down PWRKEY to GND permanently.

Indicators



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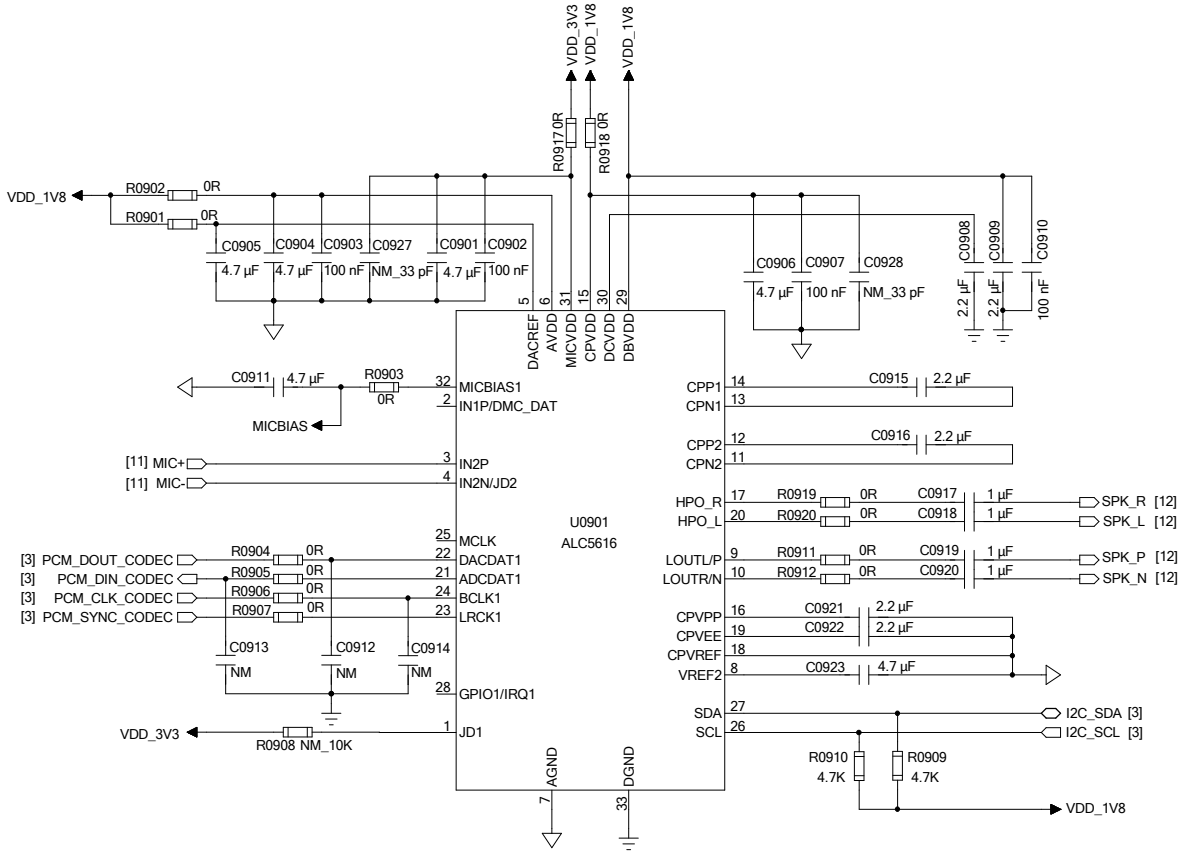
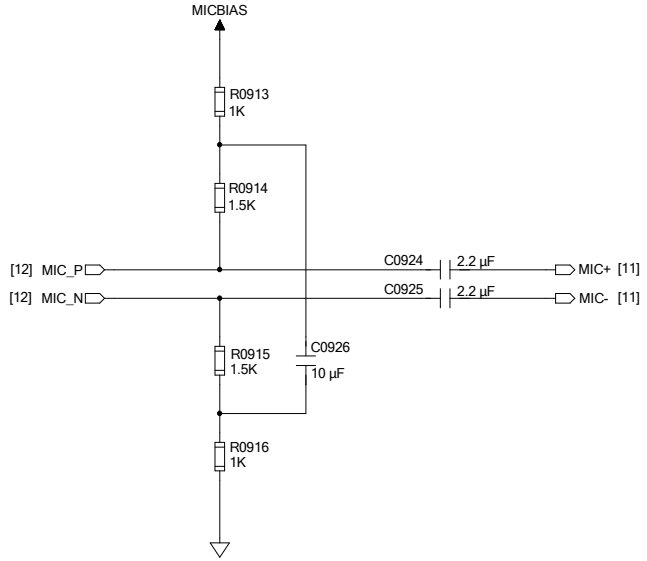
CHECKED BY Woody WU	SIZE A2	VER 1.2
	SHEET 10 OF 14	DATE 2022/8/18

Audio Codec Design





NOTE:

1. To ensure that ALC5616 works normally, follow the power-on and power-off sequences of its power supply.
   Power-on sequence: power on DBVDD/AVDD/DACREF/CPVDD first, and then MICVDD.
   Power-off sequence: power off MICVDD first, and then DBVDD/AVDD/DACREF/CPVDD.
   For more details, see the datasheet of ALC5616.
2. BG600L-M3 automatically initializes the codec via I2C interface after the module is turned on successfully, so all power supplies for the codec need to be switched on before that.

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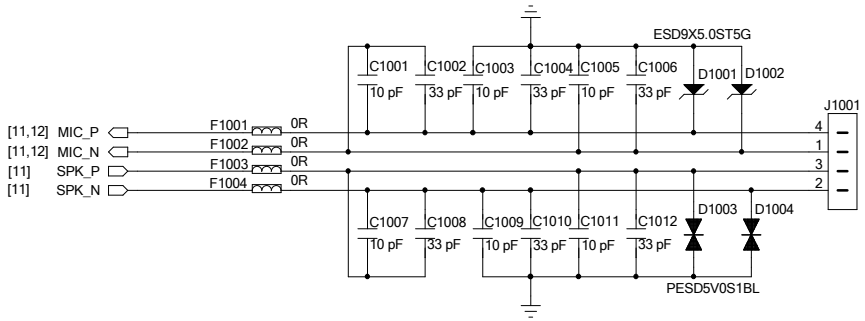
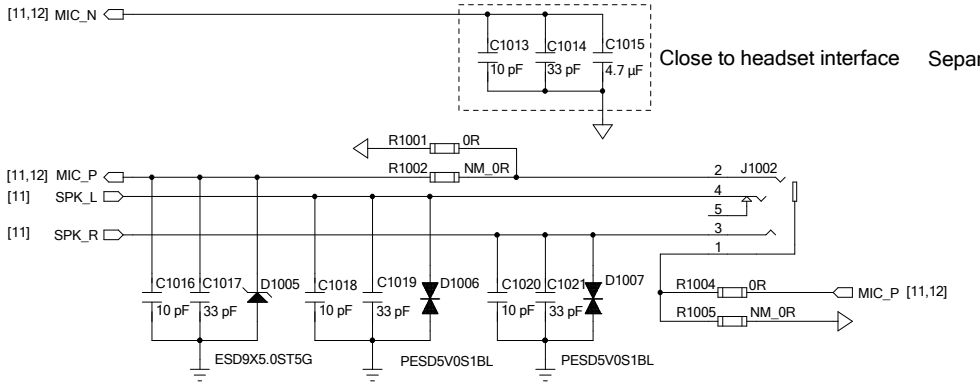
CHECKED BY Woody WU	SIZE A2	VER 1.2
	SHEET 11 OF 14	DATE 2022/8/18

Audio Interface Design

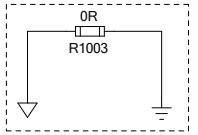
Handset Application



Headset Application



Separate analog ground and digital ground



	CTIA	OMTP
R1002/R1005	NM	M
R1001/R1004	M	NM

NOTE:

1. The analog output only drives headset and handset. For larger-power loads such as loudspeakers, add an audio power amplifier in the design.
2. The maximum capacitive loading for loudspeaker is 330 pF and that for microphone is 250 pF.
3. In handset applications, route both the microphone and the speaker signal traces as differential pairs.
4. In headset applications, route the microphone signal traces as differential pairs.
5. Route all microphone and loudspeaker signal traces with ground surrounded and keep them far away from noise signals such as clock and DC-DC signals.
6. The 0 Ω resistor (R1003), which separates analog ground and digital ground, suppresses loop current and reduces noise interference.

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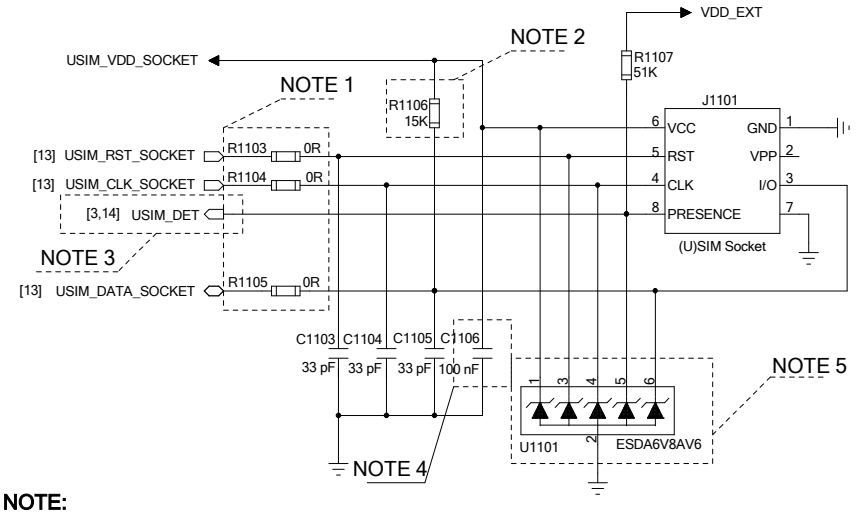
CHECKED BY Woody WU	SIZE A2	VER 1.2
	SHEET 12 OF 14	DATE 2022/8/18

(U)SIM Interface Design (1.8 V Only)

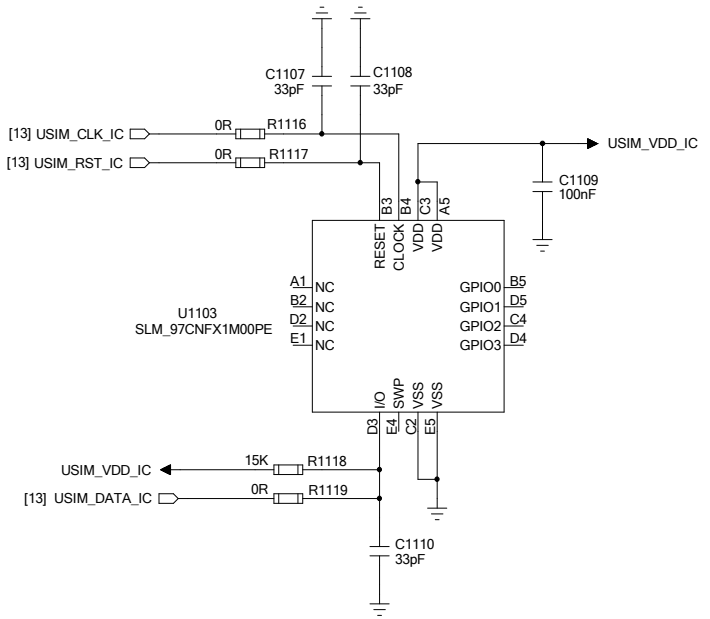
(U)SIM Card Socket Design



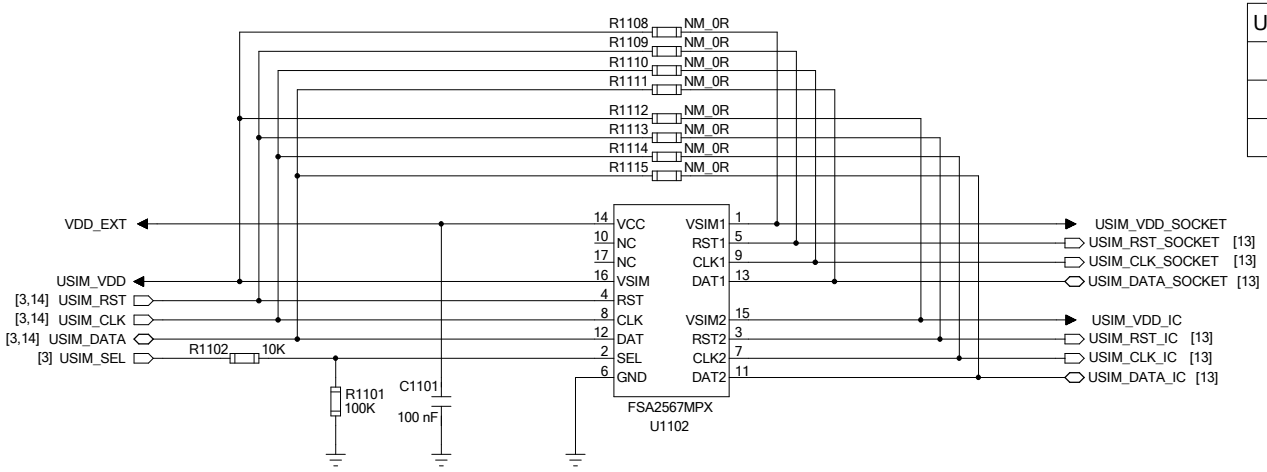
NOTE:

1. R1103–R1105 are applied to facilitate debugging. It is recommended to reserve the series resistors for (U)SIM signals of the module.
2. The pull-up resistor (R1106) on USIM_DATA trace can improve anti-jamming capability.
3. BG600L-M3 supports (U)SIM card hot-plugging, which can be implemented through USIM_DET pin.
4. The value of C1106 should be less than 1 μF.
5. Parasitic capacitance of the TVS array should not exceed 15 pF.

eSIM Design (1.8 V Only)



Analog Switch for (U)SIM Interface



U1102	R1108–R1111	R1112–R1115	
M	NM	NM	Switch + Socket/eSIM IC
NM	M	NM	Single Socket
NM	NM	M	Single eSIM IC

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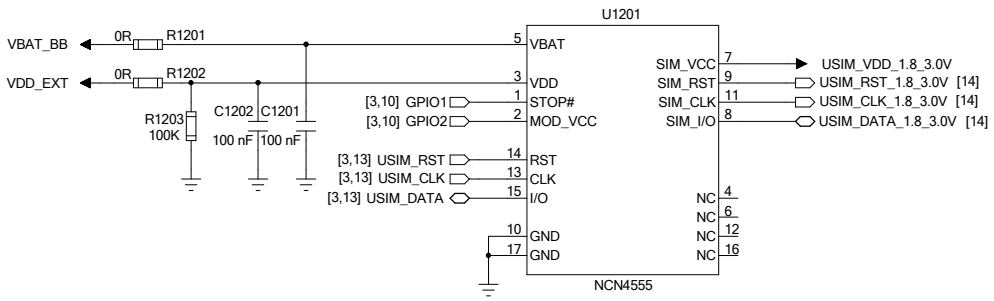
CHECKED BY Woody WU	SIZE A2	VER 1.2
	SHEET 13 OF 14	DATE 2022/8/18

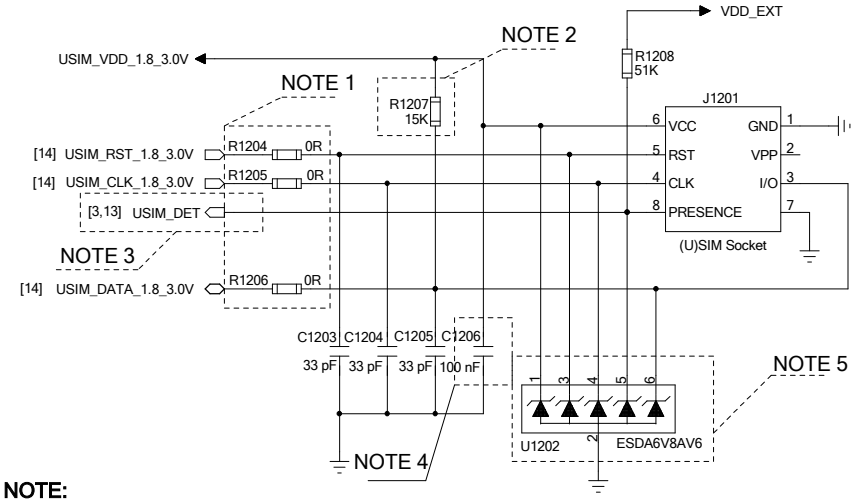
(U)SIM Interface Level-shifting Circuit Design (1.8/3.0 V)

(U)SIM Interface Level-shifting Circuit Design



STOP#	MOD_VCC	Description
Low	High/Low	Shutdown mode
High	Low	SIM_VCC = 1.8 V. 1.8 V (U)SIM card is supported (default).
High	High	SIM_VCC = 3.0 V. 3.0 V (U)SIM card is supported.

(U)SIM Card Socket Design



NOTE:

1. R1204–R1206 are applied to facilitate debugging. It is recommended to reserve the series resistors for (U)SIM signals of the module.
2. The pull-up resistor (R1207) on USIM_DATA trace can improve anti-jamming capability.
3. BG600L-M3 supports (U)SIM card hot-plugging, which can be implemented through USIM_DET pin.
4. The value of C1206 should be less than 1 μF.
5. Parasitic capacitance of the TVS array should not exceed 15 pF.

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CHECKED BY Woody WU	SIZE A2	VER 1.2
	SHEET 14 OF 14	DATE 2022/8/18