BG600L-M3 QuecOpen Hardware Design

LPWA Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-02-25	Jake JIANG/ Hyman DING/ Watt ZHU	Creation of the document
1.0	2021-03-02	Jake JIANG/ Hyman DING/ Watt ZHU	First official release
1.1	2022-08-12	Lex LI/ Pearl GUO/ Matt YE	1. Added notes about module design (Chapter 3.1). 2. Deleted the AT command information related to PSM, e-I-DRX, sleep mode, turn-off and MAIN_RI. 3. Updated the USB serial driver information (Table 2). 4. Added the high-speed operation mode of the USB interface (Table 2 and 3.11). 5. Deleted the slave mode of SPI1 interface (Table 2 and Chapter 3.14). 6. Added the features of data communication, default frame format, hardware flow control and supported baud rates of main UART interface (Table 2 and Chapter 3.12); added a note about AT+IPR and AT+IFC for configuring main UART functions (Chapter 3.12); updated the reference design of UART3 (Figure 21). 7. Updated the minimum width of VBAT_RF trace from 2 mm to 2.7 mm and the minimum supply current from 2 A to 2.7 A (Chapter 3.6.2); updated the reference design of power supply (Figure 5). 8. Updated the active condition and reference design of PON_TRIG (Chapter 3.9). 9. Added a note of UART level-shift circuit (Chapter 3.12)

	10. Updated the typical resolution of ADC interface (Table 23). 11. Updated the introduction of USB_BOOT interface (Chapter 3.19). 12. Updated the typical TTFF value under open sky cold start XTRA enabled condition and accuracy (Table 31). 13. Updated the max. I_{VBAT} value (Table 38). 14. Deleted the peak value of the module's power consumption (Table 40 and 41). 15. Updated the max. slope parameter in the reflow zone (Chapter 8.2).

Contents

Table Index

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines BG600L-M3 module in QuecOpen® solution and describes its air interface and hardware interfaces which are connect with your applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the module. To facilitate application designs, it also includes some reference designs for your reference. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

2 Product Overview

2.1. General Description

The module is a baseband processor platform based on ARM Cortex A7. The maximum dominant frequency is up to 800 MHz. You can use the module as the basis for development of QuecOpen applications.

The module is an industrial-grade module for industrial and commercial applications only.

As an embedded IoT (LTE Cat M1, LTE Cat NB2 and EGPRS) wireless communication module, it provides data connectivity on GPRS/EGPRS and LTE HD-FDD networks, and supports half-duplex FDD operation on LTE network. It also provides GNSS function to meet your specific application demands.

The module is based on an architecture in which WWAN (LTE) and GNSS Rx chains share certain hardware blocks. However, the module does not support concurrent operation of WWAN and GNSS. The solution adopted in the module is a form of coarse time-division multiplexing (TDM) between WWAN and GNSS Rx chains. Given the relaxed latency requirements of most LPWA applications, time-division sharing of resources can be made largely transparent to applications. For details, see ***document [1]***.

Table 1: Frequency Bands and GNSS Types of the Module

Supported Bands	Power Class	GNSS
Cat M1: LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B25/B26/B27/B28/B66/B85 **Cat NB2** [1]**:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B25/B28/B66/B71/B85 **EGPRS:** GSM850/EGSM900/DCS1800/PCS1900	Power Class 5 (21 dBm)	GPS GLONASS BDS Galileo QZSS

[1] LTE Cat NB2 is backward compatible with LTE Cat NB1.

The SMD type module can be embedded into applications through its 68 LGA pins. With a compact profile of 18.7 mm × 16.0 mm × 2.1 mm, it can meet most requirements for M2M applications such as smart metering, tracking system, and wireless POS.

2.2. Key Features

Table 2: Key Features

Features	Details
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 5 (21 dBm +1.7/-3 dB) for LTE HD-FDD bands ● Class 4 (33 dBm ±2 dB) for GSM850 ● Class 4 (33 dBm ±2 dB) for EGSM900 ● Class 1 (30 dBm ±2 dB) for DCS1800 ● Class 1 (30 dBm ±2 dB) for PCS1900 ● Class E2 (27 dBm ±3 dB) for GSM850 8-PSK ● Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK ● Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK ● Class E2 (26 dBm ±3 dB) for PCS1900 8-PSK
LTE Features	● Supports 3GPP Rel-14 ● Supports LTE Cat M1 and LTE Cat NB2 ● Supports 1.4 MHz RF bandwidth for LTE Cat M1 ● Supports 200 kHz RF bandwidth for LTE Cat NB2 ● Cat M1: Max. 588 kbps (DL)/1119 kbps (UL) ● Cat NB2: Max. 127 kbps (DL)/158.5 kbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 33 (33 by default) ● Coding scheme: CS 1–4 ● Max. 107 kbps (DL)/85.6 kbps (UL) **EDGE:** ● Supports EDGE multi-slot class 33 (33 by default) ● Supports GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 296 kbps (DL)/236.8 kbps (UL)
Internet Protocol Features	● Supports PPP/TCP/UDP/SSL/TLS/FTP(S)/HTTP(S)/NITZ/PING/ MQTT/LwM2M/CoAP/IPv6 protocols ● Supports PAP and CHAP for PPP connections

SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interface	Supports 1.8 V USIM/SIM card only
USB Interface	● Compliant with USB 2.0 specification (slave mode only) ● Supports operations at high-speed, full-speed and low-speed modes ● Used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging and firmware upgrade ● Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–5.18, Android 4.x–12.x
UART Interfaces	**Main UART:** ● Used for AT command communication and data communication ● 115200 bps baud rate by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control **UART1/UART2/UART3:** ● Used for communication with peripherals ● Multiplexed from GPIOs (see ***Table 5*** for details)
I2C Interface	● Master mode only ● Supports fast-mode plus
SPI Interfaces	**SPI1/SPI2:** ● Supports master mode only ● Up to 50 MHz in master mode
GNSS	● GPS, GLONASS, BDS, Galileo and QZSS ● 1 Hz data update rate by default
AT Commands	● *3GPP TS 27.007* and *3GPP TS 27.005* AT commands ● Quectel enhanced AT commands
Network Indication	One NET_STATUS pin for network connectivity status indication
Antenna Interfaces	Main antenna (ANT_MAIN) and GNSS antenna (ANT_GNSS) interfaces
Physical Characteristics	● Dimensions: (18.7 ±0.2) mm × (16.0 ±0.2) mm × (2.1 ±0.2) mm ● Weight: approx. 1.25 g
Temperature Range	● Operating temperature range: -35 to +75 °C [2] ● Extended temperature range: -40 to +85 °C [3] ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	● USB interface ● DFOTA

[2] Within the operating temperature range, the module meets 3GPP specifications.
[3] Within the extended temperature range, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- Radio frequency
- Peripheral interfaces

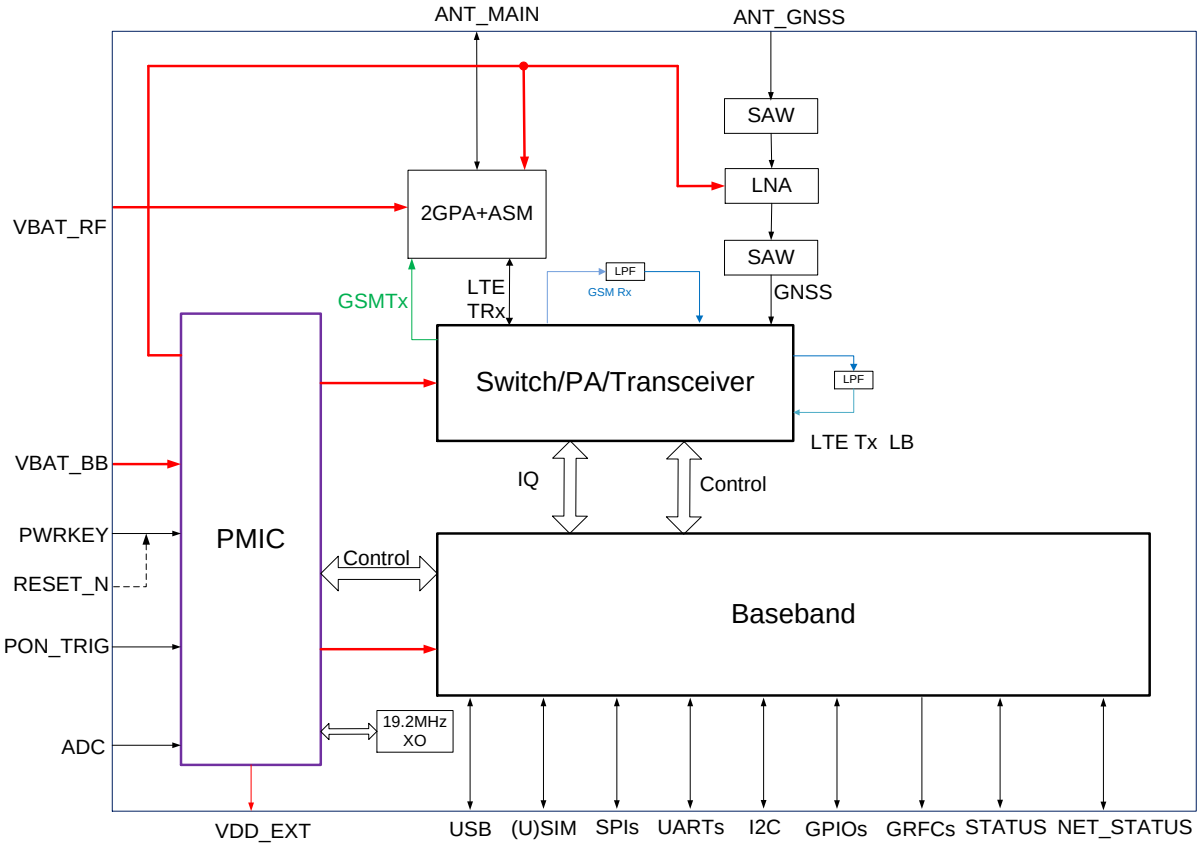


Figure 1: Functional Diagram

NOTE

1. The output voltage of PWRKEY is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull

down PWRKEY to GND permanently.
2. RESET_N is connected directly to PWRKEY inside the module.

2.4. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (LTE OPEN EVB) with accessories to control or test the module. For more details, see ***document [2]***.

3 Application Interfaces

The module is equipped with 68 LGA pins. The subsequent chapters provide detailed descriptions of the following interfaces:

- Power supply
- PON_TRIG interface
- (U)SIM interface
- USB interface
- UART interfaces
- I2C interface
- SPI interfaces
- ADC interface
- Status indication interfaces
- USB_BOOT interface
- GRFC interfaces

3.1. Pin Assignment

The following figure shows the pin assignment of the module.

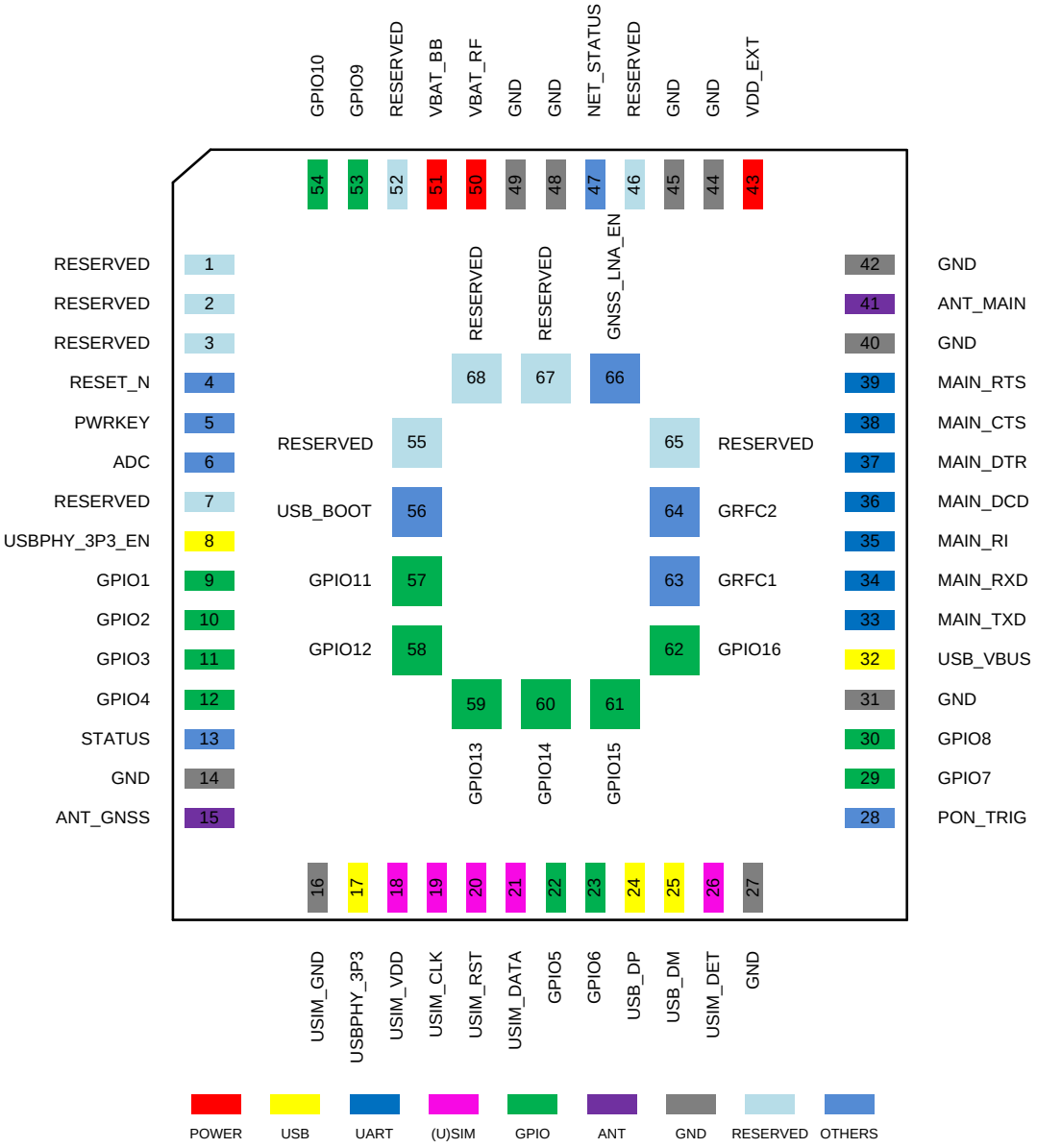


Figure 2: Pin Assignment (Top View)

NOTE

1. The output voltage of PWRKEY is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.

2. RESET_N connects directly to PWRKEY inside the module.
3. ADC input voltage must not exceed 1.8 V.
4. The input voltage range of USB_VBUS is 1.3–1.8 V.
5. GPIO1 (pin 9), NET_STATUS (pin 47), GRFC1 (pin 63) and GNSS_LNA_EN (pin 66) are BOOT_CONFIG pins. Never pull them up before startup, otherwise the module cannot power on normally.
6. Keep all RESERVED pins and unused pins unconnected.
7. Connect GND pins to ground in the design.

3.2. Pin Description

The following tables show the pin definition, alternate functions and GPIO pull-up/down resistance of the module.

Table 3: Definition of I/O Parameters

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input
PO	Power Output
PD	Pull Down
PU	Pull Up

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	51	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	-
VBAT_RF	50	PI	Power supply for the module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	-
VDD_EXT	43	PO	1.8 V output power supply for external circuits	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. If unused, keep this pin unconnected.
GND	14, 27, 31, 40, 42, 44, 45, 48, 49				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	5	DI	Turn on/off the module	Vnom = 1.5 V V_{IL}max = 0.45 V	Never pull down PWRKEY to GND permanently.
Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	4	DI	Reset the module	Vnom = 1.5 V V_{IL}max = 0.45 V	Multiplexed from PWRKEY (connected directly to PWRKEY inside the module). If unused, keep this pin unconnected.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	13	DO	Indicate the module's operation status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep this pin unconnected.
NET_STATUS	47	DO	Indicate the module's network		BOOT_CONFIG. Do not pull it up

			activity status		before startup. 1.8 V power domain. If unused, keep this pin unconnected.
PON_TRIG Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PON_TRIG	28	DI	Wake up the module from PSM	-	1.8 V power domain. Rising-edge triggered. Pulled-down by default. If unused, keep this pin unconnected.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	32	AI	USB connection detect	V_{IH}max = 1.8 V V_{IH}min = 1.3 V	-
USB_DP	24	AIO	USB differential data (+)	-	Compliant with USB 2.0 standard specification. Differential impedance of 90 Ω required.
USB_DM	25	AIO	USB differential data (-)	-	
USBPHY_3P3	17	PI	Power supply for USB PHY circuit	Vnom = 3.3 V	-
USBPHY_3P3_EN	8	DO	External LDO enable control for USB	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_DET	26	DI	(U)SIM card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin unconnected.
USIM_VDD	18	PO	(U)SIM card power supply	Vmax = 1.9 V Vmin = 1.7 V	Only 1.8 V (U)SIM card is supported.
USIM_RST	20	DO	(U)SIM card reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.

USIM_DATA	21	DIO	(U)SIM card data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
USIM_CLK	19	DO	(U)SIM card clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
USIM_GND	16	-	Specified ground for (U)SIM card	-	-
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_DTR	37	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins unconnected.
MAIN_RXD	34	DI	Main UART receive		
MAIN_TXD	33	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_CTS	38	DO	CTS: DTE clear to send signal from DCE		
MAIN_RTS	39	DI	RTS: DTE request to send signal to DCE	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	
MAIN_DCD	36	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_RI	35	DO	Main UART ring indication		
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC	6	AI	General-purpose ADC interface	Voltage range: 0.1–1.8 V	If unused, keep this pin unconnected.
USB_BOOT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	56	DI	Force the module into emergency download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin unconnected.

RF Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	41	AIO	Main antenna interface	-	50 Ω impedance
ANT_GNSS	15	AI	GNSS antenna interface	-	50 Ω impedance. If unused, keep this pin unconnected.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	1–3, 7, 46, 52, 55, 65, 67, 68				Keep these pins unconnected.
GRFC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	63	DO	Generic RF controller	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain. If unused, keep this pin unconnected.
GRFC2	64	DO	Generic RF controller	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin unconnected.
Other Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GNSS_LNA_EN	66	DO	External LNA enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain. If unused, keep this pin unconnected.
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	9	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain.

				V_{IH}min = 1.2 V V_{IH}max = 2.0 V	If unused, keep this pin unconnected.
GPIO2	10	DIO			
GPIO3	11	DIO			
GPIO4	12	DIO			
GPIO5	22	DIO			
GPIO6	23	DIO			1.8 V power domain. If unused, keep these pins unconnected.
GPIO7	29	DIO			
GPIO8	30	DIO			
GPIO9	53	DIO			
GPIO10	54	DIO			
GPIO11	57	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins unconnected.
GPIO12	58	DIO			
GPIO13	59	DIO			
GPIO14	60	DIO			
GPIO15	61	DIO			
GPIO16	62	DIO			

NOTE

1. The output voltage of PWRKEY is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.
2. RESET_N is connected directly to PWRKEY inside the module.
3. The input voltage range of USB_VBUS is 1.3–1.8 V.
4. ADC input voltage must not exceed 1.8 V.
5. USBPHY_3P3 and USBPHY_3P3_EN pins are used for USB PHY circuits.
6. GPIO1 (pin 9), NET_STATUS (pin 47), GRFC1 (pin 63) and GNSS_LNA_EN (pin 66) are BOOT_CONFIG pins. Never pull them up before startup, otherwise the module cannot power on normally.
7. Keep all RESERVED pins and unused pins unconnected.
8. Connect GND pins to ground in the design.

3.3. Pin Multiplexing Relationship

Table 5: Multiplexing Pins

Pin Name	Pin No.	Function 1	Function 2	Function 3	Function 4	Reset	Interrupt Wakeup	Comment
GPIO1	9	GPIO_4	UART3_TXD	SPI1_MOSI	-	PD	√	BOOT_CONFIG
GPIO2	10	GPIO_5	UART3_RXD	SPI1_MISO	-	PD	√	
GPIO3	11	GPIO_6	-	SPI1_CS_N	-	PD	√	
GPIO4	12	GPIO_7	-	SPI1_CLK	-	PD	-	
GPIO5	22	GPIO_12	UART2_TXD	SPI2_MOSI	-	PD	-	
GPIO6	23	GPIO_13	UART2_RXD	SPI2_MISO	-	PD	√	
GPIO7	29	GPIO_0	UART1_TXD	-	-	PD	√	
GPIO8	30	GPIO_1	UART1_RXD	-	-	PD	√	
GPIO9	53	GPIO_15	-	SPI2_CLK	-	PD	-	
GPIO10	54	GPIO_14	-	SPI2_CS_N	-	PD	√	
GPIO11	57	GPIO_2	-	-	I2C1_SDA	PD	√	

GPIO12	58	GPIO_3	-	-	I2C1_SCL	PD	-
GPIO13	59	GPIO_24	-	-	-	PD	-
GPIO14	60	GPIO_23	-	-	-	PD	-
GPIO15	61	GPIO_21	-	-	-	PD	√
GPIO16	62	GPIO_22	-	-	-	PD	√

NOTE

1. The pin functions 1/2/3/4 take effect only after software configuration.
2. The BOOT_CONFIG pin (pin 9) cannot be pulled up before startup, otherwise the module cannot power on normally.
3. "√" means supported.

Table 6: Pull-up/down Resistance of GPIOs

Symbol	Description	Min.	Max.	Unit
R_{PU}	Pull-up resistance	55	390	kΩ
R_{PD}	Pull-down resistance	55	390	kΩ

3.4. Operating Modes

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Connected	The module is connected to network. Its power consumption varies with the network setting and data transfer rate.
	Idle	The module remains registered on network, and is ready to send and receive data. In this mode, the software is active.
Extended Idle Mode DRX (e-I-DRX)	The module and the network may negotiate over non-access stratum signaling the use of e-I-DRX for reducing power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.	
Airplane Mode	**AT+CFUN=4** can set the module into airplane mode where the RF function is invalid.	
Minimum Functionality Mode	**AT+CFUN=0** can set the module into minimum functionality without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Sleep Mode	The module remains the ability to receive paging message, SMS and TCP/UDP data from the network normally. In this mode, the power consumption is reduced to a low level.	
Power OFF Mode	The module's power supply is shut down by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT) is still maintained.	
Power Saving Mode (PSM)	PSM is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. The power consumption is reduced to a minimized level.	

NOTE

1. During e-I-DRX, it is recommended to use UART interface for data communication, as the use of USB interface will increase power consumption.
2. See ***document [3]*** for details about **AT+CFUN**.

3.5. Power Saving

3.5.1. Airplane Mode

When the module enters airplane mode, the RF function does not work, and all AT commands correlative with RF function are inaccessible. This mode can be set via the following AT command.

AT+CFUN=<fun> provides choice of the functionality level, through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

NOTE

The execution of **AT+CFUN** will not affect GNSS function.

3.5.2. Power Saving Mode (PSM)

The module minimizes its power consumption through entering PSM. The mode is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. Therefore, the module in PSM cannot immediately respond to users' requests.

When the module wants to use PSM, it shall request an Active Time value during every Attach and TAU procedures. If the network supports PSM and accepts that the module uses PSM, the network confirms usage of PSM by allocating an Active Time value to the module. If the module wants to change the Active Time value, e.g. when the conditions are changed in the module, the module requests the value it wants in the TAU procedure.

If PSM is supported by the network, then it can be enabled via *qapi_QT_NW_PSM_Cfg_Set()*. See ***document [4]*** for details about the API function.

Any of the following methods can wake up the module from PSM:

- Wake up the module from PSM through a rising edge on PON_TRIG (recommended).
- Wake up the module by driving PWRKEY low.
- When the TAU timer expires, the module wakes up from PSM automatically.

3.5.3. Extended Idle Mode DRX (e-I-DRX)

The module (UE) and the network may negotiate over non-access stratum signalling the use of e-I-DRX for reducing its power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.

Applications that want to use e-I-DRX need to consider specific handling of mobile terminating services or data transfers, and in particular they need to consider the delay tolerance of mobile terminated data.

In order to negotiate the use of e-I-DRX, the UE requests e-I-DRX parameters during Attach procedure and RAU/TAU procedure. The EPC may reject or accept the UE request for enabling e-I-DRX. In case the EPC accepts e-I-DRX, the EPC based on operator policies and, if available, the e-I-DRX cycle length value in the subscription data from the HSS, may also provide different values of the e-I-DRX parameters than what were requested by the UE. If the EPC accepts the use of e-I-DRX, the UE applies e-I-DRX based on the received e-I-DRX parameters. If the UE does not receive e-I-DRX parameters in the relevant accept message because the EPC rejected its request or because the request was received by EPC not supporting e-I-DRX, the UE shall apply its regular discontinuous reception.

If e-I-DRX is supported by the network, then it can be enabled by *qapi_QT_NW_eDRX_Cfg_Set()*. See ***document [4]*** for details about the API function.

3.5.4. Sleep Mode

The module is able to reduce its power consumption to a lower value during sleep mode. The following sub-chapters describe the power saving procedure of the module.

3.5.4.1. UART Application

If the host communicates with the module via the main UART interface, the following preconditions enable the module to enter sleep mode.

- Execute *qapi_QT_QSCLK_Enable_Set()* to enable sleep mode. See ***document [4]*** for details about the API function.
- Drive MAIN_DTR high.

The following figure shows the connection between the module and the host.

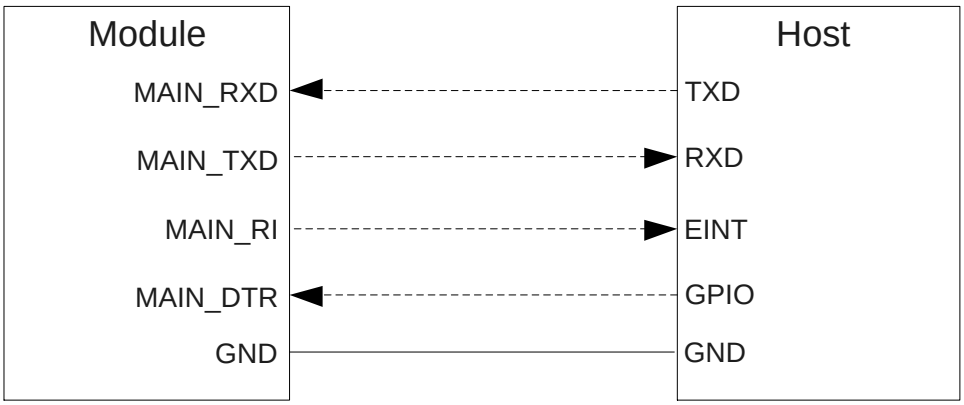


Figure 3: Sleep Mode Application via UART

- When the module has a URC to report, MAIN_RI will wake up the host. See ***Chapter 3.16*** for details about MAIN_RI behavior.
- Driving MAIN_DTR low will wake up the module.

3.6. Power Supply

3.6.1. Power Supply Pins

The module provides two VBAT pins for connection with an external power supply. There are two separate voltage domains for VBAT.

Table 8: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	50	Power supply for the module's RF part	3.3	3.8	4.3	V
VBAT_BB	51	Power supply for the module's baseband part	3.3	3.8	4.3	V
GND	14, 27, 31,40, 42, 44, 45,48, 49.	Ground	-	-	-	-

3.6.2. Decrease Voltage Drop

The power supply range of the module is 3.3–4.3 V. Make sure that the input voltage never drops below 3.3 V.

The following figure shows the module's voltage drop during burst transmission in 2G network. The voltage drop is less in LTE Cat M1 and LTE Cat NB2 networks.

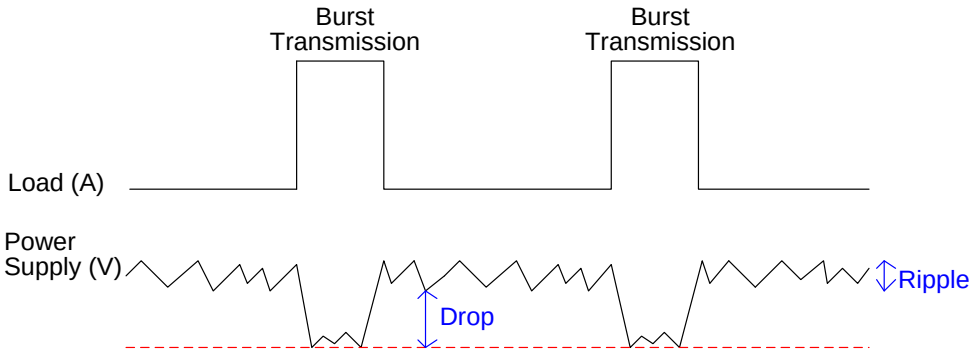


Figure 4: Power Supply Limits during Burst Transmission

To decrease voltage-drop, bypass capacitors of about 100 µF with low ESR should be used, and multi-layer ceramic chip capacitor (MLCC) arrays should also be reserved due to their low ESR. It is recommended to use seven ceramic capacitors (220 nF, 47 nF, 150 pF, 100 pF, 68 pF, 33 pF, 10 pF) for composing the MLCC array for VBAT_BB, three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array for VBAT_RF, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source that can supply power along two star-structured sub paths. The width of VBAT_BB trace should be no less than 0.6 mm, and the width of VBAT_RF trace should be no less than 2.7 mm. In principle, the longer the VBAT trace is, the wider it will be.

To get a stable power source, it is suggested to use two TVSs with low leakage current and suitable reverse stand-off voltage, and it is recommended to place them as close to the VBAT pins as possible.

Inner layer design should be adopted for VBAT_BB and VBAT_RF trace. Place the ferrite bead at the closest position to VBAT_BB. Performance requirements for ferrite bead:

- Current rating ≥ 600 mA and low DC resistance to avoid voltage drop during instantaneous high power consumption.
- ≥ 800 Ω impedance @ 700–960 MHz.

The following figure shows the star structure of the power supply.

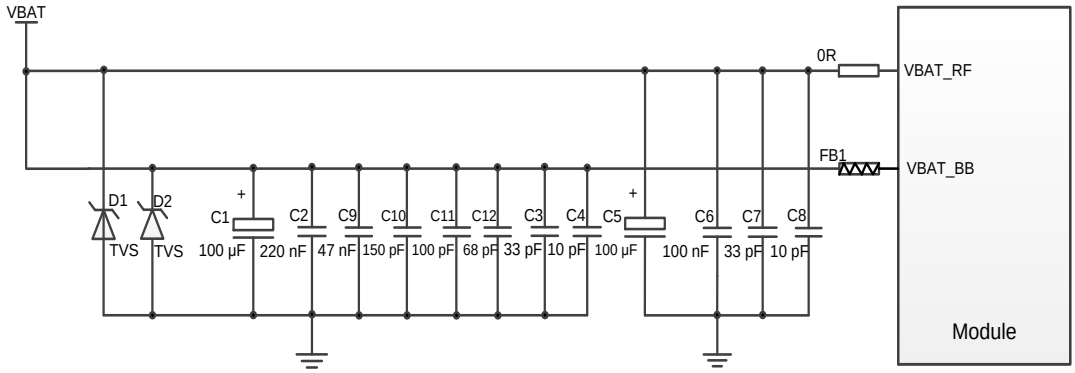


Figure 5: Reference Design of Power Supply

Power design for a module is critical to its performance. The power supply of the module should be able to provide sufficient current of 2.7 A at least, and it is recommended to select a DC-DC converter chip or an LDO chip with ultra-low leakage current and current output no less than 2.7 A for the power supply design.

3.6.3. Power Supply Voltage Monitoring

AT+CBC can be used to monitor the VBAT_BB voltage value. For more details, see ***document [3]***.

3.7. Turn On and Off Scenarios

3.7.1. Turn On with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	IO	Description	DC Characteristics	Comment
PWRKEY	5	DI	Turn on/off the module	Vnom = 1.5 V V_{IL}max = 0.45 V	The output voltage is 1.5 V because of the voltage drop inside the chipset.

When the module is in power-off mode, it can be turned on by driving PWRKEY low for 500–1000 ms. It is recommended to use an auto power-on circuit to control PWRKEY, as shown below.

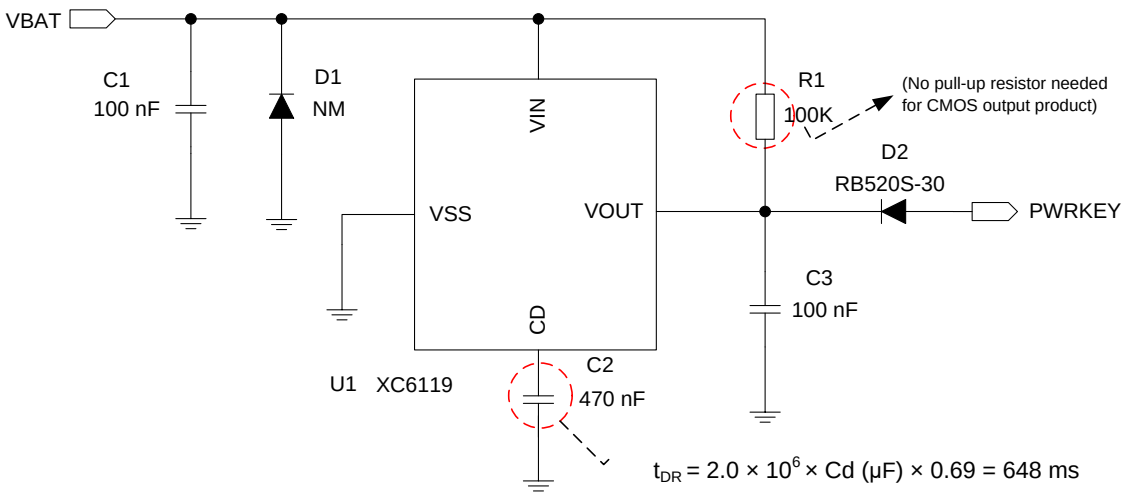


Figure 6: Auto Power-on Circuit

Visit https://www.torexsemi.com for more information on the XC6119 voltage detector.

NOTE

With the above circuit, the module automatically powers on when the power supply is switched on, and keeps PWRKEY at a high level after successful power-on. With this design, if you intend to power on the module again after you power it off with an API, switch off the power supply of the module and remain in turn-off state for at least 200 ms before you switch on the power supply to enable automatic power-on of the module.

If the device has an extra MCU, it is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

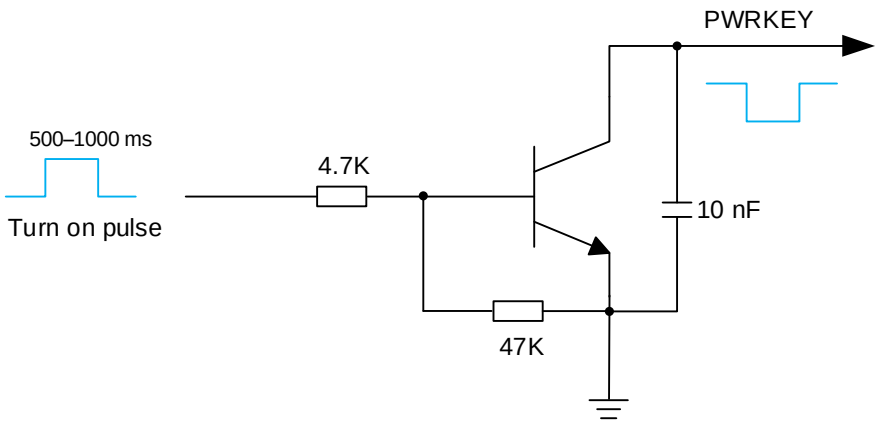


Figure 7: Turn On the Module with a Driving Circuit

Another way to control PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from the finger. Therefore, a TVS is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

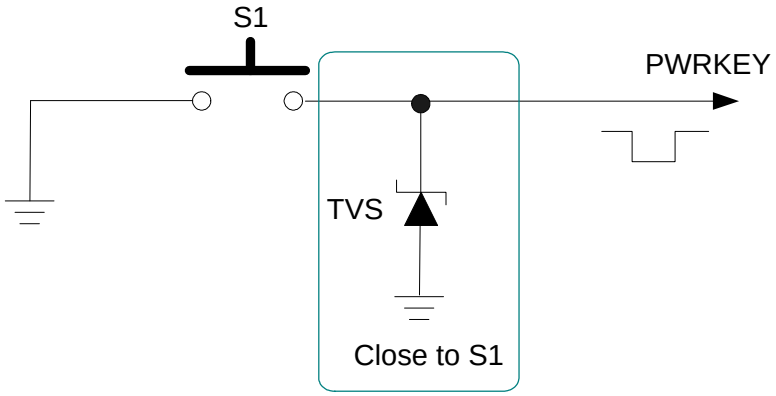


Figure 8: Turn On the Module with a Button

The power-up scenario is illustrated in the following figure.

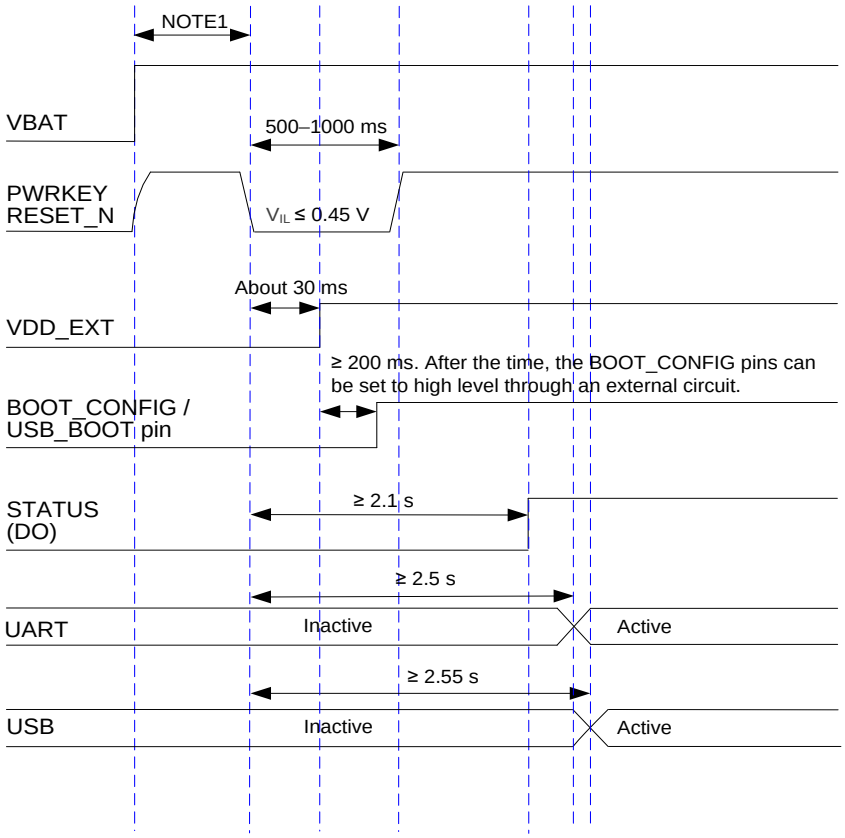


Figure 9: Power-up Timing

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY and keep the interval no less than 30 ms.
2. The output voltage of PWRKEY is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.

3.7.2. Turn Off

Either of the following methods can be used to turn off the module normally:

- Turn off the module with PWRKEY.
- Turn off the module with API.

3.7.2.1. Turn Off with PWRKEY

Driving PWRKEY low for 650–1500 ms and then releasing it, the module will execute power-down procedure.

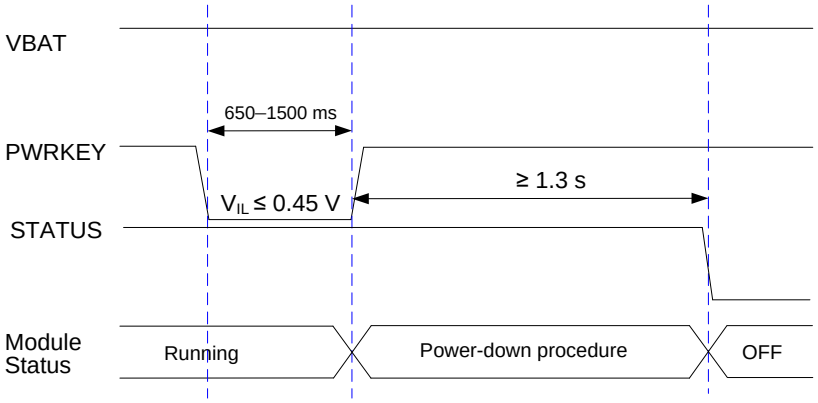


Figure 10: Power-down Timing

3.7.2.2. Turn Off with an API

It is also a safe way to turn off the module with *qapi_QT_Shutdown_Device()*, which is similar to turning off the module with PWRKEY.

See ***document [4]*** for details about the API function.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down, the power supply can be cut off.
2. While turning off the module with an API, keep PWRKEY at high level after the execution of power-off command. Otherwise, the module will be turned on again after it turns off.

3.8. Reset

RESET_N is used to reset the module. Due to platform limitations, the chipset has integrated the reset function into PWRKEY, and RESET_N is connected directly to PWRKEY inside the module.

The module can be reset by driving RESET_N low for 2–3.8 s.

Table 10: Pin Definition of RESET_N

Pin Name	Pin No.	IO	Description	DC Characteristics	Comment
RESET_N	4	DI	Reset the module	V_{IL}max = 0.45 V	Multiplexed from PWRKEY (connected directly to PWRKEY inside the module)

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control RESET_N.

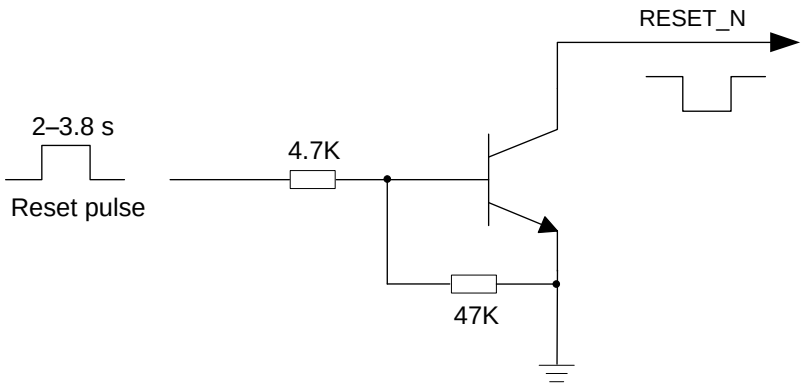


Figure 11: Reference Circuit of RESET_N with a Driving Circuit

Another way to control the RESET_N is by using a button directly.

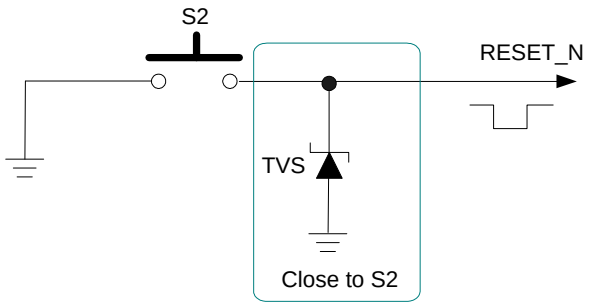


Figure 12: Reference Circuit of RESET_N with a Button

The reset scenario is illustrated in the following figure.

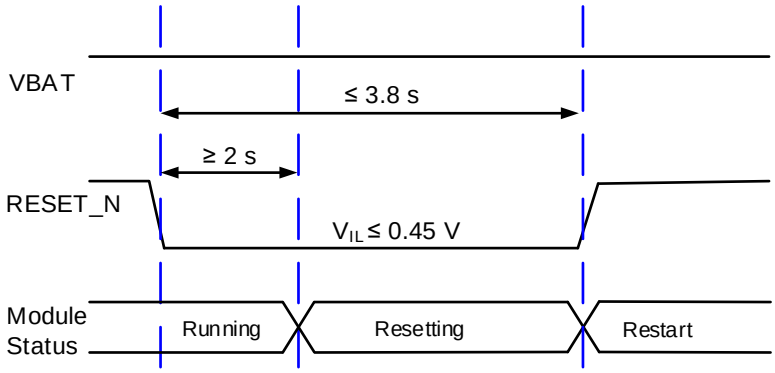


Figure 13: Reset Timing

NOTE

Ensure that there is no large capacitance on RESET_N.

3.9. PON_TRIG Interface

The module provides one PON_TRIG pin to wake up the module from PSM. When the pin detects a rising edge and keeps at a high level for at least 30 ms, the module wakes up from PSM.

Table 11: Pin Definition of PON_TRIG

Pin Name	Pin No.	I/O	Description	Comment
PON_TRIG	28	DI	Wake up the module from PSM	Rising-edge triggered. Pulled-down by default. 1.8 V power domain.

A reference circuit is shown in the following figure.

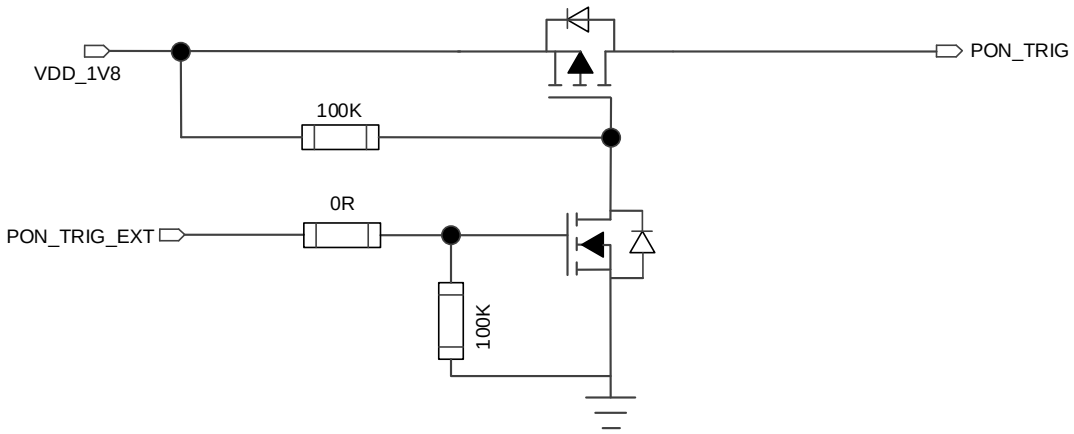


Figure 14: Reference Circuit of PON_TRIG

NOTE

VDD_1V8 is powered by an external LDO.

3.10. (U)SIM Interface

The module supports 1.8 V (U)SIM card only. The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements.

Table 12: Pin Definition of the (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_DET	26	DI	(U)SIM card hot-plug detect	1.8 V power domain.
USIM_VDD	18	PO	(U)SIM card power supply	Only 1.8 V (U)SIM card is supported.

USIM_RST	20	DO	(U)SIM card reset	1.8 V power domain.
USIM_DATA	21	DIO	(U)SIM card data	1.8 V power domain.
USIM_CLK	19	DO	(U)SIM card clock	1.8 V power domain.
USIM_GND	16		Specified ground for (U)SIM card	

The module supports (U)SIM card hot-plug via USIM_DET, and both high and low level detections are supported. The function is disabled by default, and see **AT+QSIMDET** in ***document [3]*** for more details.

The following figure shows a reference design of (U)SIM interface with an 8-pin (U)SIM card connector.

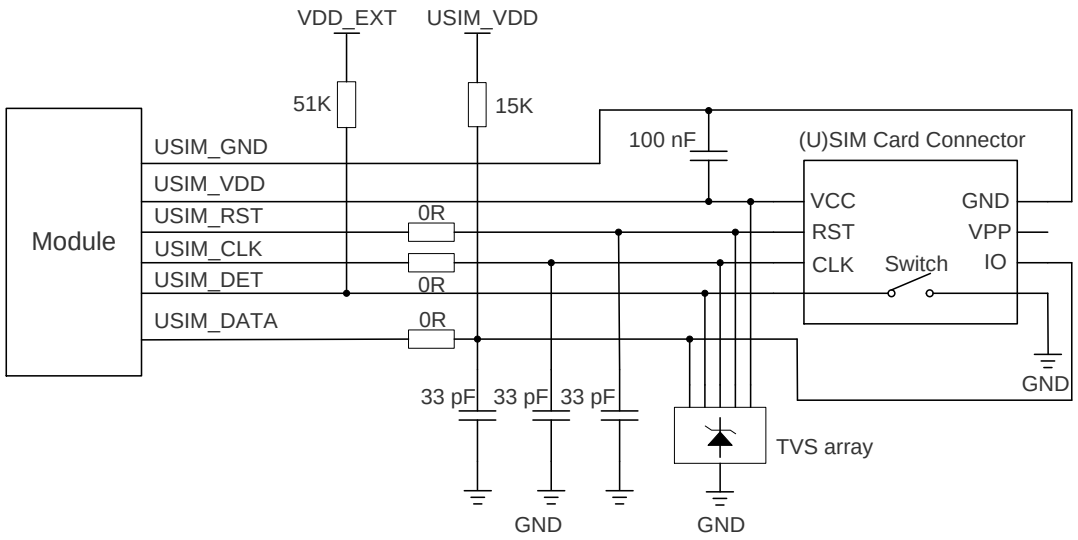


Figure 15: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

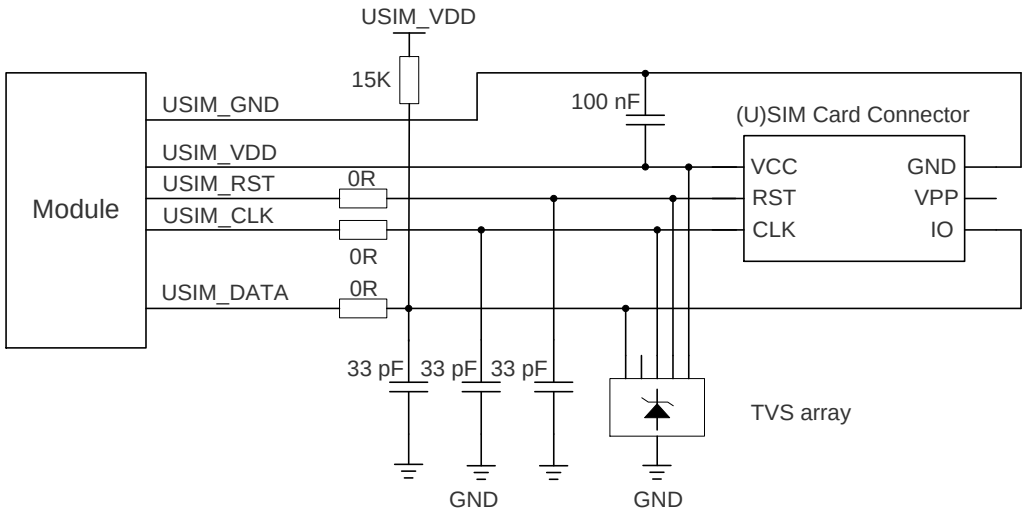


Figure 16: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length less than 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground trace between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND is less than 1 μF, and place it as close to (U)SIM card connector as possible. If the system ground plane is complete, USIM_GND can be connected to the system ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep their traces away from each other and shield them with ground. USIM_RST should also be shielded with ground.
- To offer good ESD protection, it is recommended to add a TVS array with parasitic capacitance not exceeding 15 pF. To facilitate debugging, it is recommended to reserve series resistors for the (U)SIM signals of the module. The 33 pF capacitors are used for filtering interference of EGSM900. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.

3.11. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification. The USB interface only supports slave mode and supports operation at low-speed (1.5 Mbps), full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 13: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	32	AI	USB connection detect	Input range: 1.3–1.8 V
USB_DP	24	AIO	USB differential data (+)	Differential impedance of 90 Ω required
USB_DM	25	AIO	USB differential data (-)	
USBPHY_3P3	17	PI	Power supply for USB PHY circuit	Vnom = 3.3 V
USBPHY_3P3_EN	8	DO	External LDO enable control for USB	1.8 V power domain
GND	31		Ground	

For more details about USB 2.0 specification, visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade and software debugging in application designs. It is not recommended to use USB interface for data communication, as this will increase the power consumption. The following figures show reference designs of USB PHY and USB interface.

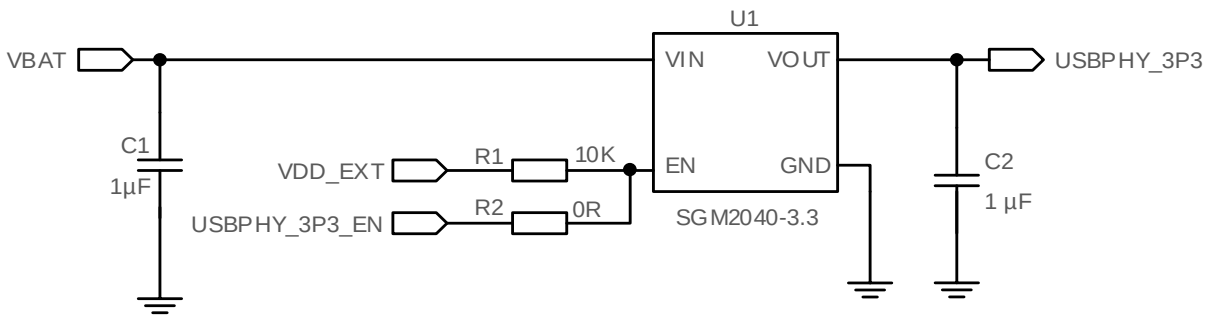


Figure 17: Reference Design of USB PHY

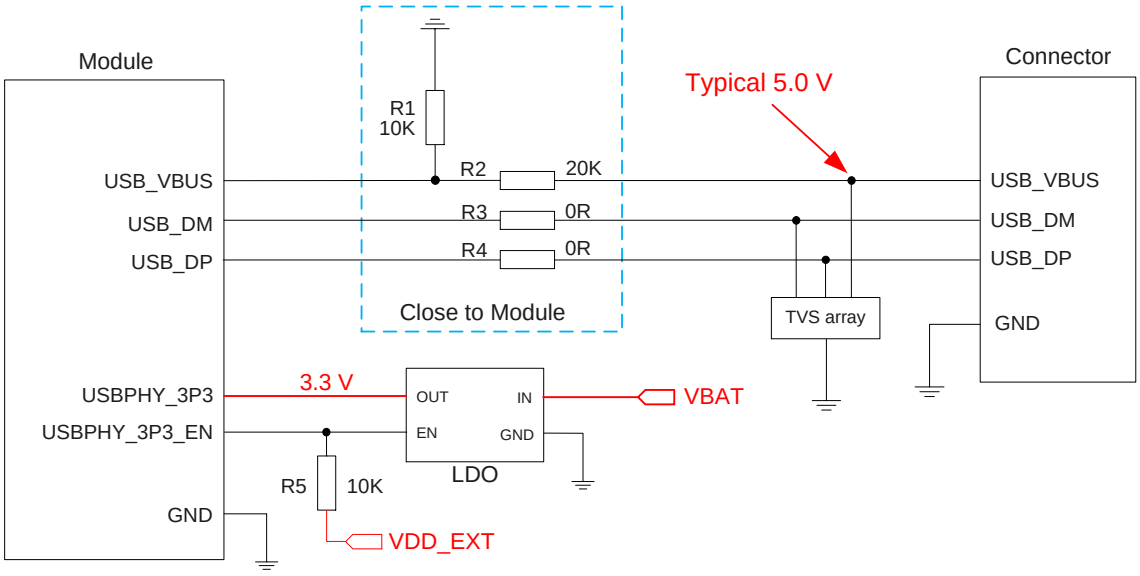


Figure 18: Reference Design of USB Interface

To ensure the integrity of USB data line signals, resistors R3 and R4 should be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

To meet USB 2.0 specification, comply with the following principles in the USB interface designing .

- It is important to route the USB signal traces as differential pairs with ground. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection components might influence USB data traces, so pay attention to device selection. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection devices as close to the USB connector as possible.

NOTE

1. The USB interface supports slave mode only.
2. The input voltage range of USB_VBUS is 1.3–1.8 V.

3.12. UART Interfaces

The module provides four UART interfaces: the main UART, UART1, UART2 and UART3.

- The main UART interface is designed for AT command communication and data transmission. The supported baud rates are 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600, 2000000, 2900000, 3000000, 3200000, 3686400 and 4000000 bps with a default baud rate of 115200 bps.
- UART1, UART2 and UART3 interfaces are used for communication with peripherals, and they are multiplexed from GPIOs.

Table 14: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_DTR	37	DI	Main UART data terminal ready	1.8 V power domain
MAIN_RXD	34	DI	Main UART receive	1.8 V power domain
MAIN_TXD	33	DO	Main UART transmit	1.8 V power domain
MAIN_CTS	38	DO	CTS: DTE clear to send signal from DCE	1.8 V power domain. CTS: Connect to DTE's CTS
MAIN_RTS	39	DI	RTS: DTE request to send signal to DCE	1.8 V power domain. RTS: Connect to DTE's RTS
MAIN_DCD	36	DO	Main UART data carrier detect	1.8 V power domain
MAIN_RI	35	DO	Main UART ring indication	1.8 V power domain

Table 15: Pin Definition of UART1 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4	Comment
GPIO7	29	DIO	GPIO_0	UART1_TXD	-	-	1.8 V power domain
GPIO8	30	DIO	GPIO_1	UART1_RXD	-	-	1.8 V power domain

Table 16: Pin Definition of UART2 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4	Comment
GPIO5	22	DIO	GPIO_12	UART2_TXD	SPI2_MOSI	-	1.8 V power domain
GPIO6	23	DIO	GPIO_13	UART2_RXD	SPI2_MISO	-	1.8 V power domain

Table 17: Pin Definition of UART3 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4	Comment
GPIO1	9	DIO	GPIO_4	UART3_TXD	SPI1_MOSI	-	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain.
GPIO2	10	DIO	GPIO_5	UART3_RXD	SPI1_MISO	-	1.8 V power domain.

NOTE

1. The pin functions 1/2/3/4 take effect only after software configuration.
2. GPIO1 (pin 9) is a BOOT_CONFIG pin. Do not pull it up before startup.
3. **AT+IPR** can be used to set the baud rate of the main UART interface, and **AT+IFC** can be used to enable/disable the hardware flow control (the function is disabled by default). See ***document [3]*** for more details about these AT commands.

The module provides 1.8 V UART interfaces. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. The voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. Visit http://www.ti.com for more information.

The following figure shows a reference design of the main UART interface.

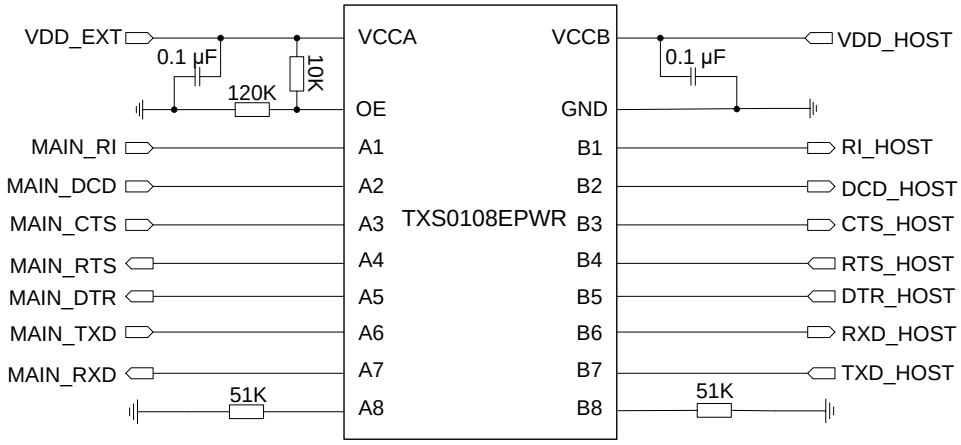


Figure 19: Main UART Reference Design (IC Solution)

Another example with transistor circuit is shown as below. For the design of circuits in dotted lines, see that of circuits in solid lines, but pay attention to the direction of connection.

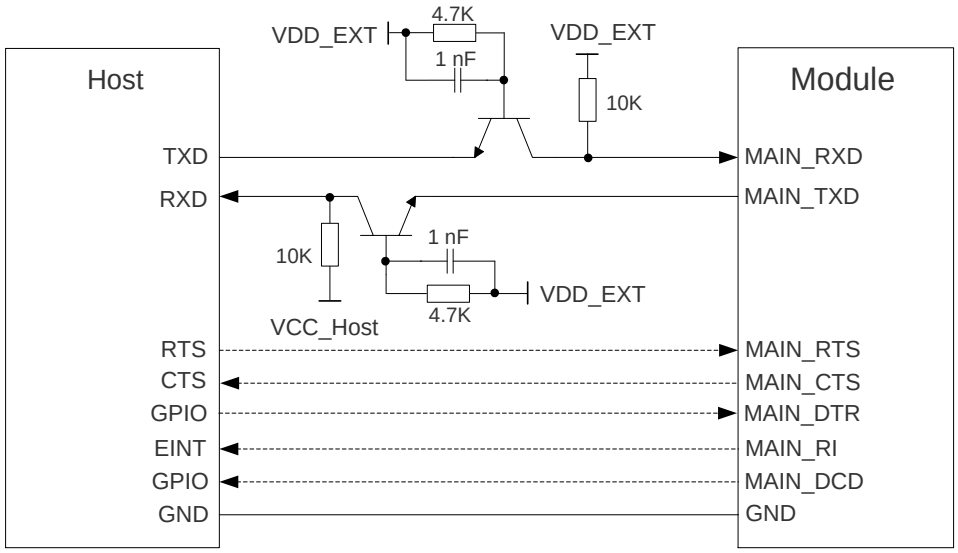


Figure 20: Main UART Reference Design (Transistor Solution)

NOTE

1. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

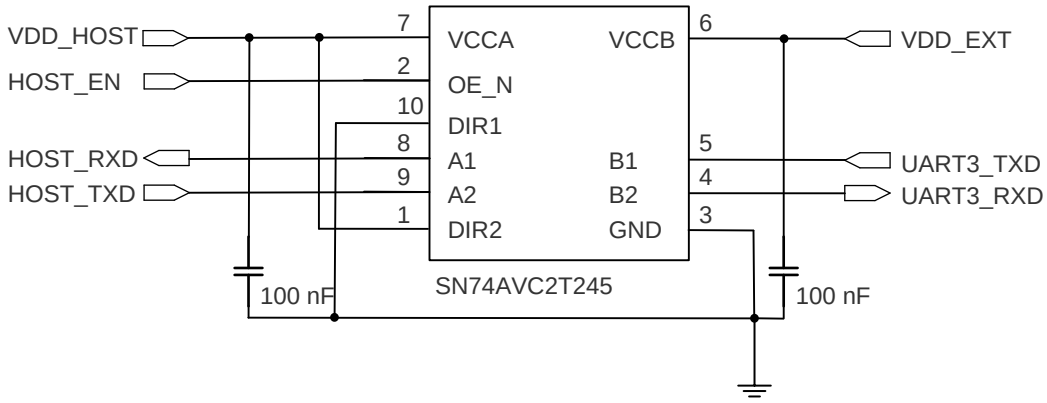


Figure 21: UART3 Reference Design (IC Solution)

NOTE

UART3 contains a BOOT_CONFIG pin (pin 9). Therefore, neither the IC solution with pull-up circuit nor the transistor solution with signal transistor/MOSFET circuit is not applicable to it. The dual-transistor circuit solution is recommended for UART3. It is recommended to use a level-shifting chip without internal pull-up.

3.13. I2C Interface

The module provides one Inter-Integrated Circuit (I2C) interface for data communication. The interface supports fast-mode plus and master mode only.

The pins of I2C interface are multiplexed from GPIOs and are open drain signals that must be pulled up to 1.8 V. The pull-up resistors should be provided externally.

Table 18: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4	Comment
GPIO11	57	DIO	GPIO_2	-	-	I2C1_SDA	1.8 V power domain.
GPIO12	58	DIO	GPIO_3	-	-	I2C1_SCL	1.8 V power domain.

NOTE

The pin functions 1/2/3/4 take effect only after software configuration.

The following figure shows a reference design of I2C interface with an external I2C interface sensor.

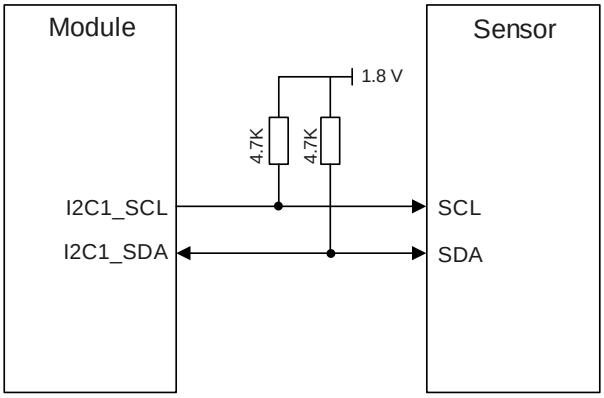


Figure 22: Reference Design of I2C Interface with an External I2C Interface Sensor

3.14. SPI Interfaces

The module provides two SPI interfaces.

SPI1 and SPI2 interfaces support master mode only, up to 50 MHz.

Table 19: Pin Definition of SPI1 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4	Comment
GPIO1	9	DIO	GPIO_4	UART3_TXD	SPI1_MOSI	-	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain.
GPIO2	10	DIO	GPIO_5	UART3_RXD	SPI1_MISO	-	1.8 V power domain.
GPIO3	11	DIO	GPIO_6	-	SPI1_CS_N	-	1.8 V power domain.
GPIO4	12	DIO	GPIO_7	-	SPI1_CLK	-	1.8 V power domain.

Table 20: Pin Definition of SPI2 Interface

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4	Comment
GPIO5	22	DIO	GPIO_12	UART2_TXD	SPI2_MOSI	-	1.8 V power domain
GPIO6	23	DIO	GPIO_13	UART2_RXD	SPI2_MISO	-	1.8 V power domain
GPIO9	53	DIO	GPIO_15	-	SPI2_CLK	-	1.8 V power domain
GPIO10	54	DIO	GPIO_14	-	SPI2_CS_N	-	1.8 V power domain

NOTE

1. The pin functions 1/2/3/4 take effect only after software configuration.
2. GPIO1 (pin 9) is a BOOT_CONFIG pin. Do not pull it up before startup.

The following figure shows the SPI master timing diagram. The related parameters of SPI master timing at 50 MHz are shown in the table below.

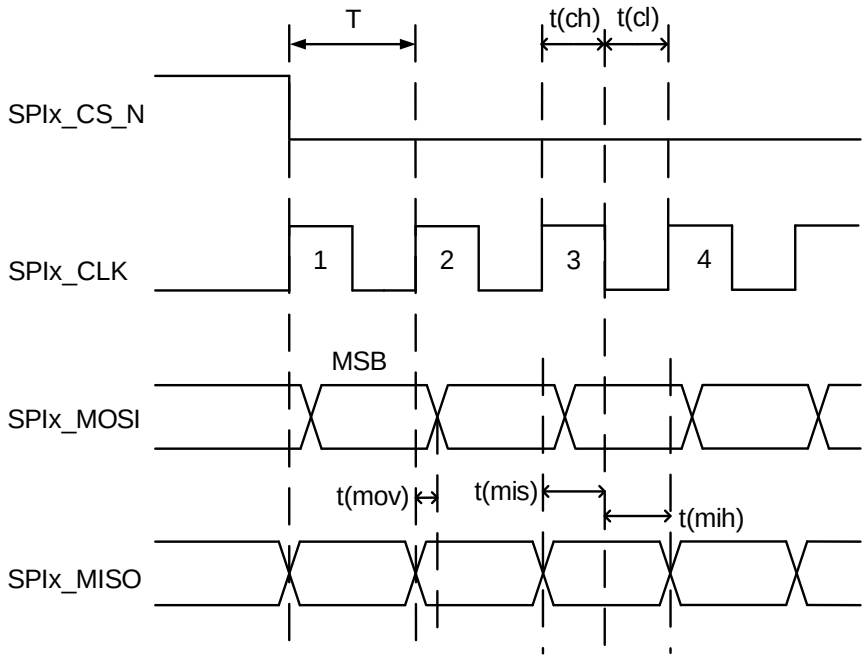


Figure 23: SPI Master Timing Diagram

Table 21: Parameters of SPI Interface Timing at 50 MHz

Parameter	Description	Min.	Typ.	Max.	Unit
T	SPI clock period: 50 MHz	20.0	-	-	ns
t (ch)	Clock high	9.0	-	-	ns
t (cl)	Clock low	9.0	-	-	ns
t (mov)	Master output valid	5.0	-	5.0	ns
t (mis)	Master input setup	5.0	-	-	ns
t (mih)	Master input hold	1.0	-	-	ns

NOTE

The power domain of the SPI interface is 1.8 V. A voltage-level translator should be used between the module and the host if your application is equipped with a 3.3 V processor or device interface.

3.15. ADC Interface

The module provides one ADC (Analog-to-Digital Converter) interface. **AT+QADC=0** can be used to read the voltage value on ADC. For more details about the AT command, see ***document [3]***.

To improve the accuracy of ADC voltage values, the trace of ADC should be shielded with ground.

Table 22: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC	6	AI	General-purpose ADC interface	Voltage range: 0.1–1.8 V

Table 23: Characteristics of ADC Interface

Parameter	Min.	Typ.	Max.	Unit
Voltage Range	0.1	-	1.8	V
Resolution (LSB)	-	64.879	-	μV

Analog Bandwidth	-	500	-	kHz
Sample Clock	-	4.8	-	MHz
Input Resistance	10	-	-	mΩ

NOTE

1. ADC input voltage must not exceed 1.8 V.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application, and the divider resistor accuracy should be no less than 1 %.

3.16. MAIN_RI

AT+QCFG="risignaltype","physical" can be used to configure MAIN_RI behavior. No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI.

The default behaviors of MAIN_RI are shown as below.

Table 24: Default Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI keeps at a high level.
URC	MAIN_RI outputs a 120 ms low pulse when a new URC is returned.

The default MAIN_RI behaviors can be configured flexibly by **AT+QCFG="urc/ri/ring"**. For more details about **AT+QCFG**, see ***document [5]***.

NOTE

A URC can be outputted from the main UART port and USB modem port (default) through configuration via *qapi_QT_URC_Port_Set()*.See ***document [4]*** for details about the API function.

3.17. Network Status Indication

The module provides one network status indication pin NET_STATUS. The pin is used to drive a network status indication LED. The following tables describe the pin definition and logic level changes of NET_STATUS in different network activity status.

Table 25: Pin Definition of NET_STATUS

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	47	DO	Indicate the module's network activity status	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain

Table 26: Operating Status of NET_STATUS

Pin Name	Indicator Status (Logic Level Changes)	Network Status
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing

A reference design is shown in the following figure.

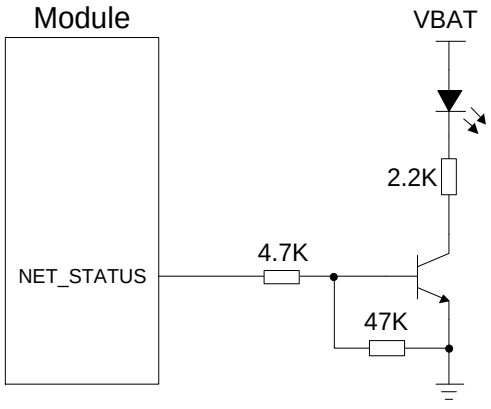


Figure 24: Reference Design of NET_STATUS

NOTE

NET_STATUS is a BOOT_CONFIG pin. Do not pull it up before startup.

3.18. STATUS

The STATUS pin is used to indicate the operation status of the module. It outputs a high level when the module powers on.

Table 27: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	13	DO	Indicate the module's operation status	1.8 V power domain

The following figure shows a reference circuit of STATUS.

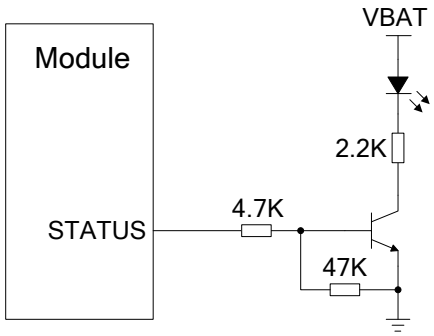


Figure 25: Reference Design of STATUS

3.19. USB_BOOT Interface

The module provides a USB_BOOT pin. You can pull up USB_BOOT to VDD_EXT before powering up the module, then the module will enter emergency download mode when powered up. In this mode, the module supports firmware upgrade over USB 2.0 interface. During development or factory production, USB_BOOT can force the module to boot from USB port for firmware upgrade.

Table 28: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	56	DI	Force the module into emergency download mode	1.8 V power domain. Active high. If unused, keep it open.

The following figure shows a reference design of USB_BOOT interface.

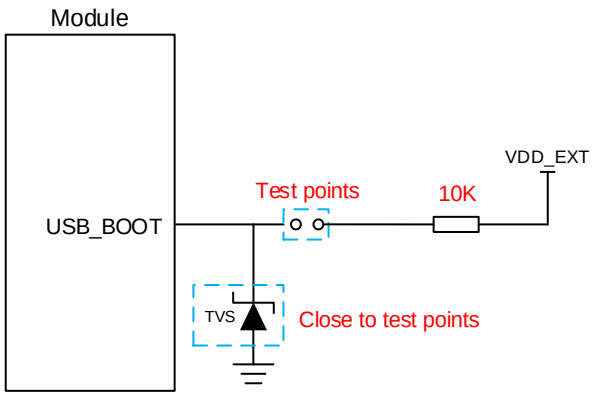


Figure 26: Reference Design of USB_BOOT Interface

The following figure shows the timing of USB_BOOT.

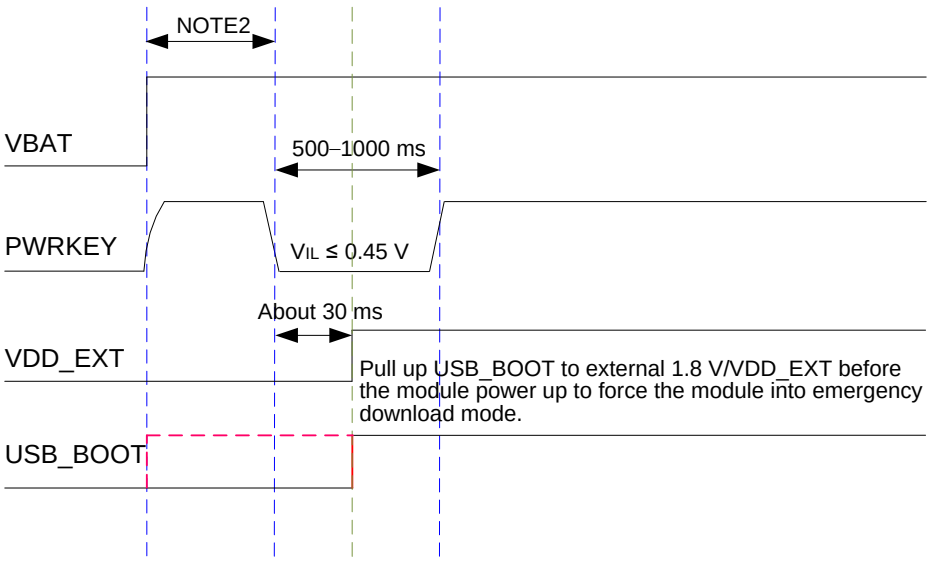


Figure 27: Timing of Turning on Module with USB_BOOT

NOTE

1. It is recommended to reserve the above circuit design during application design.
2. Ensure that VBAT is stable before pulling down PWRKEY. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY is no less than 30 ms.
3. When using MCU to control the module entering emergency download mode, follow the above timing sequence. Connecting the test points as shown in ***Figure 26*** can manually force the module into download mode.

3.20. GRFC Interfaces

The module provides two generic RF control interfaces for the control of external antenna tuners.

Table 29: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	63	DO	Generic RF controller	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain.
GRFC2	64	DO	Generic RF controller	1.8 V power domain.

Table 30: Truth Table of GRFC Interfaces

GRFC1	GRFC2	Frequency Range (MHz)	Band
Low	Low	880–2200	B1, B2, B3, B4, B8, B25, B66
High	Low	791–894	B5, B18, B19, B20, B26, B27
Low	High	698–803	B12, B13, B28, B85
High	High	617–698	B71

NOTE

GRFC1 (pin 63) is a BOOT_CONFIG pin. Do not pull it up before startup.

4 GNSS

4.1. General Description

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo and QZSS.

The module supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, the GNSS engine is switched off. It has to be switched on via AT command. The module does not support concurrent operation of WWAN and GNSS. For more details about GNSS engine technology and configurations, see ***document [1]***.

4.2. GNSS Performance

Table 31: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-147	dBm
	Reacquisition	Autonomous	-160	dBm
	Tracking	Autonomous	-159	dBm
TTFF	Cold start @ open sky	Autonomous	30.53	s
		XTRA enabled	2.16	s
	Warm start @ open sky	Autonomous	25.61	s
		XTRA enabled	1.15	s
	Hot start	Autonomous	1.5	s

	@ open sky	XTRA enabled	1.10	s
Accuracy	CEP-50	Autonomous @ open sky	2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in application designs.

- Maximize the distance between the GNSS antenna and the main antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for ANT_GNSS trace.

See ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

The module includes a main antenna interface and a GNSS antenna interface. The impedance of antenna interfaces is 50 Ω.

5.1. Main Antenna Interface

5.1.1. Pin Definition

Table 32: Pin Definition of Main Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	41	AIO	Main antenna interface	50 Ω impedance

5.1.2. Operating Frequency

Table 33: Operating Frequency

3GPP Band	Transmit	Receive	Unit
LTE HD-FDD B1	1920–1980	2110–2170	MHz
LTE-HD-FDD B2, PCS1900	1850–1910	1930–1990	MHz
LTE HD-FDD B3, DCS1800	1710–1785	1805–1880	MHz
LTE HD-FDD B4	1710–1755	2110–2155	MHz
LTE HD-FDD B5, GSM850	824–849	869–894	MHz
LTE HD-FDD B8, EGSM900	880–915	925–960	MHz
LTE HD-FDD B12	699–716	729–746	MHz
LTE HD-FDD B13	777–787	746–756	MHz

LTE HD-FDD B18	815–830	860–875	MHz
LTE HD-FDD B19	830–845	875–890	MHz
LTE HD-FDD B20	832–862	791–821	MHz
LTE HD-FDD B25	1850–1915	1930–1995	MHz
LTE HD-FDD B26 [4]	814–849	859–894	MHz
LTE HD-FDD B27 [4]	807–824	852–869	MHz
LTE HD-FDD B28	703–748	758–803	MHz
LTE HD-FDD B66	1710–1780	2110–2180	MHz
LTE HD-FDD B71 [5]	663–698	617–652	MHz
LTE HD-FDD B85	698–716	728–746	MHz

5.1.3. Reference Design

A reference design of main antenna interface is shown as below. It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1/C1/C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

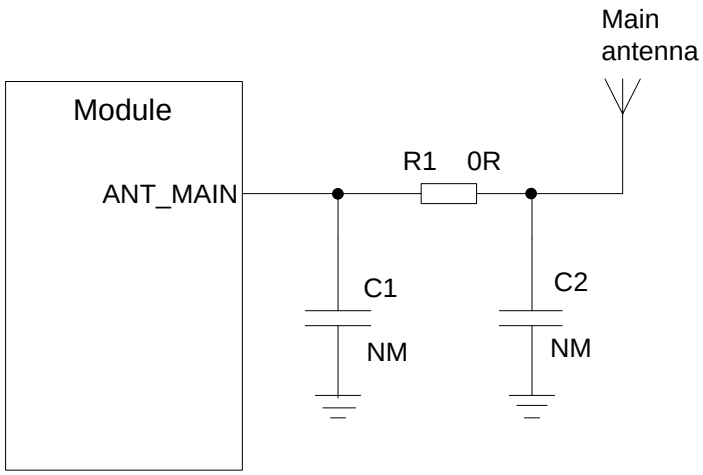


Figure 28: Reference Design of Main Antenna Interface

[4] LTE HD-FDD B26 and B27 are supported by LTE Cat M1 only.
[5] LTE HD-FDD B71 is supported by LTE Cat NB2 only.

5.2. GNSS Antenna Interface

5.2.1. Pin Definition

Table 34: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	15	AI	GNSS antenna interface	50 Ω impedance

5.2.2. GNSS Operating Frequency

Table 35: GNSS Operating Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz
QZSS	1575.42 ±1.023	MHz

5.2.3. Reference Design

A reference design of GNSS antenna interface is shown as below.

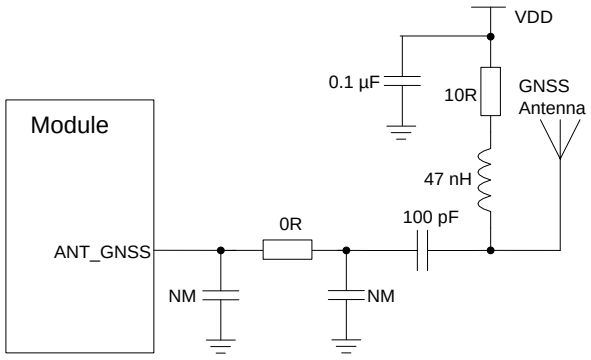


Figure 29: Reference Design of GNSS Antenna Interface

NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. RF Routing Guidelines

For users' PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

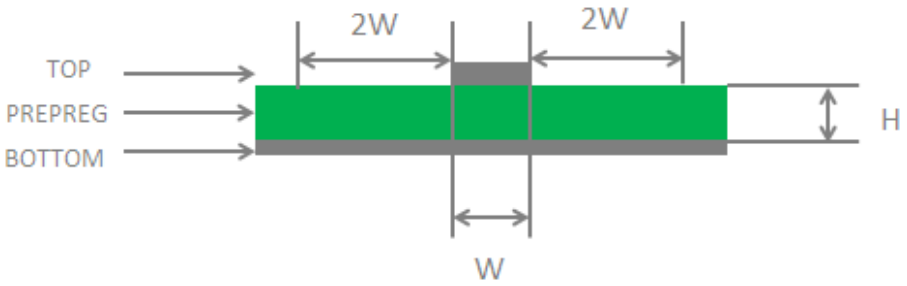


Figure 30: Microstrip Design on a 2-layer PCB

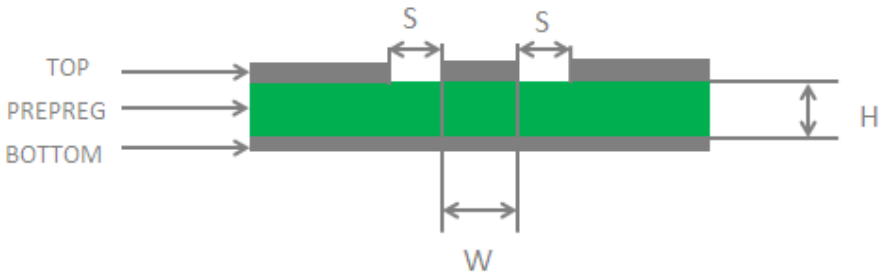


Figure 31: Coplanar Waveguide Design on a 2-layer PCB

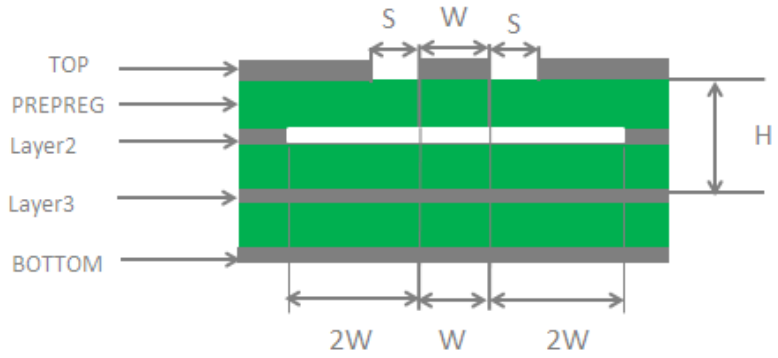


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

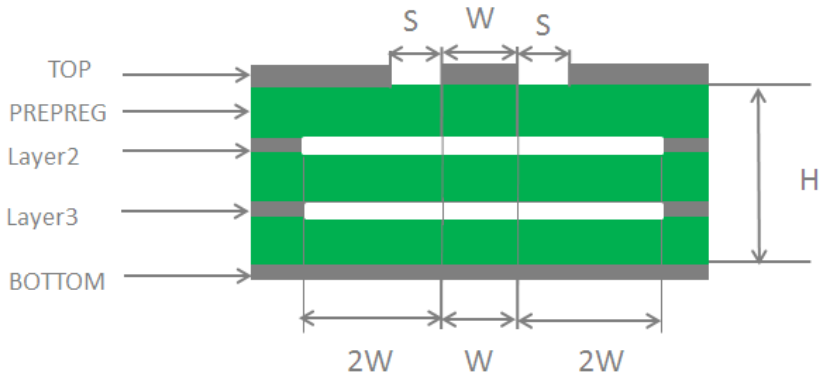


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [6]***.

5.4. Antenna Installation

5.4.1. Antenna Design Requirements

Table 36: Antenna Requirements

Antenna Type	Requirements
GNSS	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0 dBi Active antenna noise figure: < 1.5 dB Active antenna gain: > 0 dBi Active antenna embedded LNA gain: < 17 dB
LTE/GSM	VSWR: ≤ 2 Efficiency: > 30 % Max Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz)

NOTE

It is recommended to use a passive GNSS antenna when LTE HD-FDD B13 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.4.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connectors provided by HIROSE.

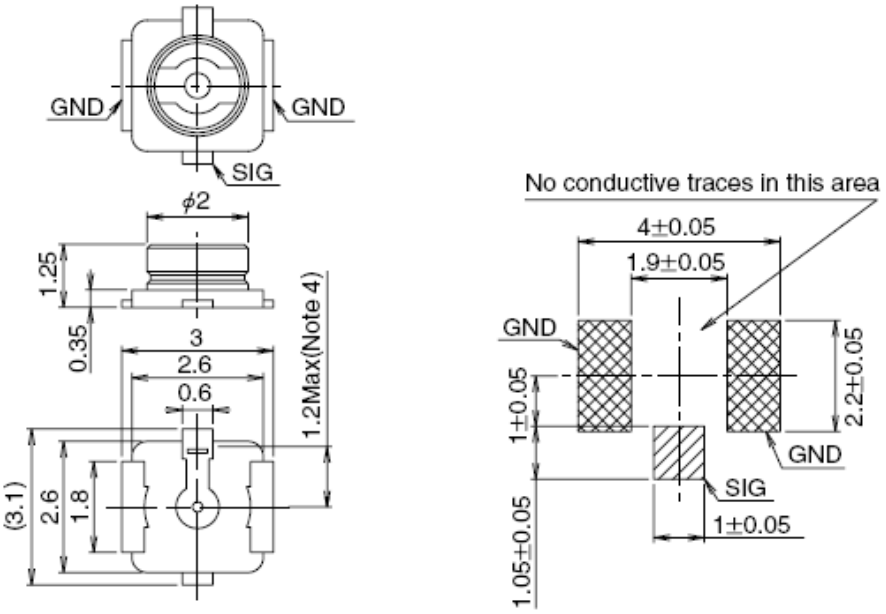


Figure 34: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

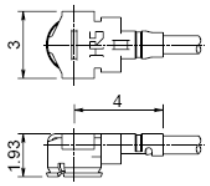
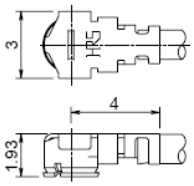
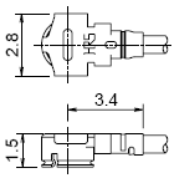
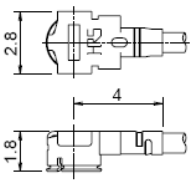
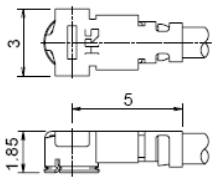
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 35: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

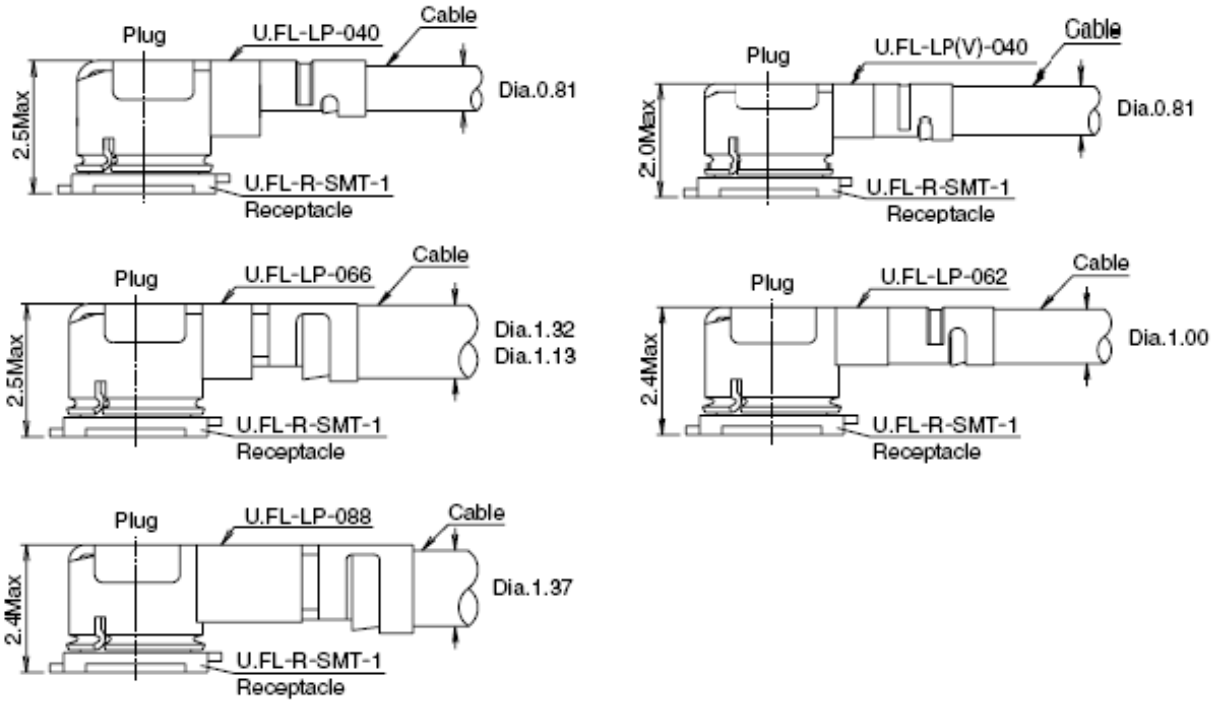


Figure 36: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 37: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_BB	-0.5	6.0	V
VBAT_RF	-0.3	6.0	V
USB_VBUS	1.3	1.8	V
Voltage at Digital Pins	-0.3	2.09	V

6.2. Power Supply Ratings

Table 38: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB/VBAT_RF	The actual input voltages must be kept between the minimum and the maximum values.	3.3	3.8	4.3	V
I_{VBAT}	Peak current of power supply (during transmission	Maximum power control level on EGSM900	-	1.8	2.7	A

	slot)				
USBPHY_3P3	Power supply for USB PHY circuit	-	3.3	-	V
USB_VBUS	USB connection detection	1.3	-	1.8	V

6.3. Operating and Storage Temperatures

Table 39: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [6]	-35	+25	+75	ºC
Extended Temperature Range [7]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	°C

6.4. Power Consumption

Table 40: Power Consumption

Description	Conditions	Typ.	Unit
Leakage [8]	Power-off @ USB/UART disconnected	13.4	μA
PSM [9]	PSM @ USB/UART disconnected	3.97	μA
Rock Bottom	**AT+CFUN=0** @ Sleep Mode	0.6	mA

[6] Within the operating temperature range, the module meets 3GPP specifications.

[7] Within the extended temperature range, the module remains the ability to establish and maintain functions such as SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

[8] The power consumption of the module in PSM is much lower than that in power off mode due to the following two designs:

- More internal power supplies are powered off in PSM.
- The internal clock frequency is reduced in PSM.

[9] The module's USB and UART interfaces are disconnected, and GSM network does not support PSM.

Sleep Mode (USB disconnected)	LTE Cat M1 DRX = 1.28 s	1.66	mA
	LTE Cat NB1 DRX = 1.28 s	1.47	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	0.66	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	0.69	mA
Idle Mode (USB disconnected)	LTE Cat M1 DRX = 2.56 s	18.14	mA
	LTE Cat NB1 DRX = 2.56 s	14.33	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	17.8	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	14.15	mA
LTE Cat M1 data transfer (GNSS OFF)	LTE HD-FDD B1 @ 20.82 dBm	183.89	mA
	LTE HD-FDD B2 @ 20.9 dBm	186.91	mA
	LTE HD-FDD B3 @ 20.64 dBm	180.23	mA
	LTE HD-FDD B4 @ 20.85 dBm	182.41	mA
	LTE HD-FDD B5 @ 20.71 dBm	190.88	mA
	LTE HD-FDD B8 @ 20.41 dBm	185.95	mA
	LTE HD-FDD B12 @ 20.74 dBm	184.84	mA
	LTE HD-FDD B13 @ 20.69 dBm	198.6	mA
	LTE HD-FDD B18 @ 20.65 dBm	192.59	mA
	LTE HD-FDD B19 @ 20.68 dBm	192.27	mA
	LTE HD-FDD B20 @ 20.4 dBm	191.52	mA
	LTE HD-FDD B25 @ 20.54 dBm	183.77	mA
	LTE HD-FDD B26 @ 20.73 dBm	189.34	mA

	LTE HD-FDD B27 @ 20.63 dBm	193.68	mA
	LTE HD-FDD B28A @ 20.69 dBm	184.34	mA
	LTE HD-FDD B28B @ 20.76 dBm	188.58	mA
	LTE HD-FDD B66 @ 20.95 dBm	183.03	mA
	LTE HD-FDD B85 @ 20.81 dBm	182.73	mA
LTE Cat NB1 data transfer (GNSS OFF)	LTE HD-FDD B1 @ 20.85 dBm	145.15	mA
	LTE HD-FDD B2 @ 20.75 dBm	147.67	mA
	LTE HD-FDD B3 @ 20.92 dBm	145.3	mA
	LTE HD-FDD B4 @ 21.09 dBm	146.31	mA
	LTE HD-FDD B5 @ 20.7 dBm	158.21	mA
	LTE HD-FDD B8 @ 20.56 dBm	152.29	mA
	LTE HD-FDD B12 @ 20.6 dBm	147.8	mA
	LTE HD-FDD B13 @ 20.81 dBm	163.15	mA
	LTE HD-FDD B18 @ 20.68 dBm	156.46	mA
	LTE HD-FDD B19 @ 20.56 dBm	155.17	mA
	LTE HD-FDD B20 @ 20.49 dBm	155.57	mA
	LTE HD-FDD B25 @ 20.78 dBm	147.64	mA
	LTE HD-FDD B28 @ 20.76 dBm	152.18	mA
	LTE HD-FDD B66 @ 20.89 dBm	145.63	mA
	LTE HD-FDD B71 @ 21.08 dBm	142.02	mA
	LTE HD-FDD B85 @ 20.73 dBm	146.11	mA
GPRS data transfer (GNSS OFF)	GSM850 4UL/1DL @ 30 dBm	598	mA
	GSM850 3UL/2DL @ 31 dBm	526	mA
	GSM850 2UL/3DL @ 33 dBm	434	mA
	GSM850 1UL/4DL @ 33 dBm	283	mA

	EGSM900 4UL/1DL @ 30 dBm	621	mA
	EGSM900 3UL/2DL @ 32 dBm	543	mA
	EGSM900 2UL/3DL @ 33 dBm	445	mA
	EGSM900 1UL/4DL @ 33 dBm	289	mA
	DCS1800 4UL/1DL @ 27 dBm	442	mA
	DCS1800 3UL/2DL @ 28 dBm	368	mA
	DCS1800 2UL/3DL @ 30 dBm	306	mA
	DCS1800 1UL/4DL @ 31 dBm	222	mA
	PCS1900 4UL/1DL @ 27 dBm	456	mA
	PCS1900 3UL/2DL @ 28 dBm	365	mA
	PCS1900 2UL/3DL @ 29 dBm	302	mA
	PCS1900 1UL/4DL @ 31 dBm	220	mA
EDGE data transfer (GNSS OFF)	GSM850 4UL/1DL @ 23 dBm	525	mA
	GSM850 3UL/2DL @ 24 dBm	424	mA
	GSM850 2UL/3DL @ 26 dBm	325	mA
	GSM850 1UL/4DL @ 26 dBm	216	mA
	EGSM900 4UL/1DL @ 23 dBm	527	mA
	EGSM900 3UL/2DL @ 24 dBm	425	mA
	EGSM900 2UL/3DL @ 26 dBm	329	mA
	EGSM900 1UL/4DL @ 27 dBm	217	mA
	DCS1800 4UL/1DL @ 22 dBm	461	mA
	DCS1800 3UL/2DL @ 23 dBm	373	mA
	DCS1800 2UL/3DL @ 25 dBm	295	mA
	DCS1800 1UL/4DL @ 26 dBm	210	mA
	PCS1900 4UL/1DL @ 22 dBm	462	mA

	PCS1900 3UL/2DL @ 23 dBm	370	mA
	PCS1900 2UL/3DL @ 25 dBm	286	mA
	PCS1900 1UL/4DL @ 26 dBm	196	mA

Table 41: GNSS Power Consumption (3.8 V Power Supply, Room Temperature)

Description	Conditions	Typ.	Unit
Acquisition (**AT+CFUN=0**)	Cold start @ Instrument	66.51	mA
	Hot start @ Instrument	65.9	mA
	Warm start @ Instrument	66.73	mA
	Lost state @ Instrument	66.89	mA
Tracking (**AT+CFUN=0**)	Instrument Environment @ Passive Antenna	20.8	mA
	Open Sky @ Real network, Passive Antenna	22.74	mA
	Open Sky @ Real network, Active Antenna	23.77	mA

6.5. Tx Power

Table 42: Tx Power

Frequency Bands	Max.	Min.
LTE HD-FDD B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B25/B26 [10]/B27 [10]/B28/B66/B71 [11]/B85	21 dBm +1.7/-3 dB	< -39 dBm
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
GSM850/EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB

[10] LTE HD-FDD B26 and B27 are supported by LTE Cat M1 only.
[11] LTE HD-FDD B71 is supported by LTE Cat NB2 only.

DCS1800/PCS1900 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB

6.6. Rx Sensitivity

Table 43: Conducted Rx Sensitivity (25 °C, 3.8 V)

Mode	Band	Primary	Diversity	Rx Sensitivity (dBm)	
				Cat M1/3GPP	Cat NB2 [12]/3GPP
LTE	LTE HD-FDD B1	Supported	Not Supported	-105 /-102.3	-115/-107.5
	LTE HD-FDD B2			-107/-100.3	-115/-107.5
	LTE HD-FDD B3			-104.8/-99.3	-115/-107.5
	LTE HD-FDD B4			-105.6/-102.3	-115/-107.5
	LTE HD-FDD B5			-105/-100.8	-115/-107.5
	LTE HD-FDD B8			-106/-99.8	-115/-107.5
	LTE HD-FDD B12			-105.5/-99.3	-115/-107.5
	LTE HD-FDD B13			-105.8/-99.3	-115/-107.5
	LTE HD-FDD B18			-106/-102.3	-115/-107.5
	LTE HD-FDD B19			-106/-102.3	-115/-107.5
	LTE HD-FDD B20			-105/-99.8	-115/-107.5
	LTE HD-FDD B25			-108/-100.3	-114/-107.5
	LTE HD-FDD B26			-106/-100.3	Not Supported
	LTE HD-FDD B27			-106/-100.8	Not Supported
	LTE HD-FDD B28			-107/-100.8	-115/-107.5
	LTE HD-FDD B66			-106/-101.8	-115/-107.5
	LTE HD-FDD B71			Not Supported	-115/-107.5

[12] 3GPP has made no demand for LTE Cat NB Rx Sensitivity repetition.

	LTE HD-FDD B85			-106/-99.3	-115/-107.5

Mode	Band	Primary	Diversity	Rx Sensitivity (dBm)
				GSM/3GPP
GSM	GSM850/EGSM900	Supported	Not Supported	-107/-102
	DCS1800/PCS1900			-107/-102

6.7. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 44: Electrostatic Discharge Characteristics (25 ºC, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±6	±8	kV
Main/GNSS Antenna Interfaces	±5	±6	kV

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

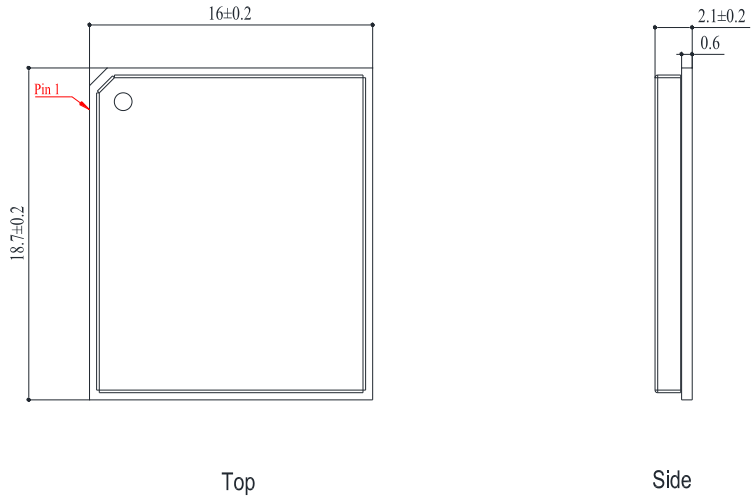


Figure 37: Module Top and Side Dimensions

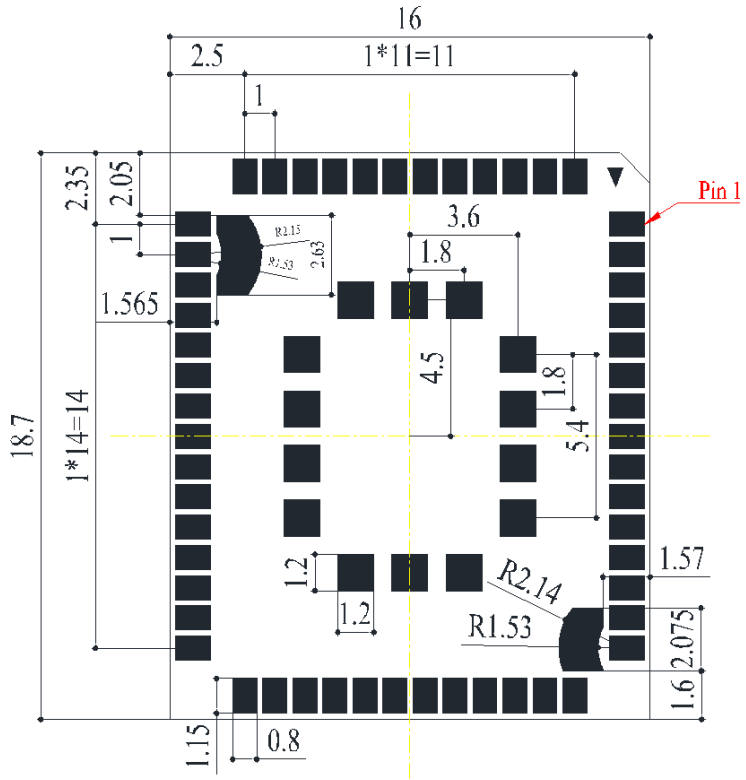


Figure 38: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

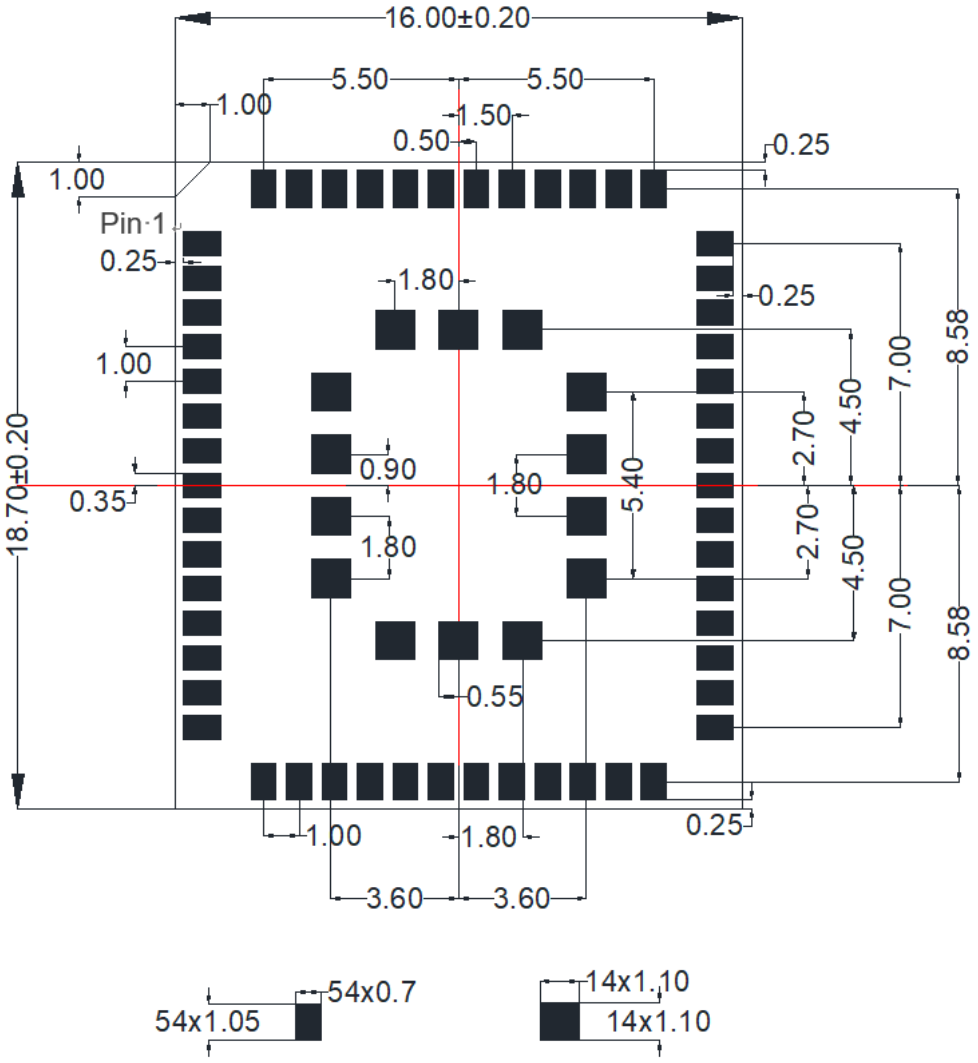


Figure 39: Recommended Footprint (Top View)

NOTE

1. For easy maintenance of the module, keep a distance of about 3 mm between the module and other components on the motherboard.
2. All RESERVED pins must be kept open.

7.3. Top and Bottom Views

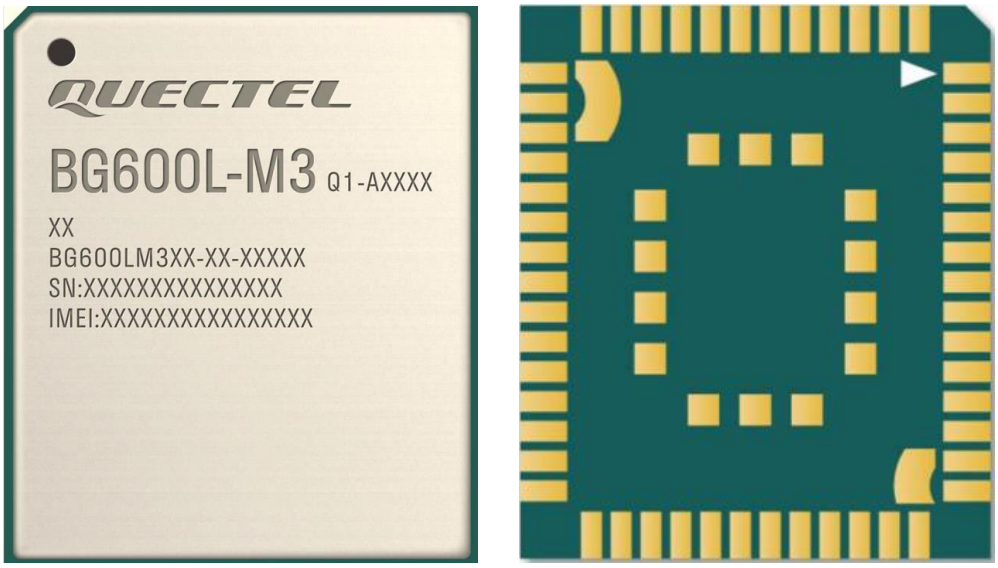


Figure 40: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [13] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[13] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [7]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

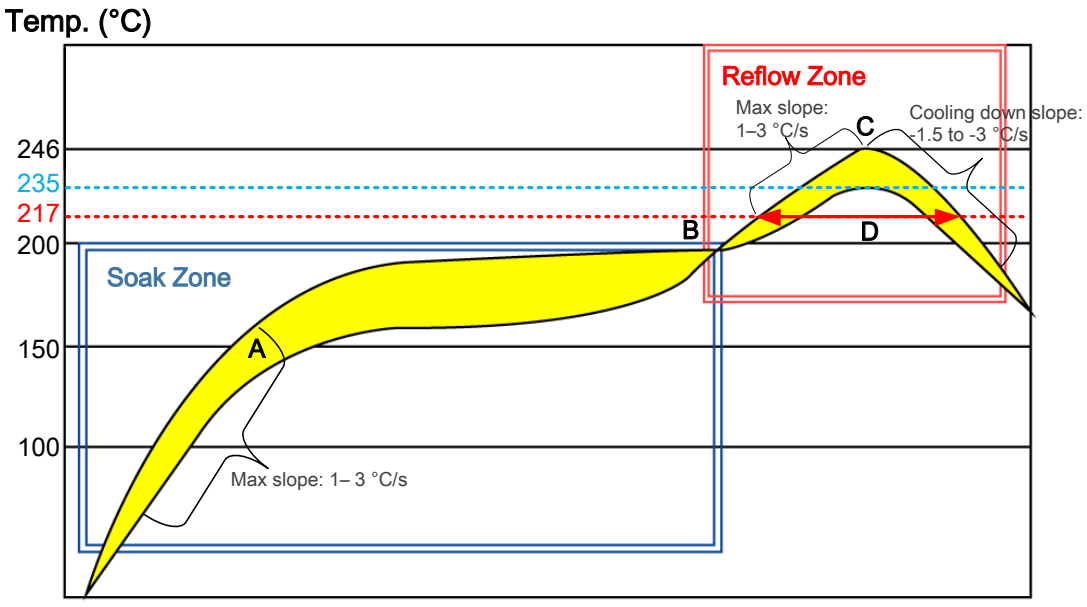


Figure 41: Recommended Reflow Soldering Thermal Profile

Table 45: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	1–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235–246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [7]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

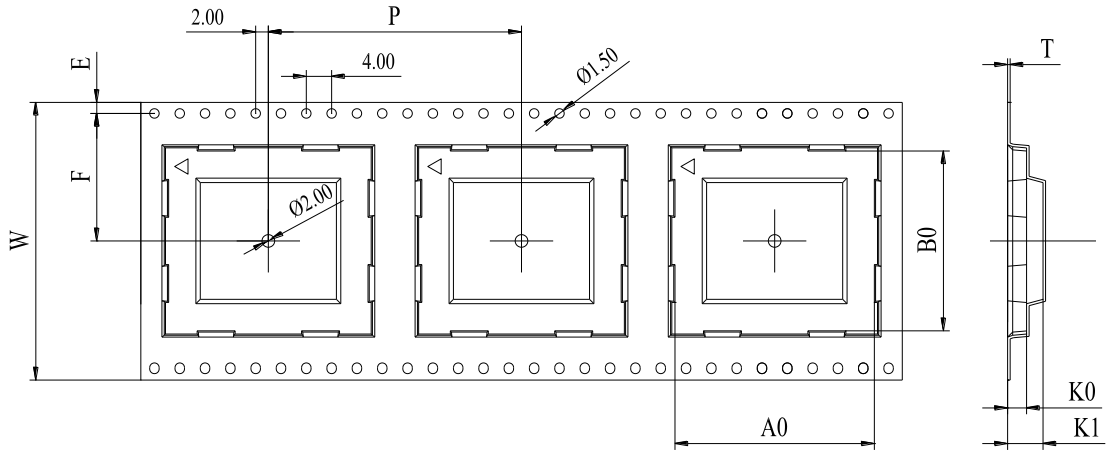


Figure 42: Carrier Tape Dimension Drawing

Table 46: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	24	0.4	16.4	19.0	2.9	7.9	14.2	1.75

8.3.2. Plastic Reel

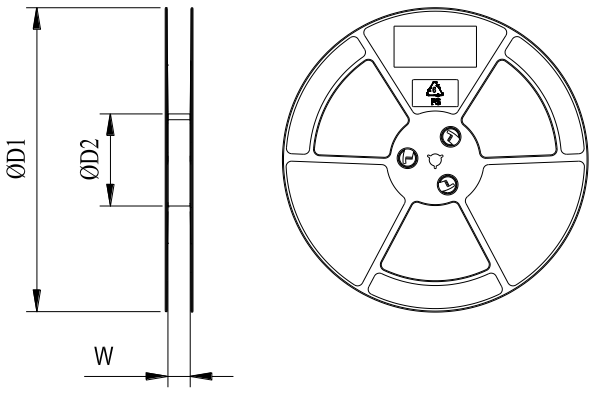
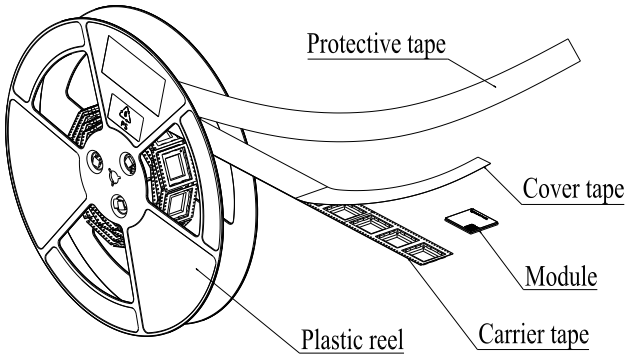


Figure 43: Plastic Reel Dimension Drawing

Table 47: Plastic Reel Dimension Table (Unit: mm)

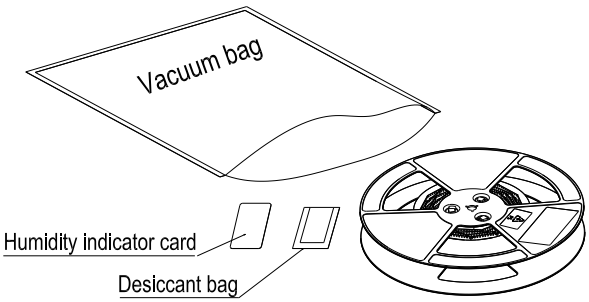
øD1	øD2	W
330	100	32.5

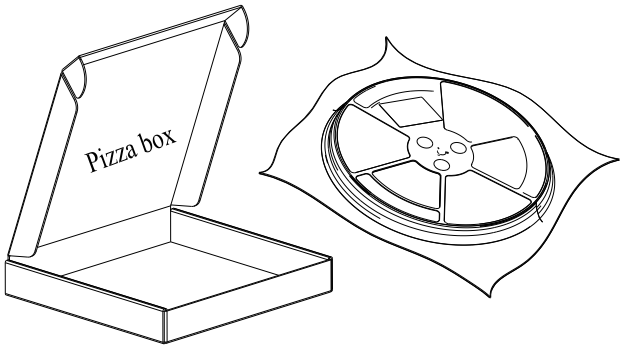
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 cartoon box can pack 1000 modules.

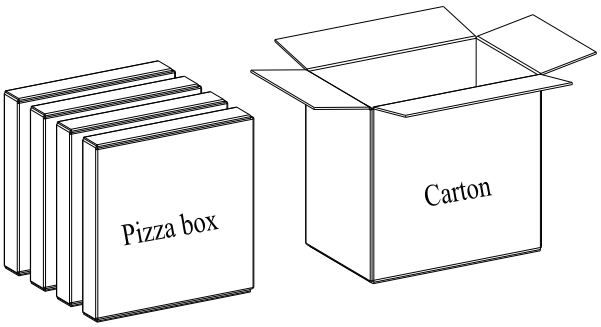


Figure 44: Packaging Process

9 Appendix References

Table 48: Related Documents

Document Name
[1] Quectel_BG95&BG77&BG600L_Series_GNSS_Application_Note
[2] Quectel_LTE_OPEN_EVB_User_Guide
[3] Quectel_BG95&BG77&BG600L_Series_AT_Commands_Manual
[4] Quectel_BG95&BG77&BG600L_Series_QuecOpen_Extended_QAPI_Reference_Manual
[5] Quectel_BG95&BG77&BG600L_Series_QCFG_AT_Commands_Manual
[6] Quectel_RF_Layout_Application_Note
[7] Quectel_Module_Secondary_SMT_Application_Note

Table 49: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
bps	bit(s) per second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
e-I-DRX	Extended Idle Mode Discontinuous Reception
EDGE	Enhanced Data Rates for GSM Evolution

EGPRS	Enhanced General Packet Radio Service
EGSM	Extended GSM (Global System for Mobile Communications)
EPC	Evolved Packet Core
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HD-FDD	Half-duplex FDD
HSS	Home Subscriber Server
I2C	Inter-Integrated Circuit
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
ME	Mobile Equipment
MO	Mobile Originated
MS	Mobile Station
MSL	Moisture Sensitivity Level
MT	Mobile Terminated
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDN	Packet Data network
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
PSM	Power Saving Mode

RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SAW	Surface Acoustic Wave
SMS	Short Message Service
SPI	Serial Peripheral Interface
TAU	Tracking Area Update
TCP	Transmission Control Protocol
TDM	Time-Division Multiplexing
TVS	Transient Voltage Suppressor
UL	Uplink
UE	User Equipment
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
$V_{IH}max$	Maximum High-level Input Voltage
$V_{IH}min$	Minimum High-level Input Voltage
$V_{IL}max$	Maximum Low-level Input Voltage
$V_{IL}min$	Minimum Low-level Input Voltage
$V_{OH}min$	Minimum High-level Output Voltage
$V_{OL}max$	Maximum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WWAN	Wireless Wide Area Network